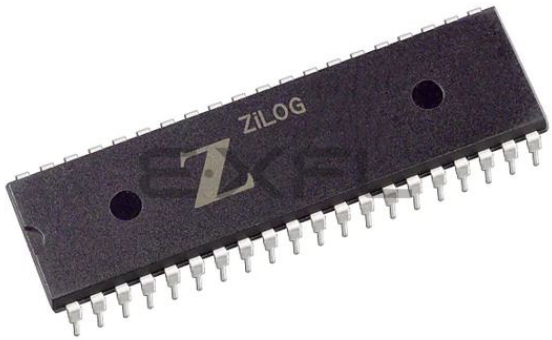

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	-
Peripherals	LVD, POR, WDT
Number of I/O	31
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.620", 15.75mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e7316psc

Features

Table 1 lists some of the features of the Z86E72/73 microcontrollers.

Table 1. Z86E72/73 Features

Part	ROM (KB)	RAM* (Bytes)	I/O	Voltage Range
Z86E73	32	236	31	3.0 V to 5.5 V
Z86E72	16	748	31	3.0 V to 5.5 V

Note: *General-purpose

- Low power consumption—60 mW (typical)
- Two standby modes (typical)
  - STOP—2 μA
  - HALT—0.8 mA
- Special architecture to automate both generation and reception of complex pulses or signals:
  - One programmable 8-bit counter/timer with two capture registers
  - One programmable 16-bit counter/timer with one capture register
  - Programmable input glitch filter for pulse reception
- Five priority interrupts
  - Three external
  - Two assigned to counter/timers
- Two independent comparators with programmable interrupt polarity
- On-chip oscillator that accepts a crystal, ceramic resonator, LC, RC (mask option), or external clock drive
- Software-selectable 200±50% KΩ resistive transistor pull-ups on Port 0 and Port 2
  - Port 2 pull-ups are bit selectable
  - Pull-ups automatically disabled as outputs
- Software mouse/trackball interface on P00 through P03

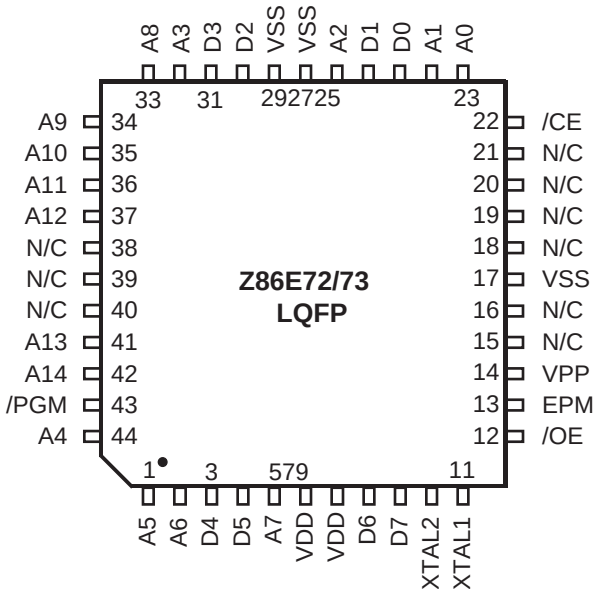


Figure 8. 44-Pin LQFP Pin Assignments (EPROM Mode)

Table 3 identifies the pins in packages in standard mode. Table 4 on page 11 identifies the pins in the 40-pin DIP in EPROM mode. Table 5 on page 12 identifies the pins in the 44-pin LQFP and PLCC.

Table 3. Pin Identification (Standard Mode)

40-Pin DIP #	44-Pin PLCC #	44-Pin LQFP #	Symbol	Direction	Description
26	40	23	P00	Input/Output	Port 0 is Nibble Programmable.
27	41	24	P01	Input/Output	Port 0 can be configured as A15–A8 external program
30	44	27	P02	Input/Output	
34	5	32	P03	Input/Output	ROM Address Bus.
5	17	44	P04	Input/Output	Port 0 can be configured as a
6	18	1	P05	Input/Output	mouse/trackball input.
7	19	2	P06	Input/Output	
10	22	5	P07	Input/Output	
28	42	25	P10	Input/Output	Port 1 is byte programmable.

Table 3. Pin Identification (Standard Mode) (Continued)

40-Pin DIP #	44-Pin PLCC #	44-Pin LQFP #	Symbol	Direction	Description
29	43	26	P11	Input/Output	Port 1 can be configured as multiplexed A7–A0/D7–D0 external program ROM Address/Data Bus
32	3	30	P12	Input/Output	
33	4	31	P13	Input/Output	
8	20	3	P14	Input/Output	.
9	21	4	P15	Input/Output	
12	25	8	P16	Input/Output	
13	26	9	P17	Input/Output	
35	6	33	P20	Input/Output	Port 2 pins are individually configurable as input or output
36	7	34	P21	Input/Output	
37	8	35	P22	Input/Output	
38	9	36	P23	Input/Output	
39	10	37	P24	Input/Output	
2	14	41	P25	Input/Output	
3	15	42	P26	Input/Output	
4	16	43	P27	Input/Output	
16	29	12	P31	Input	IRQ2/Modulator input
17	30	13	P32	Input	IRQ0
18	31	14	P33	Input	IRQ1
19	32	15	P34	Output	T8 output
22	36	19	P35	Output	T16 output
24	38	21	P36	Output	T8/T16 output
23	37	20	P37	Output	
20	33	16	/AS	Output	Address Strobe
40	11	38	/DS	Output	Data Strobe
1	13	40	R//W	Output	Read/Write
21	35	18	/RESET	Input	Reset
15	28	11	XTAL1	Input	Crystal, Oscillator Clock

Table 5. Z86E72/73 44-Pin LQFP/PLCC Pin Identification—EPROM Mode

44-Pin LQFP	44-Pin PLCC	Symbol	Function	Direction
41–42	14–15	A13–A14	Address 13, 14	Input
43	16	/PGM	Prog. Mode	Input
44	17	A4	Address 4	Input

Absolute Maximum Ratings

Table 6 lists the absolute maximum ratings for the Z86E72/73 microcontrollers.

Table 6. Absolute Maximum Ratings

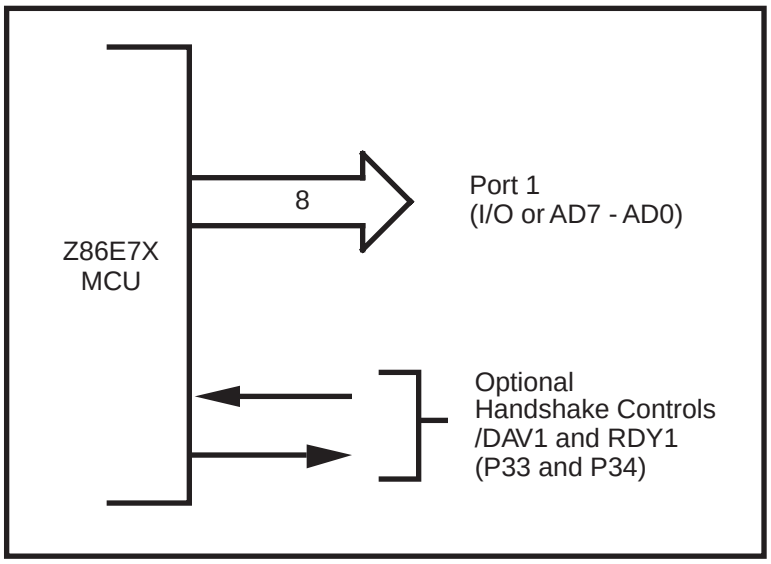
Symbol	Description	Min	Max	Units
V_{MAX}	Supply Voltage (*)	–0.3	+7.0	V
T_{STG}	Storage Temperature	–65°	+150°	C
T_A	Oper. Ambient Temperature		†	C

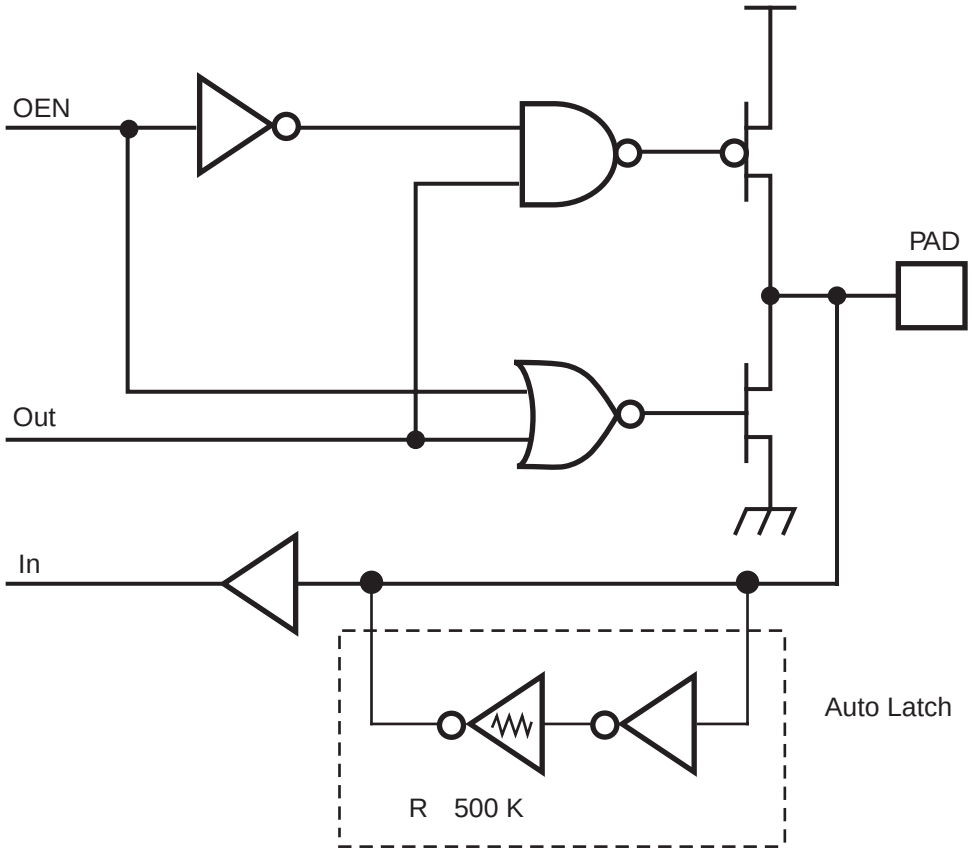
Notes:
* Voltage on all pins with respect to GND.
† See “Ordering Information” on page 97.

Stresses greater than those listed under Absolute Maximum Ratings might cause permanent damage to the device. This rating is a stress rating only. Operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period might affect device reliability.

Table 9. External I/O or Memory Read and Write Timing

				T_A = 0 °C to +70 °C 16 MHz			
No.	**Symbol**	**Parameter**	**V_{CC}**	**Min.**	**Max.**	**Units**	**Notes**
1	TdA(AS)	Address Valid to /AS Rising Delay	3.0 V 5.5 V	55 55		ns ns	2
2	TdAS(A)	/AS Rising to Address Float Delay	3.0 V 5.5 V	70 70		ns ns	2
3	TdAS(DR)	/AS Rising to Read Data Required Valid	3.0 V 5.5 V		400 400	ns ns	1, 2 1, 2
4	TwAS	/AS Low Width	3.0 V 5.5 V	80 80		ns ns	2 2
5	Td	Address Float to /DS Falling	3.0 V 5.5 V	0 0		ns ns	
6	TwDSR	/DS (Read) Low Width	3.0 V 5.5 V	300 300		ns ns	1, 2
7	TwDSW	/DS (Write) Low Width	3.0 V 5.5 V	165 165		ns ns	1, 2
8	TdDSR(DR)	/DS Falling to Read Data Required Valid	3.0 V 5.5 V		260 260	ns ns	1, 2
9	ThDR(DS)	Read Data to /DS Rising Hold Time	3.0 V 5.5 V	0 0		ns ns	
10	TdDS(A)	/DS Rising to Address Active Delay	3.0 V 5.5 V	85 95		ns ns	2
11	TdDS(AS)	/DS Rising to /AS Falling Delay	3.0 V 5.5 V	60 70		ns ns	2
12	TdR/W(AS)	R//W Valid to /AS Rising Delay	3.0 V 5.5 V	70 70		ns ns	2
13	TdDS(R/W)	/DS Rising to R//W Not Valid	3.0 V 5.5 V	70 70		ns ns	2
14	TdDW(DSW)	Write Data Valid to /DS Falling (Write) Delay	3.0 V 5.5 V	80 80		ns ns	2
15	TdDS(DW)	/DS Rising to Write Data Not Valid Delay	3.0 V 5.5 V	70 80		ns ns	2
16	TdA(DR)	Address Valid to Read Data Required Valid	3.0 V 5.5 V		475 475	ns ns	1, 2


Z86E7X
MCU
8
Port 1
(I/O or AD7 - AD0)
Optional
Handshake Controls
/DAV1 and RDY1
(P33 and P34)


OEN
PAD
Out
In
Auto Latch
R 500 K

/RESET (Input, Active Low)

Reset initializes the MCU. Reset is accomplished either through Power-On, Watch-Dog Timer, Stop-Mode Recovery, Low-Voltage detection, or external reset. During Power-On Reset and Watch-Dog Timer Reset, the internally generated reset drives the reset pin Low for the POR time. Any devices driving the reset line need to be open-drain to avoid damage from a possible conflict during reset conditions. Pull-up is provided internally. There is no condition internal to the Z86E7X that does not allow an external reset to occur.

After the POR time, /RESET is a Schmitt-triggered input. To avoid asynchronous and noisy reset problems, the Z86E7X is equipped with a reset filter of four external clocks (4TpC). If the external reset signal is less than 4TpC in duration, no reset occurs. On the fifth clock after the reset is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks or for the duration of the external reset, whichever is longer.

During the reset cycle, /DS is held active Low while /AS cycles at a rate of TpC/2. Program execution begins at location 000CH, 5–10 TpC cycles after the RST is released. For Power-On Reset, the typical reset output time is 5 ms.

Note: The Z86E7X devices do not have internal pull resistors on Port 3 inputs.

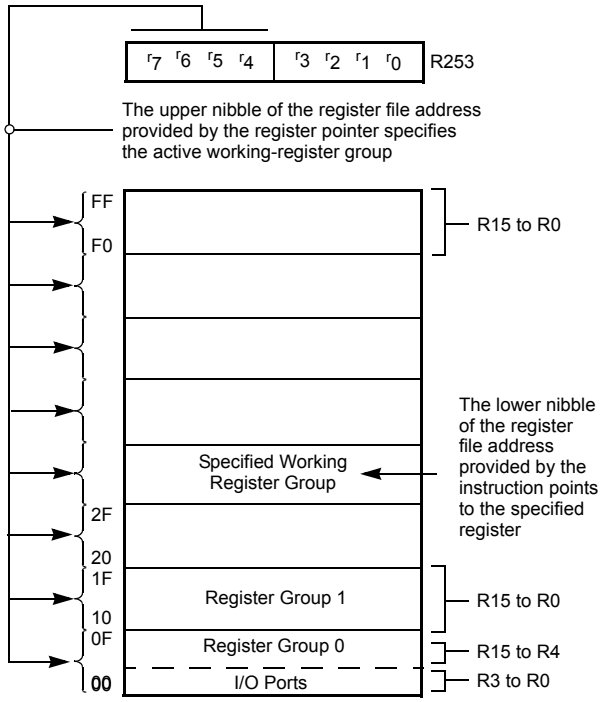


Figure 24. Register Pointer

Stack

The Z86E7X external data memory or the internal register file is used for the stack. An 8-bit stack pointer (R255) is used for the internal stack that resides in the general-purpose registers (R4–R239). SPH is used as a general-purpose register only when using internal stacks.

Note: When SPH is used as a general-purpose register and Port 0 is in address mode, the contents of SPH are loaded into Port 0 whenever the internal stack is accessed.

Counter/Timer Register Description

Table 13 describes the expanded register group D.

Table 13. Expanded Register Group D

(D) 0Ch	Reserved
(D) 0Bh	HI8
(D) 0Ah	LO8

HI16(D)09h Register

This register (Table 16) holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the MS-Byte of the data.

Table 16. HI16(D)09h Register

Field	Bit Position	Value	Description
T16_Capture_HI	76543210	R/W	Captured Data No Effect

L016(D)08h Register

This register (Table 17) holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the LS-Byte of the data.

Table 17. LO16(D)08h Register

Field	Bit Position	Value	Description
T16_Capture_LO	76543210	R/W	Captured Data No Effect

TC16H(D)07h Register

Table 18 describes the Counter/Timer2 MS-Byte Hold Register.

Table 18. TC16H(D)07h Register

Field	Bit Position	Value	Description
T16_Data_HI	76543210	R/W	Data

TC16L(D)06h Register

Table 19 describes the Counter/Timer2 LS-Byte Hold Register.

Table 19. TC16L(D)06h Register

Field	Bit Position	Value	Description
T16_Data_LO	76543210	R/W	Data

TC8H(D)05h Register

Table 20 describes the Counter/Timer8 High Hold Register.

Table 20. TC8H(D)05h Register

Field	Bit Position	Value	Description
T8_Level_HI	76543210	R/W	Data

TC8L(D)04h Register

Table 21 describes the Counter/Timer8 Low Hold Register.

Table 21. TC8L(D)04h Register

Field	Bit Position	Value	Description
T8_Level_LO	76543210	R/W	Data

CTR0(D)00h Register

Table 22 describes the Counter/Timer8 Control Register.

Table 22. CTR0(D)00h Register

Field	Bit Position		Value	Description
T8_Enable	7-------	R	0*	Counter Disabled
			1	Counter Enabled
		W	0	Stop Counter
			1	Enable Counter
Single/Modulo	-6------	R/W	0	Modulo-N
			1	Single Pass
Time_Out	--5------	R	0	No Counter Time-Out
			1	Counter Time-Out Occurred
			0	No Effect
		W	1	Reset Flag to 0
T8 _Clock	---43---	R/W	0 0	SCLK
			0 1	SCLK/2
			1 0	SCLK/4
			1 1	SCLK/8
Capture_INT_MASK	-----2--	R/W	0	Disable Data Capture Int.
			1	Enable Data Capture Int.

Starting Ping-Pong Mode

First, make sure both counter/timers are not running. Then set T8 into Single-Pass Mode (CTR0 D6), set T16 into Single-Pass Mode (CTR2 D6), and set Ping-Pong Mode (CTR1 D2, D3). These instructions do not have to be in any particular order. Finally, start Ping-Pong Mode by enabling either T8 (CTR0 D7) or T16 (CTR2 D7).

During Ping-Pong Mode

The enable bits of T8 and T16 (CTR0 D7, CTR2 D7) are alternately set and cleared by hardware. The time-out bits (CTR0 D5, CTR2 D5) are set every time the counter/timers reach the terminal count.

Output Circuit

Figure 36 shows the output circuit.

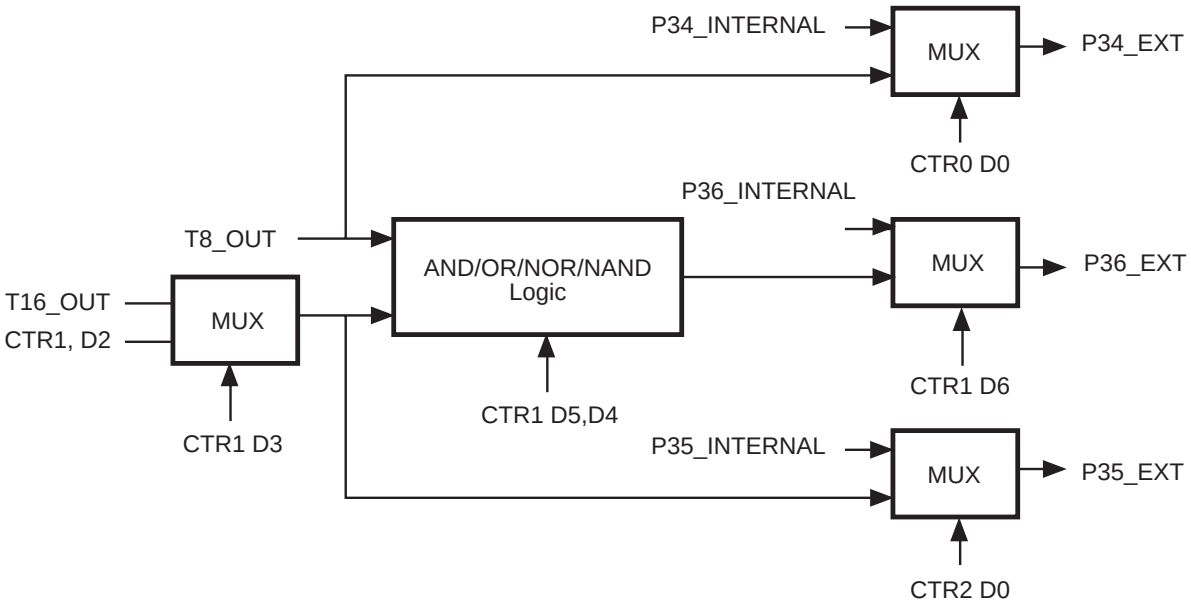


Figure 36. Output Circuit

Interrupts

The Z86E7X has five different interrupts. The interrupts are maskable and prioritized, as shown in Figure 37. The five sources are divided as follows: three sources are claimed by Port 3 lines P33–P31 and the remaining two by the counter/timers (see Table 26). The Interrupt Mask Register globally or individually enables or disables the five interrupt requests.

The crystal must be connected across XTAL1 and XTAL2 using the recommended capacitors (capacitance greater than or equal to 22 pF) from each pin to ground. The RC oscillator configuration is an external resistor connected from XTAL1 to XTAL2, with a frequency-setting capacitor from XTAL1 to ground (see Figure 38).

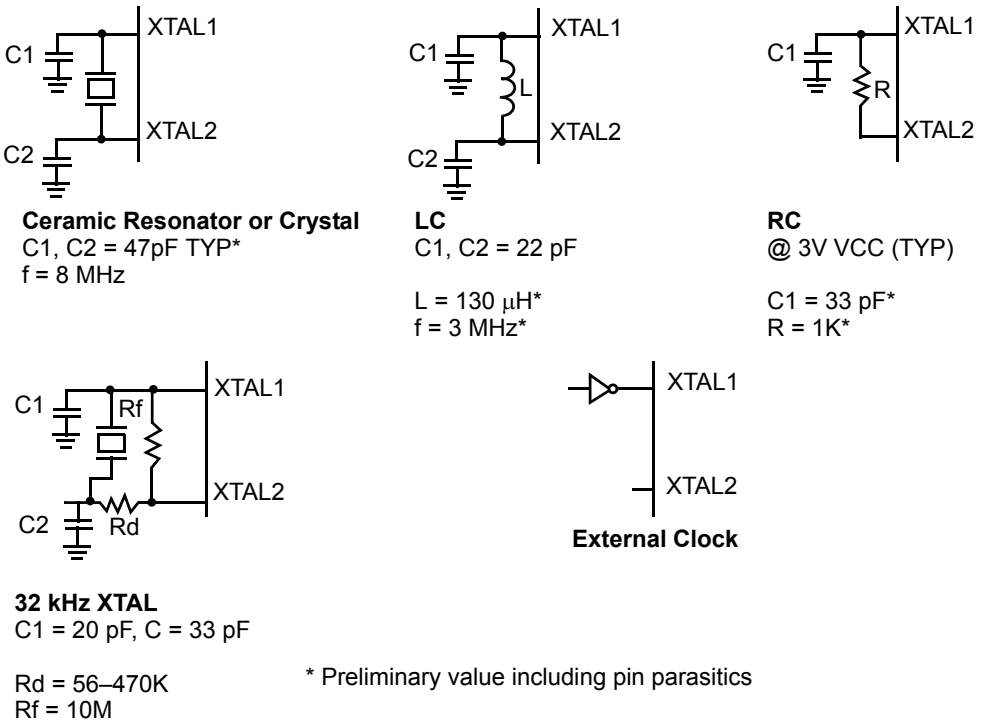


Figure 38. Oscillator Configuration

Power-On Reset (POR)

A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR time allows VCC and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

- Power Fail to Power OK status.
- Stop-Mode Recovery (if D5 of SMR = 1).
- WDT Time-Out.

The POR time is a nominal 5 ms. Bit 5 of the Stop-Mode Register determines whether the POR timer is bypassed after Stop-Mode Recovery (typical for external clock, RC, and LC oscillators).

HALT

HALT turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, IRQ3, and IRQ4 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP

This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 μA (typical) or less. STOP Mode is terminated only by a reset, such as WDT time-out, POR, SMR, or external reset. This causes the processor to restart the application program at address 000CH. To enter STOP (or HALT) mode, you need to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, you must execute a NOP (op code = FFH) immediately before the appropriate sleep instruction. For example:

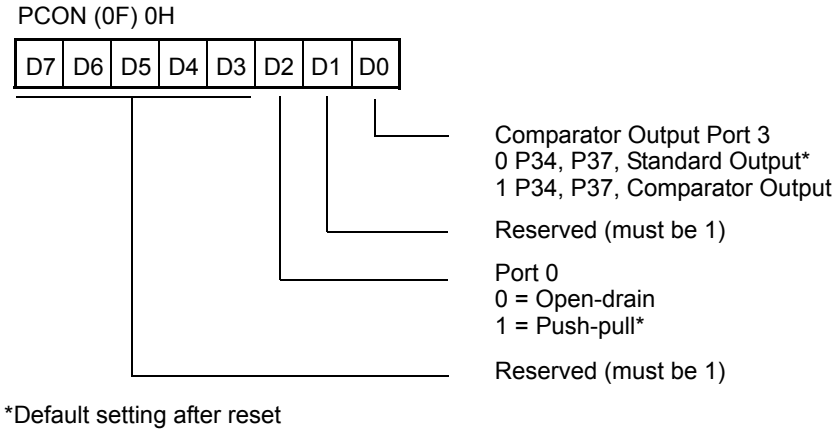
```
FF          NOP         ; clear the pipeline
6F          STOP        ; enter STOP Mode
```

or

```
FF          NOP         ; clear the pipeline
7F          HALT        ; enter HALT Mode
```

Port Configuration Register (PCON)

The PCON register (Figure 39) configures the comparator output on Port 3. It is located in the expanded register file at Bank F, location 00.



*Default setting after reset

Figure 39. Port Configuration Register (PCON)—Write Only

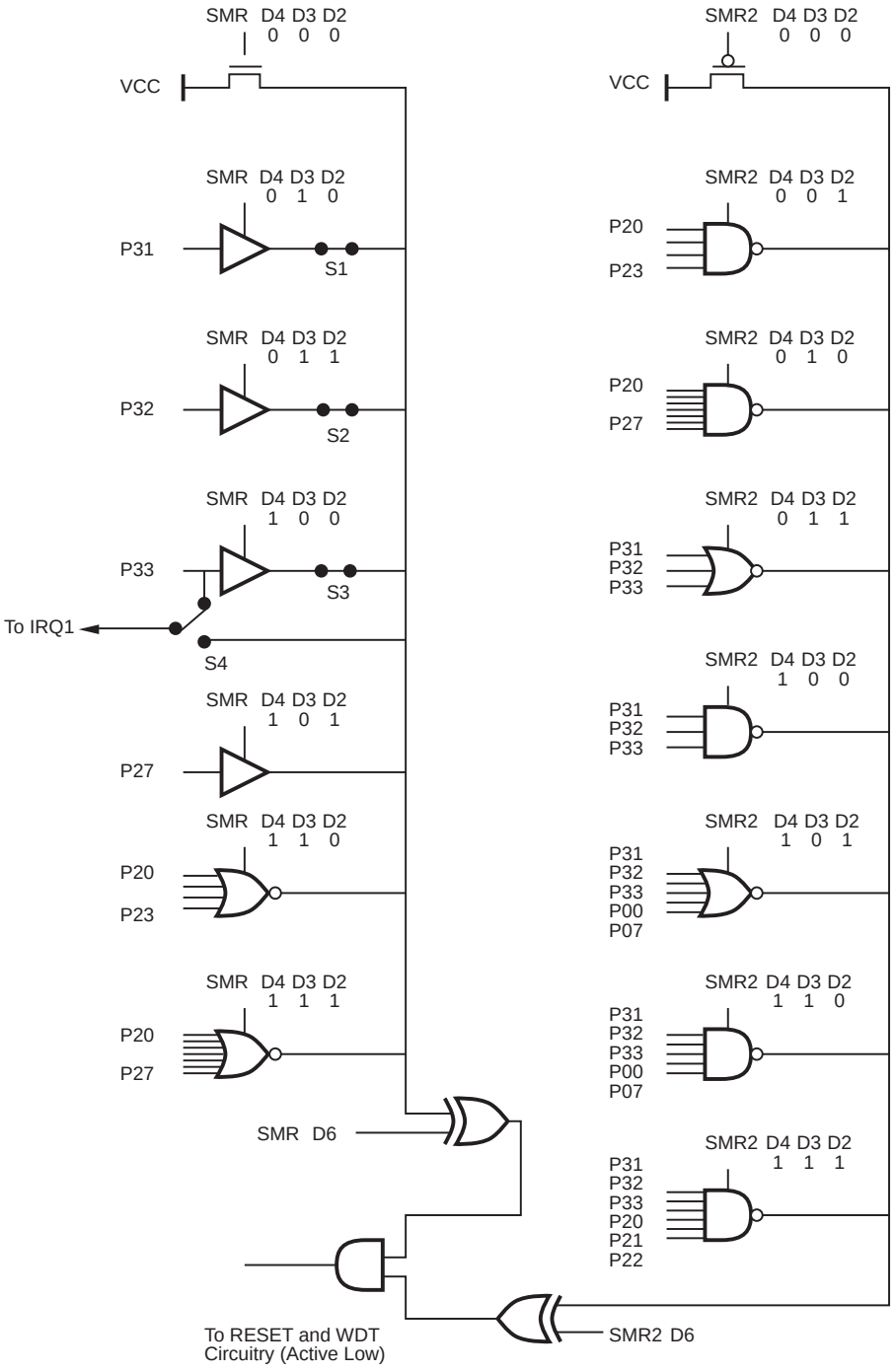


Figure 40. Stop-Mode Recovery Register

EPROM Programming

Table 31 describes the programming and test modes.

Table 31. Programming and Test Modes

	Device Pins									
User/Test Mode Device Pin # User Modes	**P33 V_{PP}**	**P32 EPM**	**Pref1 /CE**	**P31 /OE**	**P20 /PGM**	**Addr**	**V_{CC}**	**Port 1 CNFG DATA**	**Test ADDR A0–A3**	**Note**
EPROM Read	V_{CC}	V_H	V_{IL}	V_{IL}	V_{IH}	Addr	3.0 V	Out	XX	
Program	V_{PP}	V_{CC}	V_{IL}	V_{IH}	V_{IL}	Addr	6.0 V	In	XX	
Program Verify	V_{PP}	V_{CC}	V_{IL}	V_{IL}	V_{IH}	Addr	6.0 V	Out	XX	
RC Option	V_{PP}	V_{CC}	V_H	V_{IH}	V_{IL}	XX	6.0 V	XX	XX	
Margin Read	V_{VA}	V_H	V_{IL}	V_H	V_{IH}	Addr	6.0 V	Out	00	1
Shadow Row Rd	V_{CC}	V_H	V_{IL}	V_{IL}	V_{IH}	COL	3.0 V	Out	01	1
Shadow Row Prg	V_{PP}	V_H	V_{IL}	V_{IH}	V_{IL}	COL	6.0 V	In	01	1
Shadow Row Ver	V_{PP}	V_H	V_{IL}	V_{IL}	V_{IH}	COL	6.0 V	Out	01	1
Shadow Col Rd	V_{CC}	V_H	V_{IL}	V_{IL}	V_{IH}	ROW	3.0 V	Out	02	1
Shadow Col Prg	V_{PP}	V_H	V_{IL}	V_{IH}	V_{IL}	ROW	6.0 V	In	03	1
Shadow Col Ver	V_{PP}	V_H	V_{IL}	V_{IL}	V_{IH}	ROW	6.0 V	Out	02	1
Page Prg 2 Byte	V_{PP}	V_H	V_{IL}	V_{IH}	V_{IL}	TBD	6.0 V	In	04	1
Page Prg 4 Byte	V_{PP}	V_H	V_{IL}	V_{IH}	V_{IL}	TBD	6.0 V	In	05	1
Page Prg 8 Byte	V_{PP}	V_H	V_{IL}	V_{IH}	V_{IL}	TBD	6.0 V	In	06	1
Page Prg 16 Byte	V_{PP}	V_H	V_{IL}	V_{IH}	V_{IL}	TBD	6.0 V	In	07	1

Notes:
1. All test modes are entered by first setting up the corresponding test address and then latching the address by bringing the /OE to V_H and then to V_{IL}, except for the margin read which requires /OE to be kept at V_H.

V_{VA} = Variable from V_{CC} to V_{PP}
V_{PP} = 12.5 V ± 0.5 V
V_H = 12.5 V ± 0. 5 V
V_{IH} = 3 V
V_{IL} = 0 V
XX = Irrelevant
I_{PP} during programming = 40 mA maximum
I_{CC} during programming, verify, or read = 40 mA maximum.

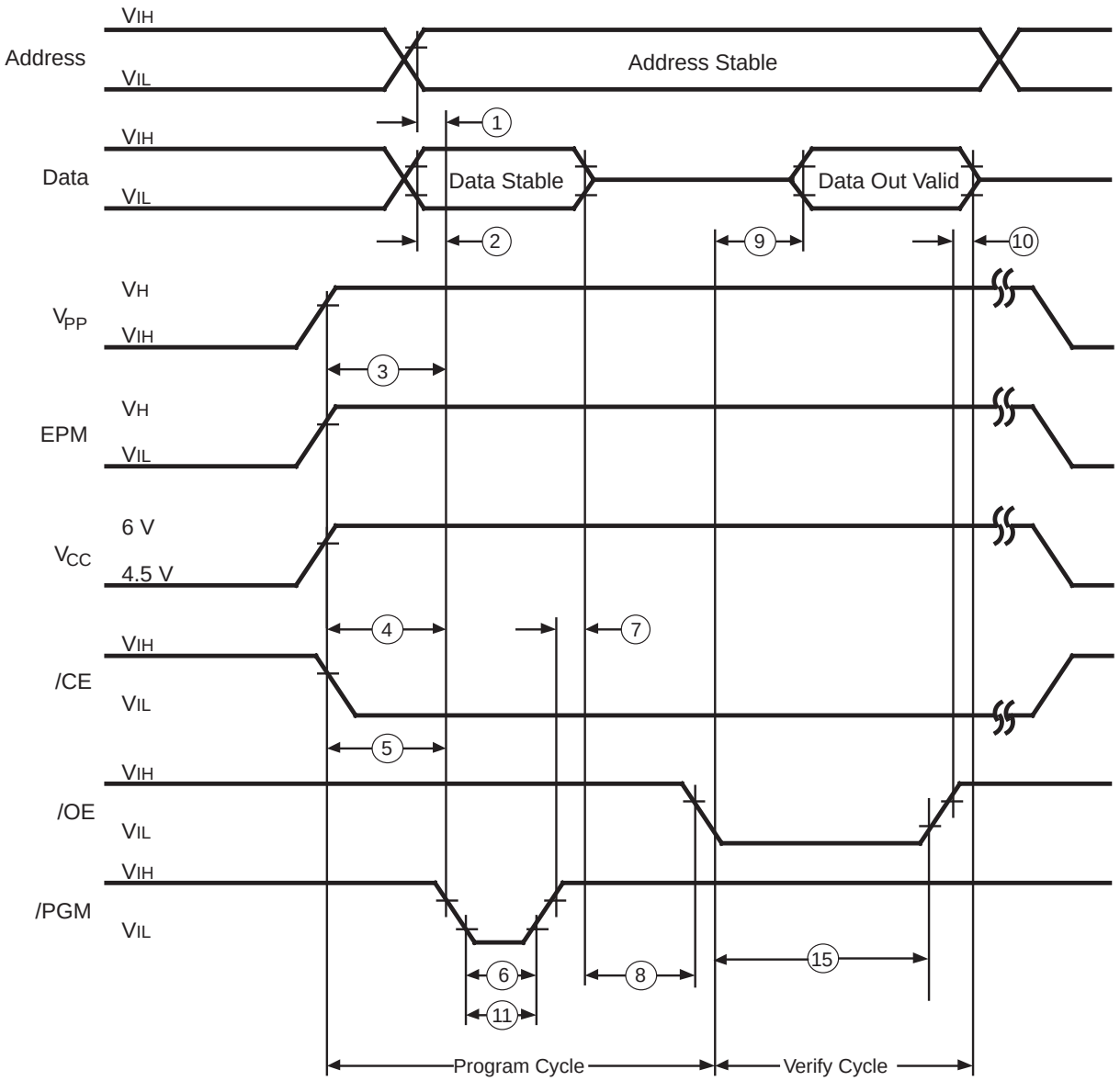


Figure 46. EPROM Program and Verify

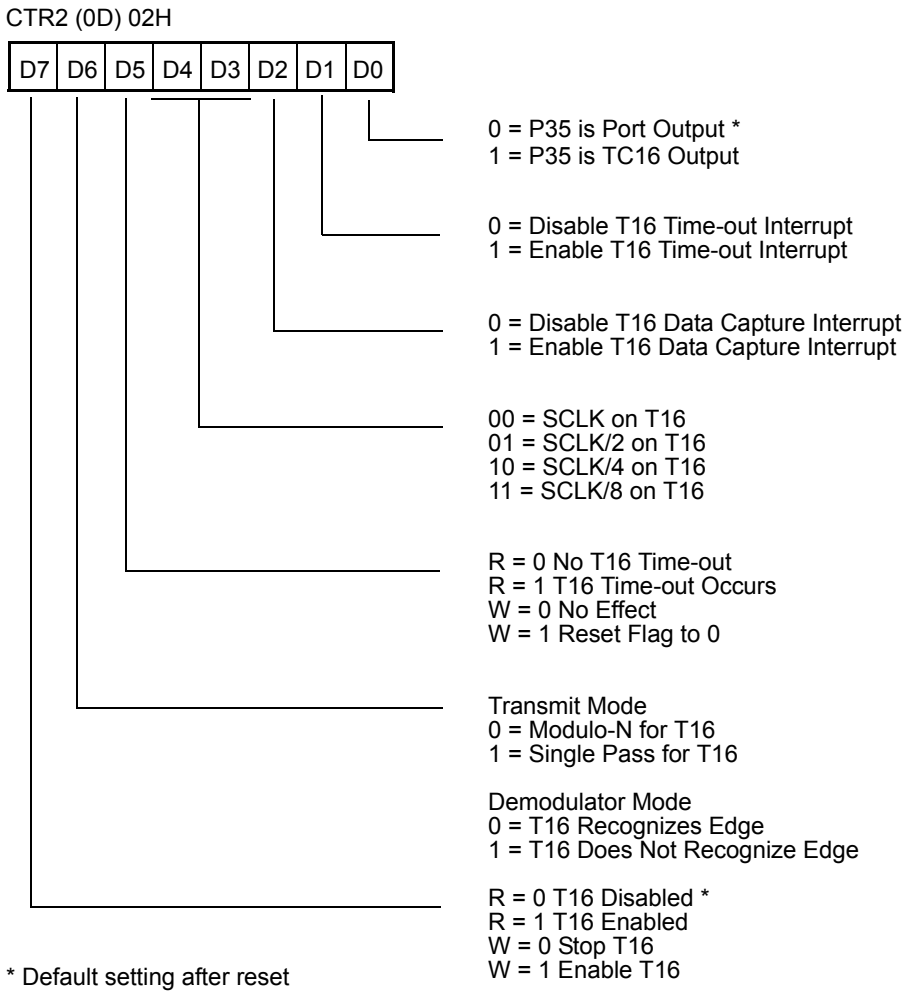


Figure 51. T16 Control Register—(0D) 2H: Read/Write Except Where Noted

Z8 Standard Control Register Diagrams

Figure 58 through Figure 66 show the Z8 standard control register diagrams.

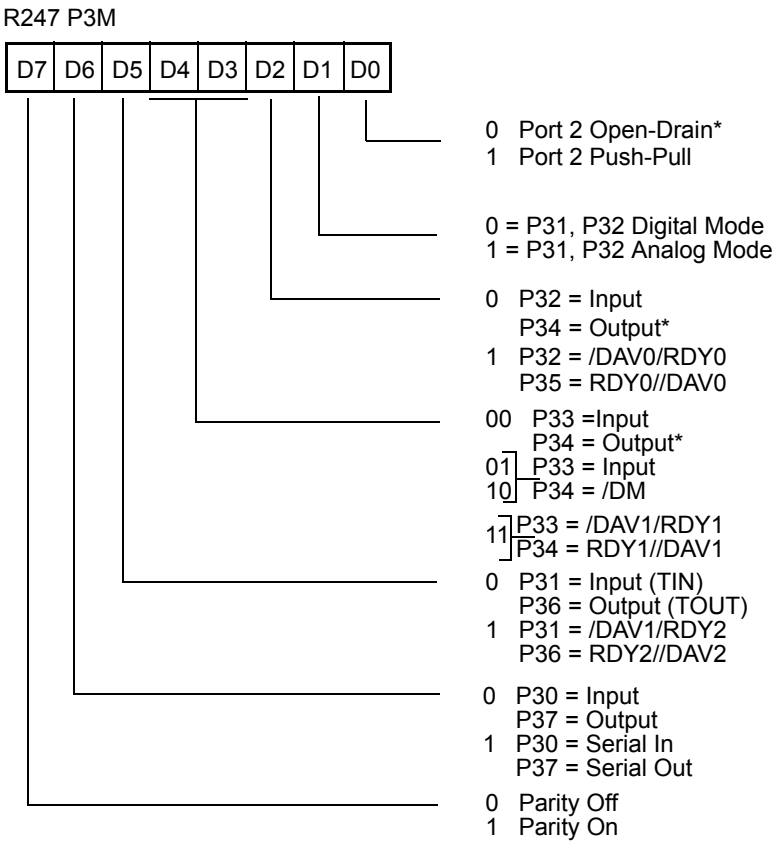


Figure 58. Port 3 Mode Register—F7H: Write Only

Figure 60. Interrupt Priority Registers—(0) F9H: Write Only

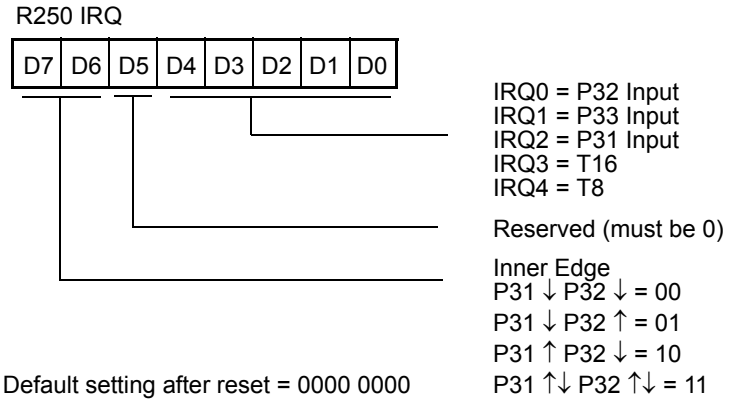


Figure 61. Interrupt Request Register—(0) FAH: Read/Write

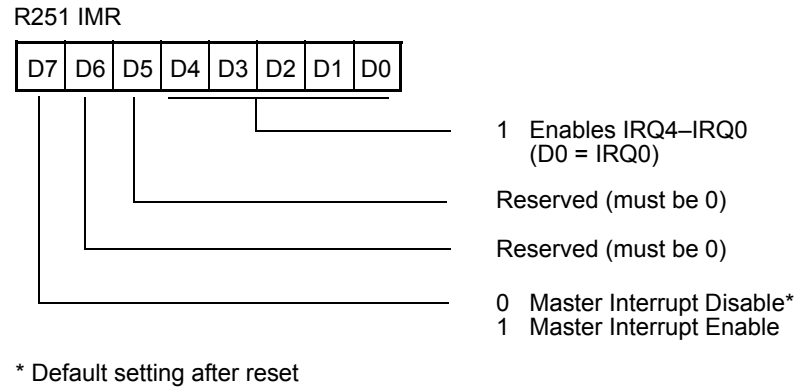


Figure 62. Interrupt Mask Register—(0) FBH: Read/Write

Figure 66. Stack Pointer Low—(0) FFH: Read/Write