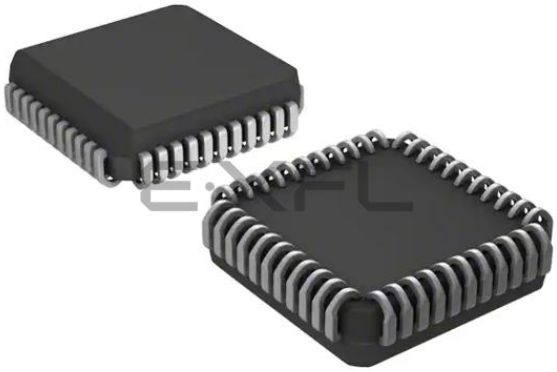

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	-
Peripherals	LVD, POR, WDT
Number of I/O	31
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e7316vsc

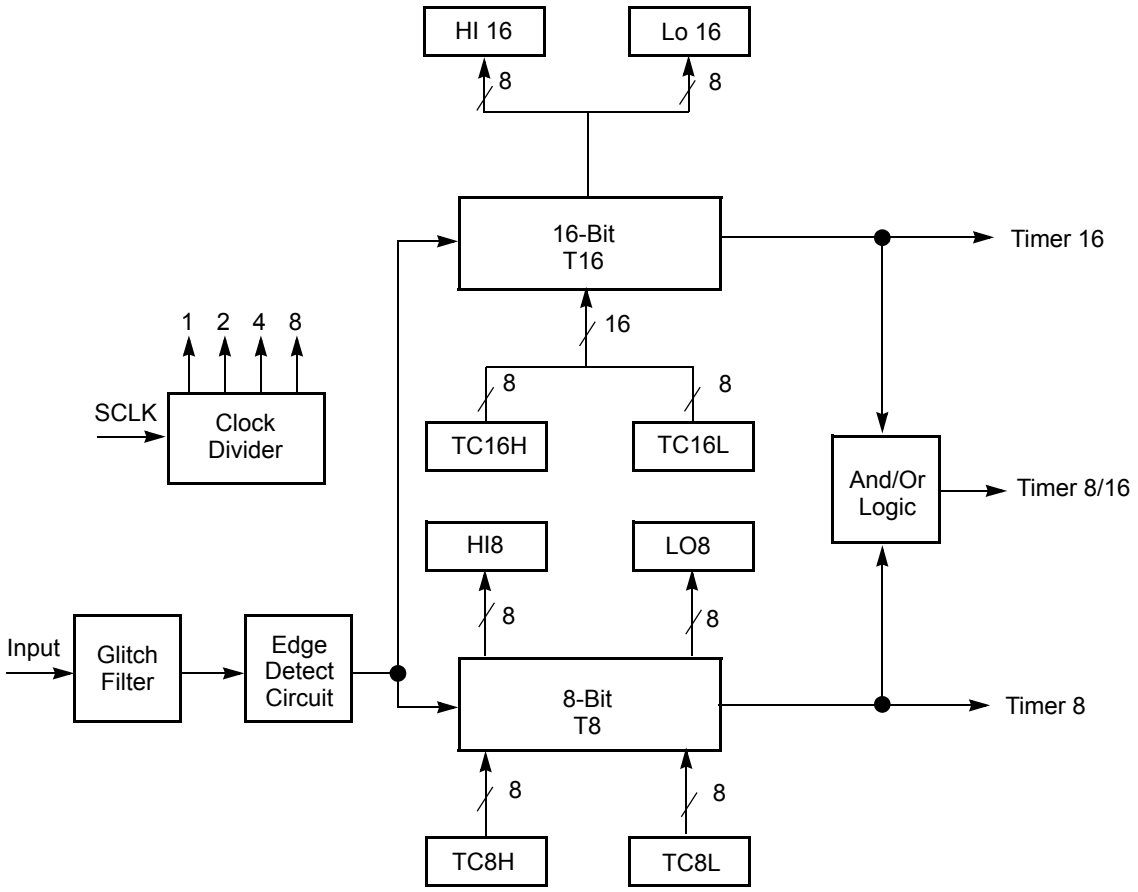


Figure 1. Z86E7X Counter/Timer Block Diagram

Power connections follow the conventions listed in Table 2.

Table 2. Power Connections

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

Figure 2 displays the functional block diagram.

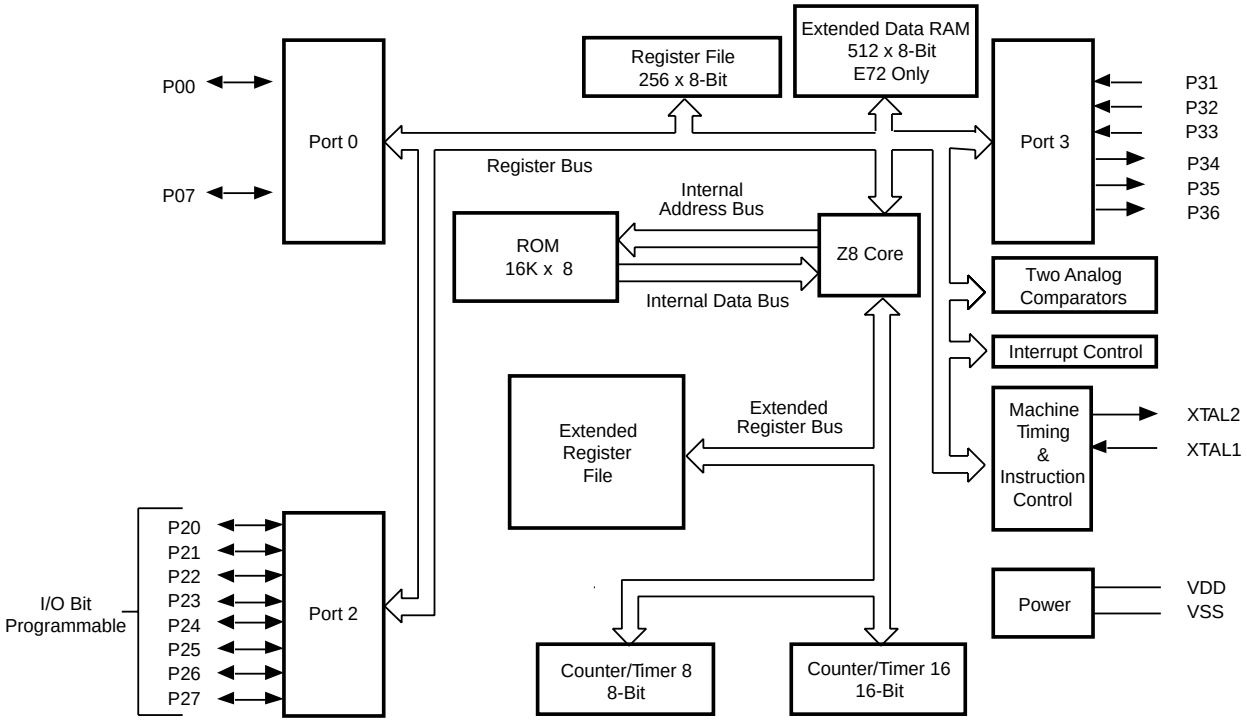


Figure 2. Z86E7X Functional Block Diagram

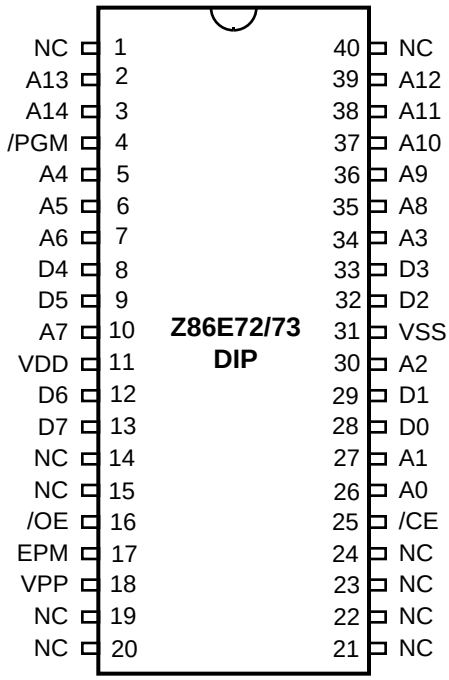


Figure 4. 40-Pin DIP Pin Assignments (EPROM Mode)

Figure 5 on page 7 shows the pin assignments for the standard mode of the 44-pin plastic leaded chip carrier (PLCC). Figure 6 on page 7 displays the pin assignments for the EPROM mode of the 44-pin PLCC.

Functional Description

The Z86E72/73 microcontrollers incorporate special functions to enhance the Z8's functionality in consumer and battery-operated applications.

Reset

The device is reset in one of the following conditions:

- Power-On Reset
- Watch-Dog Timer
- Stop-Mode Recovery Source
- Low Voltage Detection
- External Reset

Program Memory

The Z86E72/73 microcontrollers address up to 16K/32 KB of internal program memory, with the remainder being external memory (Figure 20). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain five 16-bit vectors that correspond to the five available interrupts. Addresses of 16K/32K consist of on-chip OTP. At addresses 16K or 32K and greater, the Z86E72/73 microcontrollers execute external program memory fetches (see “External Memory” on page 38).

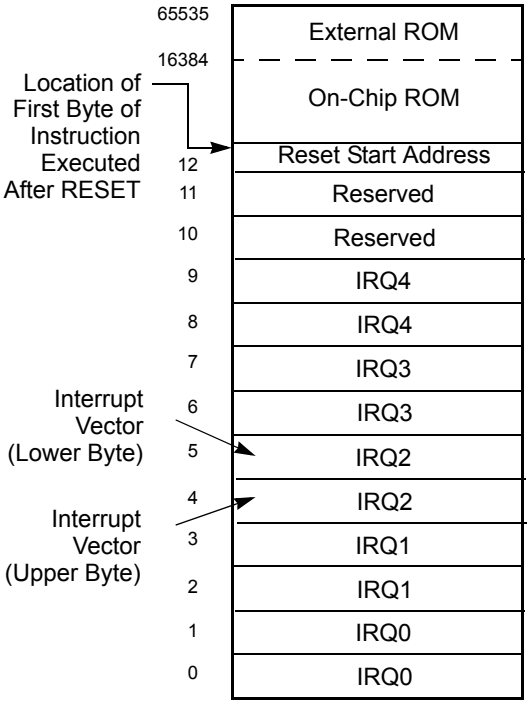


Figure 20. Program Memory Map

RAM

The Z86E72 has a 768-byte RAM; 256 bytes make up the register file. The remaining 512 bytes make up the Extended Data RAM. The Z86E73 has just the 256 bytes of the register file.

Extended Data RAM

The Extended Data RAM of the Z86E72 occupies the address range FE00H–FFFFH (512 bytes). This range of addresses FD00H–FFFFH cannot be used to directly read from or write to external memory. Accessing the Extended Data RAM is accomplished by using LDE or LDEI instructions. Port 1 and Port 0 are free to be set as I/O or ADDR/DATA modes; expect high-impedance when accessing Extended Data RAM. In addition, if the external memory uses the same address range of the Extended Data RAM, it can be used as the External Stack only.

Exercise caution when using extended data RAM (not Z8 RAM) on the Z86E72 OTP microcontroller. Extended RAM spaces FF0C–FF0F, FF10, FE0C–FE0F, and FE10 are reserved. Do not use these extended RAM locations.

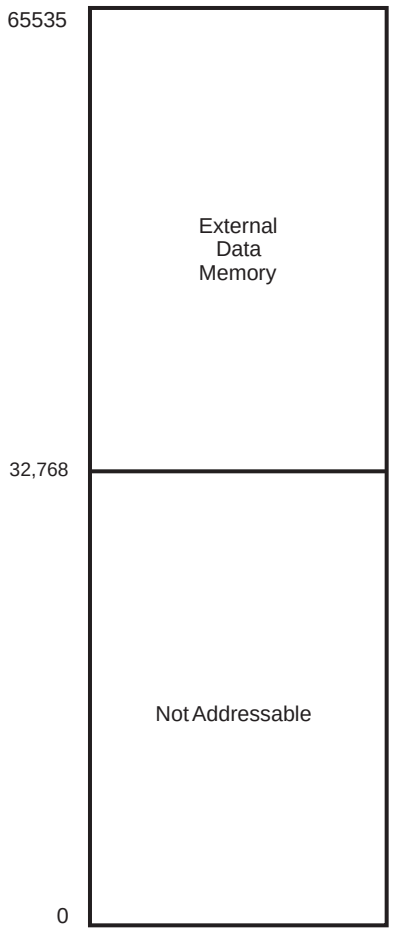


Figure 21. External Memory Map

Expanded Register File

The register file has been expanded to allow for additional system control registers and for mapping of additional peripheral devices into the register address area. The Z8 register address space R0 through R15 has been implemented as 16 banks of 16 registers per bank. These register groups are known as the Expanded Register File (ERF).

Bits 7–4 of register RP select the working register group. Bits 3–0 of register RP select the expanded register file bank.

Note: The expanded register bank is also referred to as the expanded register group (see Figure 22).

The upper nibble of the register pointer (Figure 23 on page 42) selects which working register group of 16 bytes in the register file, out of the possible 256, is accessed. The lower nibble selects the expanded register file bank and, in the case of the Z86E7X family, banks 0, F, and D are implemented. A 0h in the lower nibble allows the normal register file (bank 0) to be addressed, but any other value from 1h to Fh exchanges the lower 16 registers to an expanded register bank.

For example, Z86E73 (see Figure 22):

```
R253 RP = 00H
     R0 = Port0
     R1 = Port1
     R2 = Port2
     R3 = Port3
```

But if:

```
R253 RP = 0DH
     R0 = CTRL0
     R1 = CTRL1
     R2 = CTRL2
     R3 = Reserved
```

The counter/timers are mapped into ERF group D. Access is easily done using the following example:

```
LD          RP,#0Dh     ; Select ERF D for access and register
                        ; Bank 0 as the working register group.
LD          R0,#xx      ; access CTRL0
LD          1,#xx       ; access CTRL1
LD          RP,#7Dh     ; Select expanded register group (ERF)
                        ; group D for access and register
                        ; Bank 7 as the working register bank.
LD          R1,2        ; CTRL2→register 71H
```

HI16(D)09h Register

This register (Table 16) holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the MS-Byte of the data.

Table 16. HI16(D)09h Register

Field	Bit Position	Value	Description
T16_Capture_HI	76543210	R/W	Captured Data No Effect

L016(D)08h Register

This register (Table 17) holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the LS-Byte of the data.

Table 17. LO16(D)08h Register

Field	Bit Position	Value	Description
T16_Capture_LO	76543210	R/W	Captured Data No Effect

TC16H(D)07h Register

Table 18 describes the Counter/Timer2 MS-Byte Hold Register.

Table 18. TC16H(D)07h Register

Field	Bit Position	Value	Description
T16_Data_HI	76543210	R/W	Data

TC16L(D)06h Register

Table 19 describes the Counter/Timer2 LS-Byte Hold Register.

Table 19. TC16L(D)06h Register

Field	Bit Position	Value	Description
T16_Data_LO	76543210	R/W	Data

Table 22. CTR0(D)00h Register (Continued)

Field	Bit Position		Value	Description
Counter_INT_Mask	------1-	R/W	0 1	Disable Time-Out Int. Enable Time-Out Int.
P34_Out	-------0	R/W	0* 1	P34 as Port Output T8 Output on P34

Note: *Indicates the value upon Power-On Reset

T8 Enable

This field enables T8 when set (written) to 1.

Single/Modulo-N

When set to 0 (modulo-n), the counter reloads the initial value when the terminal count is reached. When set to 1 (single pass), the counter stops when the terminal count is reached.

Time-Out

This bit is set when T8 times out (terminal count reached). To reset this bit, a 1 must be written to this location.

Notes: This is the only way to reset this status condition; therefore, you must reset this bit before using/enabling the counter/timers.

Care must be taken when using the OR or AND commands to manipulate CTR0, bit 5 and CTR1, bits 0 and 1 (demodulation mode). These instructions use a Read-Modify-Write sequence in which the current status from the CTR0 and CTR1 registers is ORed or ANDed with the designated value and then written back into the registers. For example, when the status of bit 5 is 1, a reset condition occurs.

T8 Clock

This bit defines the frequency of the input signal to T8.

Capture_INT_Mask

Set this bit to allow interrupt when data is captured into either LO8 or HI8 upon a positive or negative edge detection in demodulation mode.

Table 23. CTR1(D)01h Register (Continued)

Field	Bit Position		Value	Description
Initial_T8_Out/Rising_Edge	------1-			Transmit Mode
		R/W	0	T8_OUT is 0 Initially
			1	T8_OUT is 1 Initially
				Demodulation Mode
		R	0	No Rising Edge
			1	Rising Edge Detected
		W	0	No Effect
			1	Reset Flag to 0
Initial_T16_Out/Falling _Edge	-------0			Transmit Mode
		R/W	0	T16_OUT is 0 Initially
			1	T16_OUT is 1 Initially
				Demodulation Mode
		R	0	No Falling Edge
			1	Falling Edge Detected
		W	0	No Effect
			1	Reset Flag to 0

Note: * Indicates the value upon Power-On Reset.

Mode

If it is 0, the counter/timers are in the transmit mode; otherwise, they are in the demodulation mode.

P36_Out/Demodulator_Input

In transmit mode, this bit defines whether P36 is used as a normal output pin or the combined output of T8 and T16.

In demodulation mode, this bit defines whether the input signal to the counter/timers is from P20 or P31.

T8/T16_Logic/Edge _Detect

In transmit mode, this field defines how the outputs of T8 and T16 are combined (AND, OR, NOR, NAND).

In demodulation mode, this field defines which edge needs to be detected by the edge detector.

Transmit_Submode/Glitch Filter

In transmit mode, this field defines whether T8 and T16 are in the “Ping-Pong” mode or in independent normal operation mode. Setting this field to “Normal

CTR2(D)02h Register

Table 24 describes the Counter/Timer16 Control Register.

Table 24. CTR2(D)02h Register

Field	Bit Position		Value	Description
T16_Enable	7-------	R	0*	Counter Disabled
			1	Counter Enabled
		W	0	Stop Counter
			1	Enable Counter
Submode/Modulo-N	-6------	R/W		Transmit Mode
			0	Modulo-N
			1	Single Pass
				Demodulation Mode
			0	T16 Recognizes Edge
			1	T16 Does Not Recognize Edge
Time_Out	--5-----	R	0	No Counter Time-Out
			1	Counter Time-Out Occurred
		W	0	No Effect
			1	Reset Flag to 0
T16 _Clock	---43---	R/W	00	SCLK
			01	SCLK/2
			10	SCLK/4
			11	SCLK/8
Capture_INT_Mask	-----2--	R/W	0	Disable Data Capture Int.
			1	Enable Data Capture Int.
Counter_INT_Mask	------1-	R/W	0	Disable Time-Out Int.
			1	Enable Time-Out Int.
P35_Out	-------0	R/W	0*	P35 as Port Output
			1	T16 Output on P35

Note: * Indicates the value upon Power-On Reset.

T16_Enable

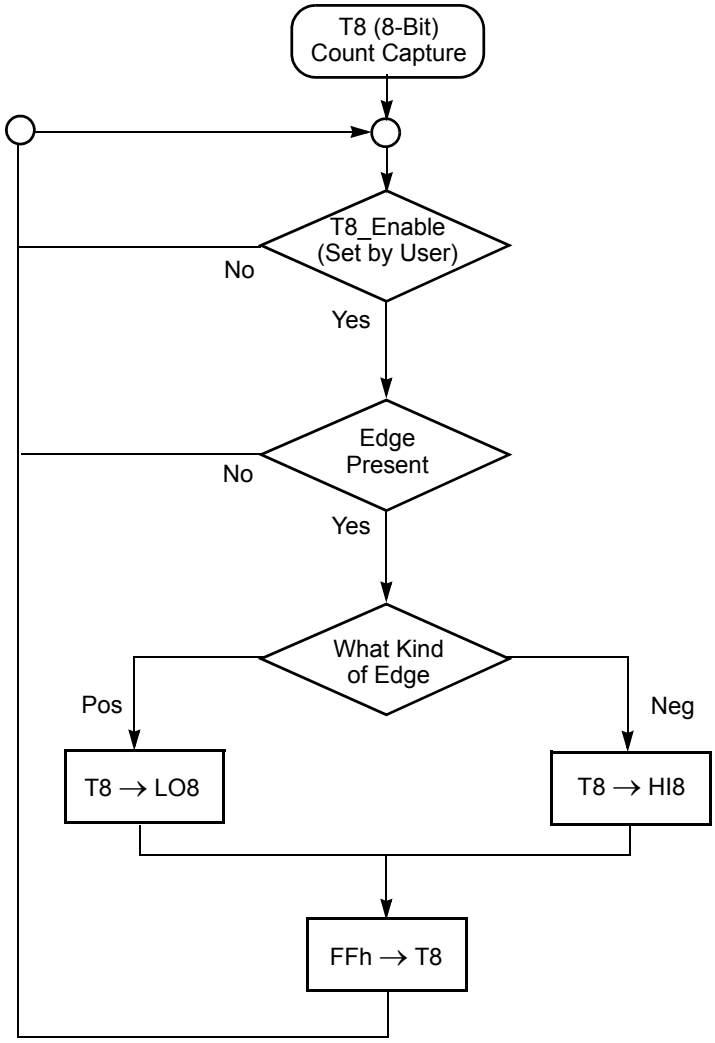
This field enables T16 when set to 1.

Single/Modulo-N

In transmit mode, when set to 0, the counter reloads the initial value when terminal count is reached. When set to 1, the counter stops when the terminal count is reached.

T8 Demodulation Mode

You need to program TC8L and TC8H to FFh. After T8 is enabled, when the first edge (rising, falling, or both depending on CTR1 D5, D4) is detected, it starts to count down. When a subsequent edge (rising, falling, or both depending on CTR1 D5, D4) is detected during counting, the current value of T8 is one's complemented and put into one of the capture registers. If it is a positive edge, data is put into LO8; if negative edge, HI8. One of the edge-detect status bits (CTR1 D1, D0) is set, and an interrupt can be generated if enabled (CTR0 D2). Meanwhile, T8 is loaded with FFh and starts counting again. When T8 reaches 0, the time-out status bit (CTR0 D5) is set, an interrupt can be generated if enabled (CTR0 D1), and T8 continues counting from FFh (see Figure 30 and Figure 31).



Sixteen-Bit Counter/Timer Circuits

Figure 32 shows the 16-bit counter/timer circuits.

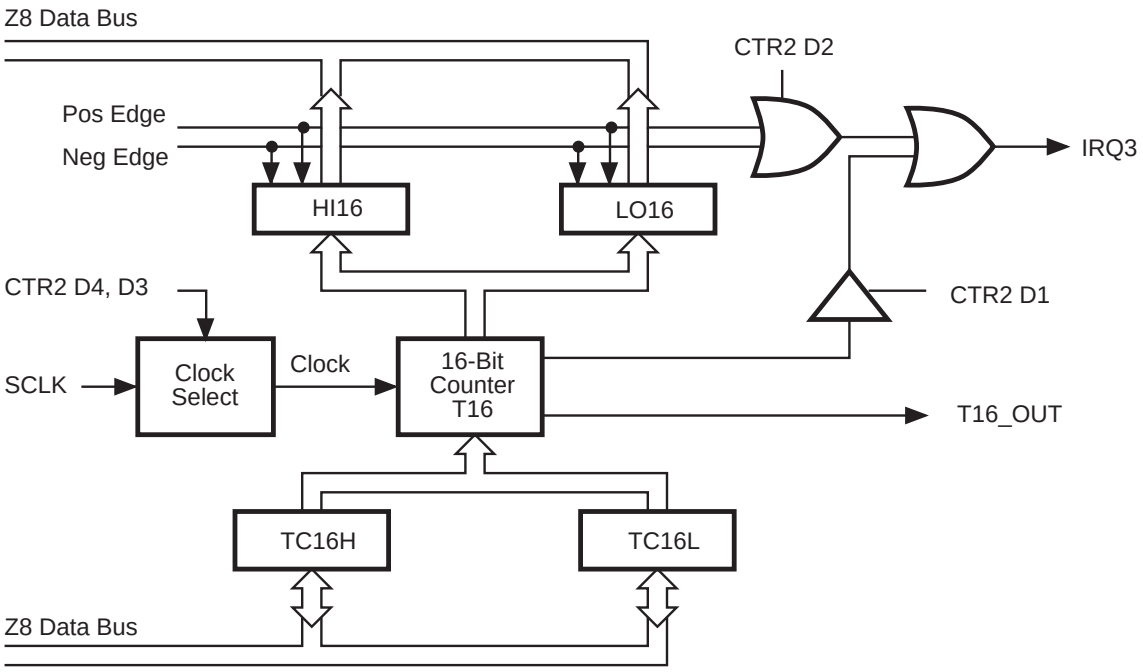


Figure 32. Sixteen-Bit Counter/Timer Circuits

T16 Transmit Mode

In Normal or Ping-Pong Mode, the output of T16, when not enabled, is dependent on CTR1, D0. If it is a 0, T16_OUT is a 1; if it is a 1, T16_OUT is 0. You can force the output of T16 to either a 0 or 1 whether it is enabled or not by programming CTR1 D3, D2 to a 10 or 11.

When T16 is enabled, TC16H * 256 + TC16L is loaded, and T16_OUT is switched to its initial value (CTR1 D0). When T16 counts down to 0, T16_OUT is toggled (in Normal or Ping-Pong Mode), an interrupt is generated if enabled (CTR2 D1), and a status bit (CTR2 D5) is set.

Note: Global interrupts override this function as described in "Interrupts" on page 62.

If T16 is in Single-Pass Mode, it is stopped at this point (see Figure 33). If it is in Modulo-N Mode, it is loaded with TC16H * 256 + TC16L, and the counting continues (see Figure 34).

Starting Ping-Pong Mode

First, make sure both counter/timers are not running. Then set T8 into Single-Pass Mode (CTR0 D6), set T16 into Single-Pass Mode (CTR2 D6), and set Ping-Pong Mode (CTR1 D2, D3). These instructions do not have to be in any particular order. Finally, start Ping-Pong Mode by enabling either T8 (CTR0 D7) or T16 (CTR2 D7).

During Ping-Pong Mode

The enable bits of T8 and T16 (CTR0 D7, CTR2 D7) are alternately set and cleared by hardware. The time-out bits (CTR0 D5, CTR2 D5) are set every time the counter/timers reach the terminal count.

Output Circuit

Figure 36 shows the output circuit.

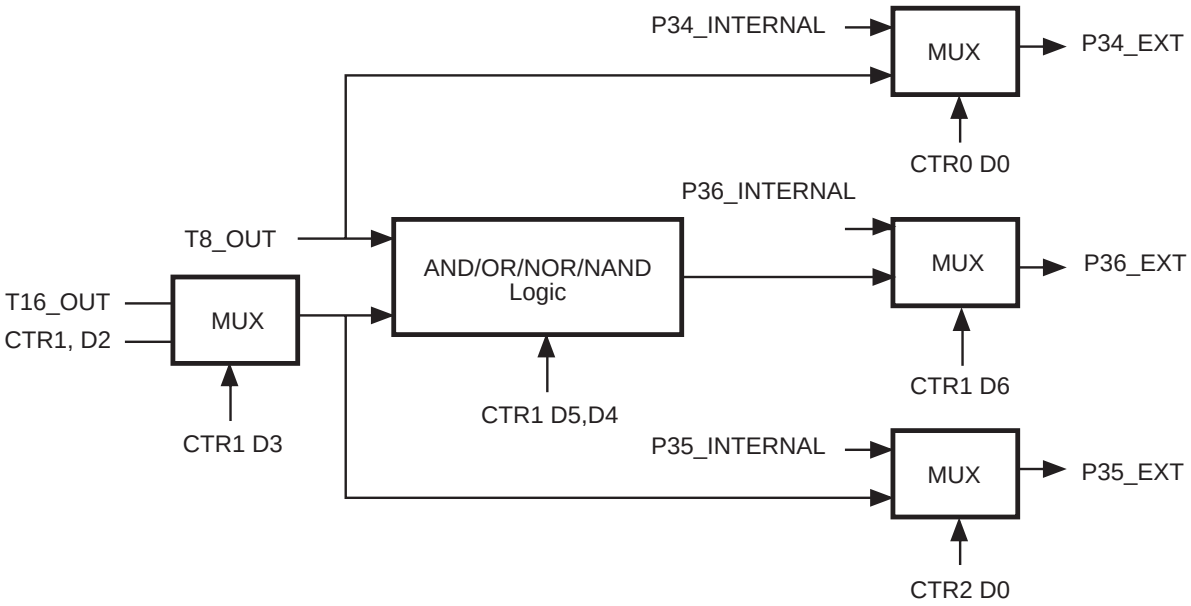


Figure 36. Output Circuit

Interrupts

The Z86E7X has five different interrupts. The interrupts are maskable and prioritized, as shown in Figure 37. The five sources are divided as follows: three sources are claimed by Port 3 lines P33–P31 and the remaining two by the counter/timers (see Table 26). The Interrupt Mask Register globally or individually enables or disables the five interrupt requests.

Stop-Mode Recovery Register 2 (SMR2)

This register (see Figure 42) determines the mode of STOP Mode recovery for SMR2.

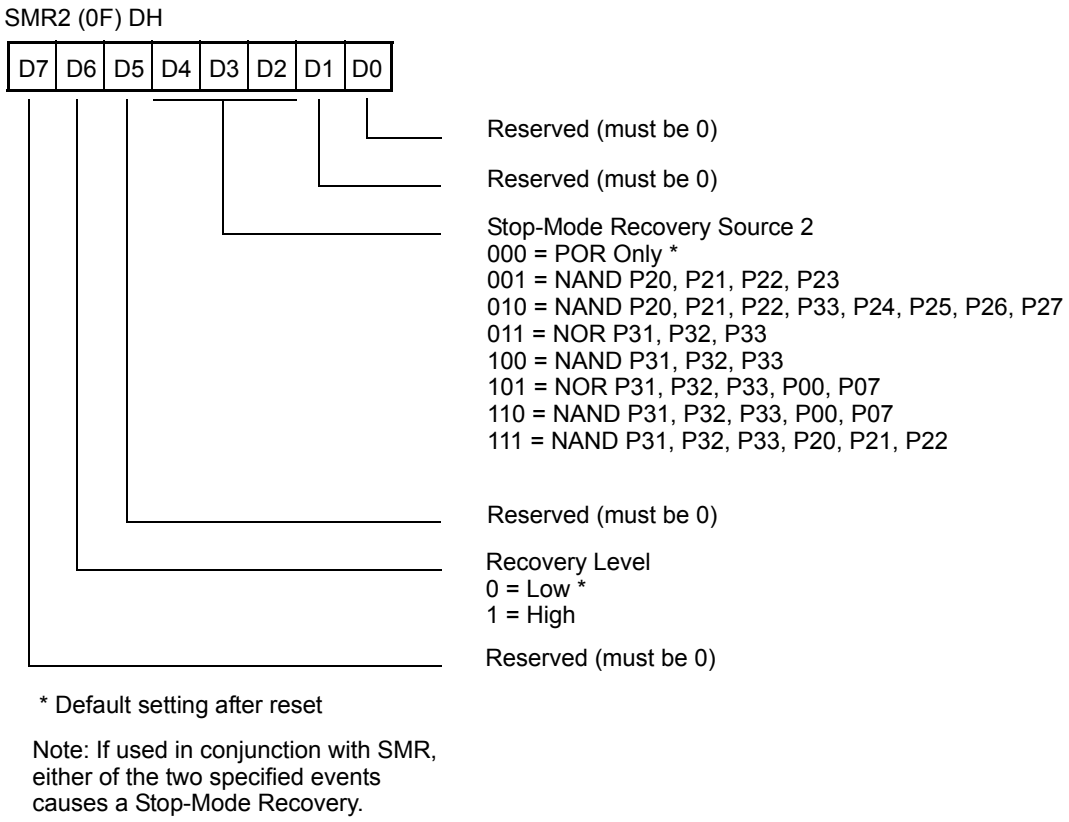


Figure 42. Stop-Mode Recovery Register 2—(0F) DH: D2–D4, D6 Write Only

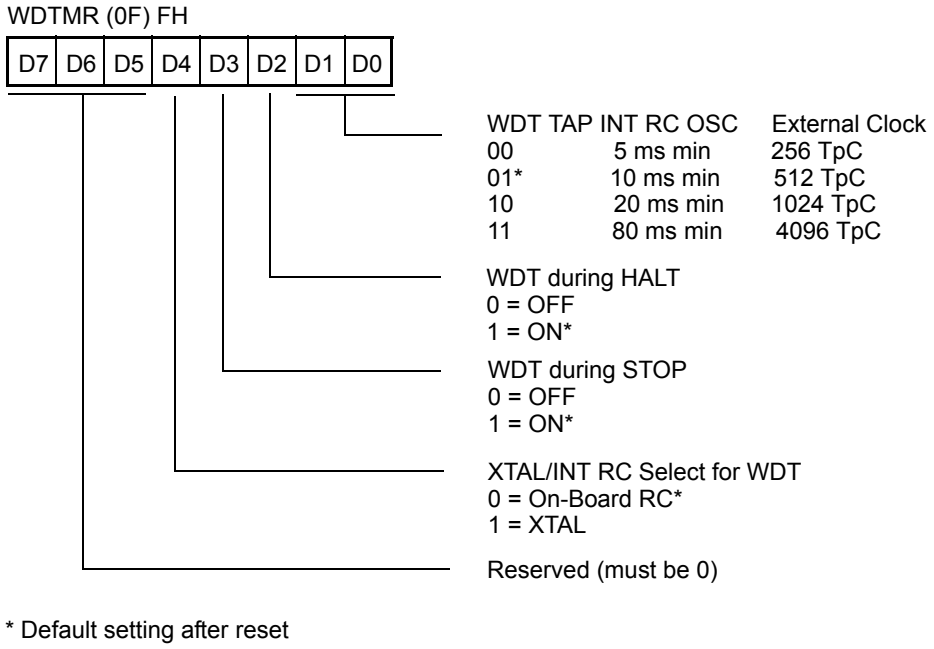
If SMR2 is used in conjunction with SMR, either of the specified events causes a Stop-Mode Recovery.

Note: Port pins configured as outputs are ignored as a SMR or SMR2 recovery source. For example, if the NAND of P23–P20 is selected as the recovery source and P20 is configured as an output, the remaining SMR pins (P23–P21) form the NAND equation.

Watch-Dog Timer Mode Register (WDTMR)

The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT must initially be enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT circuit is driven by an on-board RC oscillator or external oscillator from the XTAL1 pin. The WDT instruction affects the Zero (Z), Sign (S), and Overflow (V) flags.

The POR clock source is selected with bit 4 of the WDT register. Bit 0 and 1 control a tap circuit that determines the time-out period. Bit 2 determines whether the WDT is active during HALT, and Bit 3 determines WDT activity during STOP. Bits 5 through 7 are reserved. See Figure 43.



* Default setting after reset

Figure 43. Watch-Dog Timer Mode Register—Write Only

This register is accessible only during the first 60 processor cycles (SCLK) from the execution of the first instruction after Power-On-Reset, Watch-Dog Reset, or a Stop-Mode Recovery (Figure 40 on page 68). After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in Bank F of the Expanded Register Group at address location 0FH. It is organized as shown in Figure 43.

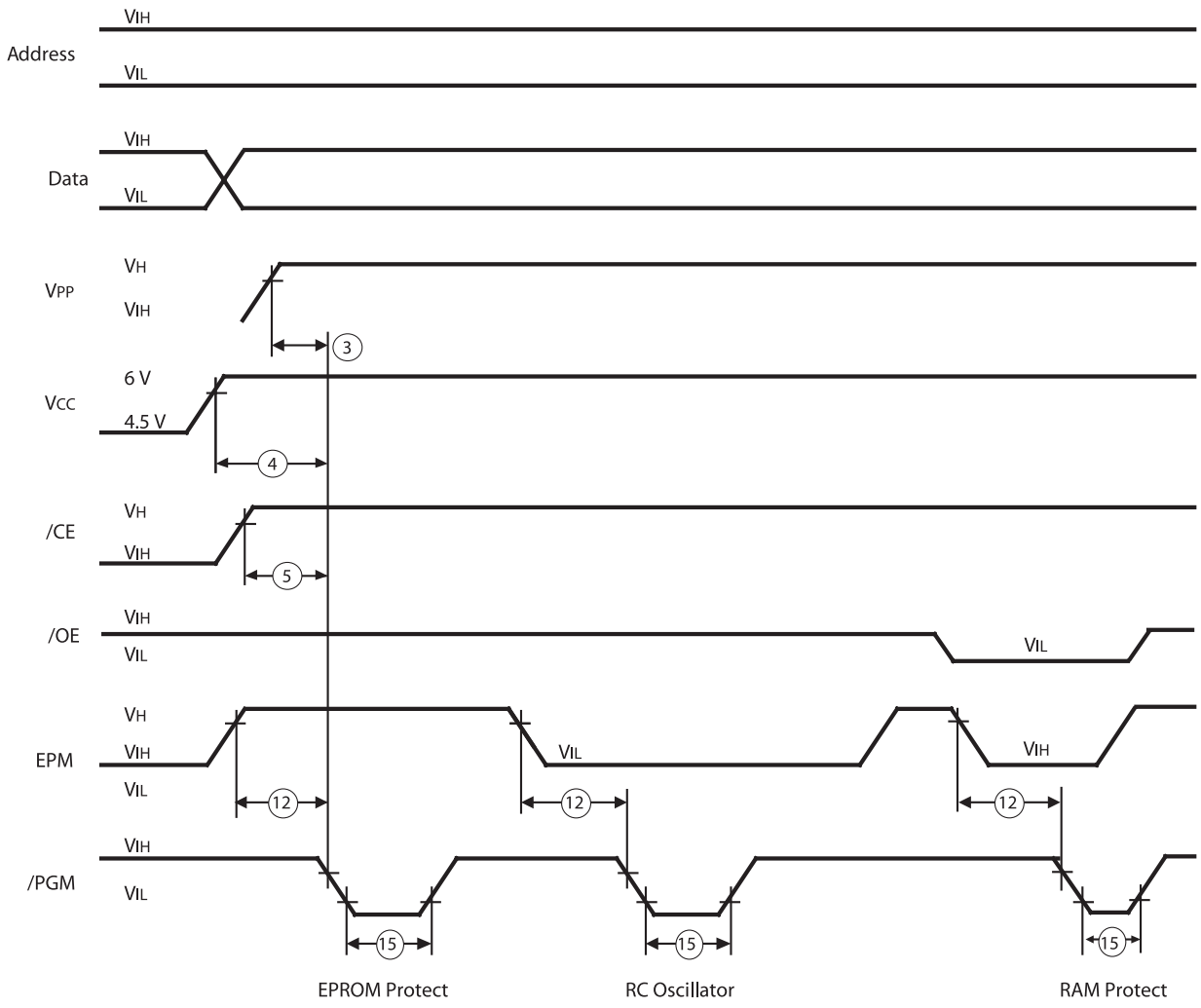


Figure 47. Programming EPROM, RAM Protect, and 16K Size Selection

Figure 48 shows the programming flowchart.

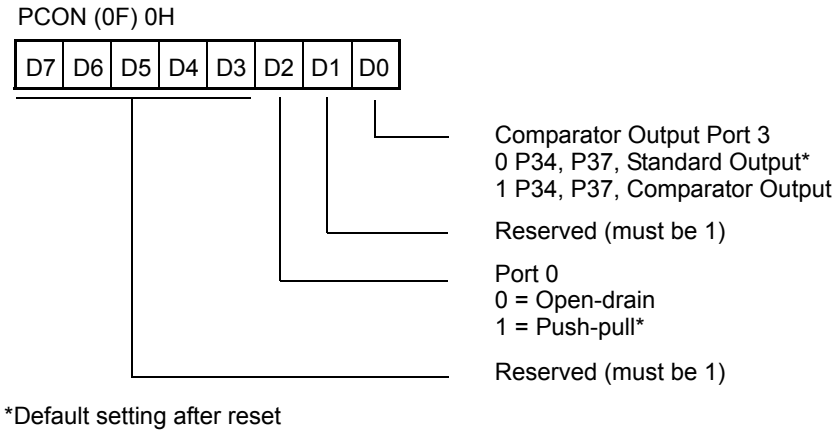


Figure 56. Port Configuration Register (PCON)—(0F) 0H: Write Only

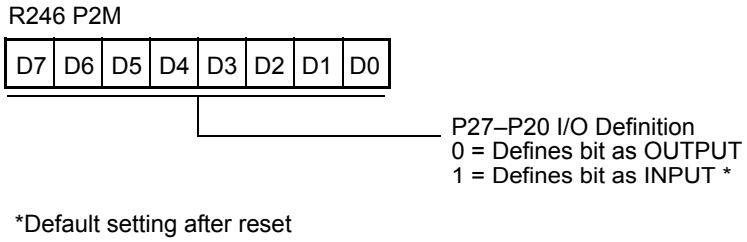


Figure 57. Port 2 Mode Register—F6H: Write Only

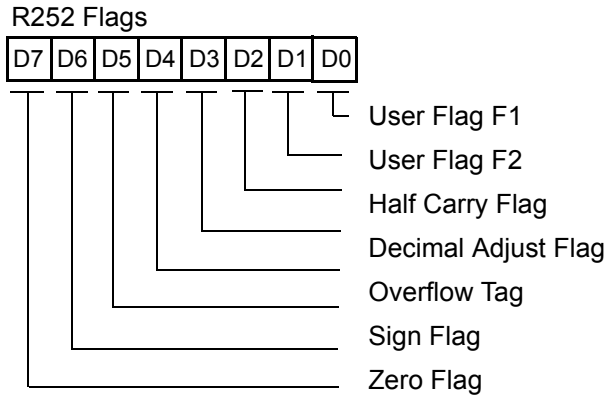


Figure 63. Flag Register—(0) FCH: Read/Write

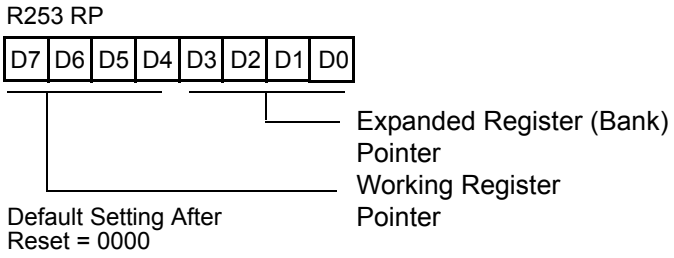


Figure 64. Register Pointer—(0) FDH: Read/Write

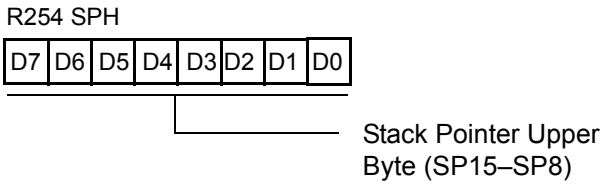
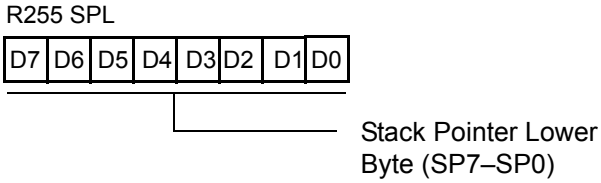
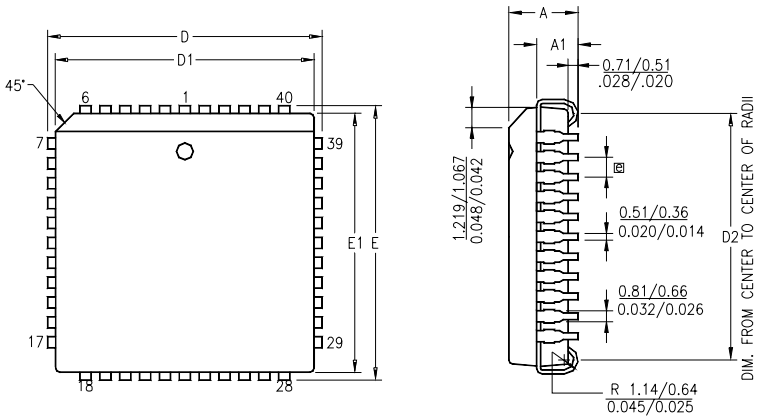


Figure 65. Stack Pointer High—(0) FEH: Read/Write





SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.27	4.57	0.168	0.180
A1	2.41	2.92	0.095	0.115
D/E	17.40	17.65	0.685	0.695
D1/E1	16.51	16.66	0.650	0.656
D2	15.24	16.00	0.600	0.630
e	1.27 BSC		0.050 BSC	

NOTES:
1. CONTROLLING DIMENSION : INCH
2. LEADS ARE COPLANAR WITHIN 0.004".
3. DIMENSION : MM
INCH

Figure 69. 44-Pin PLCC Package Diagram