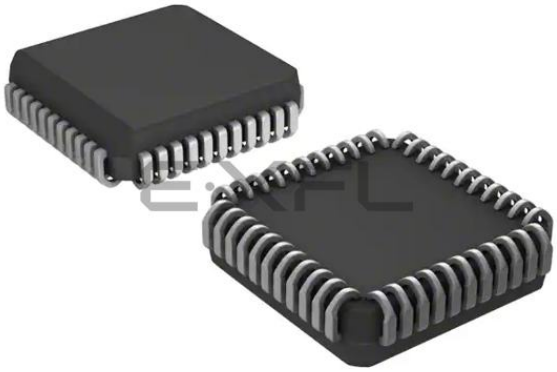

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	-
Peripherals	LVD, POR, WDT
Number of I/O	31
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e7316vsg

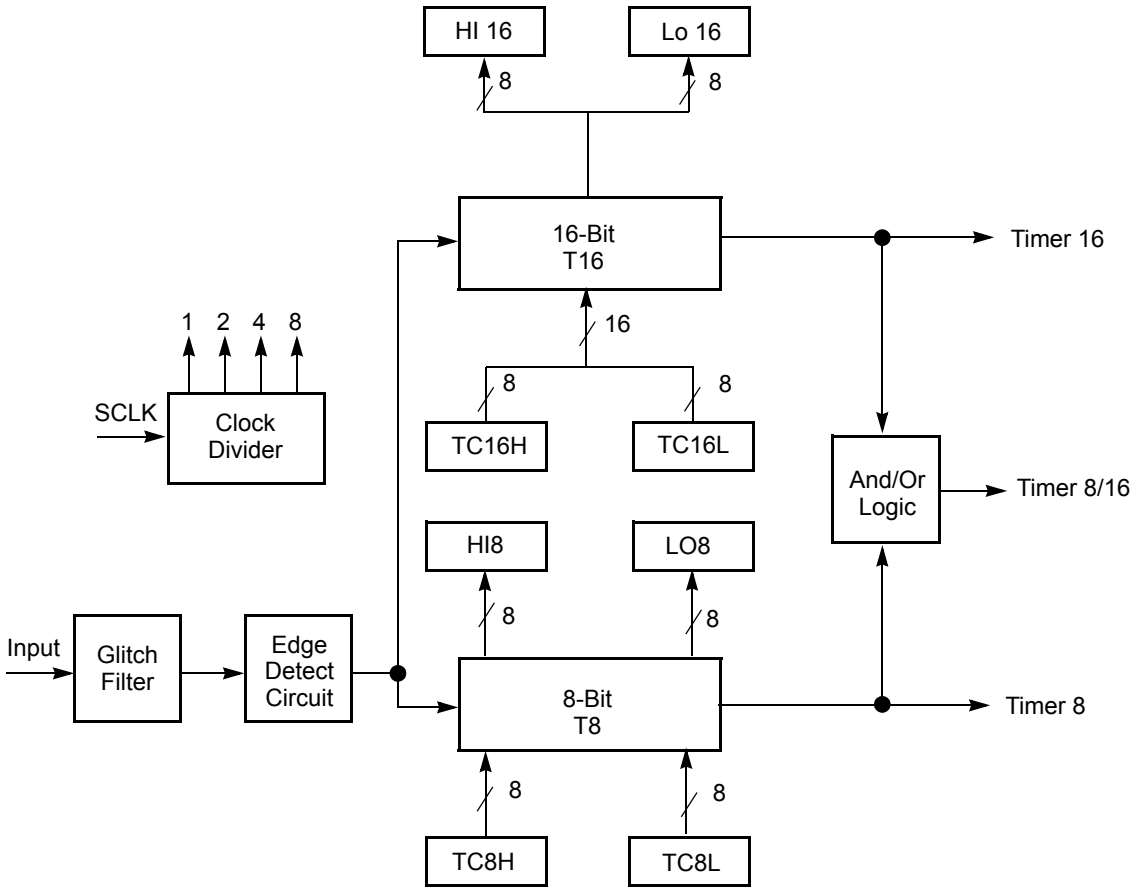


Figure 1. Z86E7X Counter/Timer Block Diagram

Power connections follow the conventions listed in Table 2.

Table 2. Power Connections

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

Figure 2 displays the functional block diagram.

Figure 7 displays the pin assignments for the standard mode of the 44-pin low-profile quad flat pack (LQFP). Figure 8 on page 9 shows the pin assignments for the EPROM mode of the 44-pin LQFP.

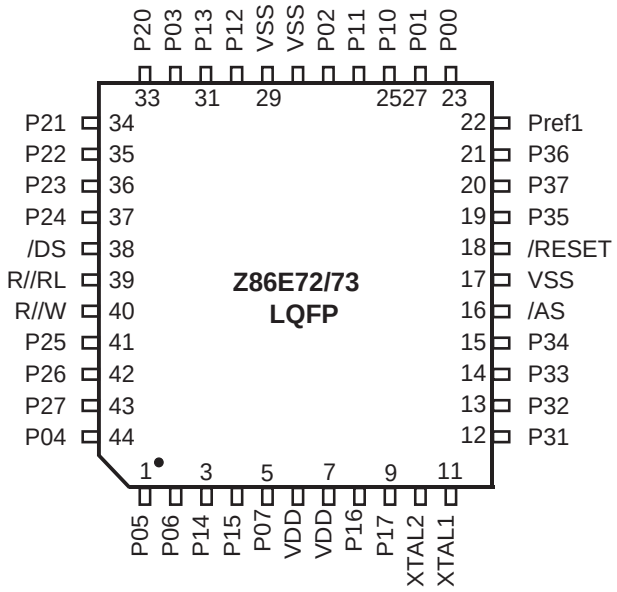


Figure 7. 44-Pin LQFP Pin Assignments (Standard Mode)

AC Characteristics

Figure 10 shows the external input/output (I/O) or memory read and write timing. Table 9 describes the I/O or memory read and write timing.

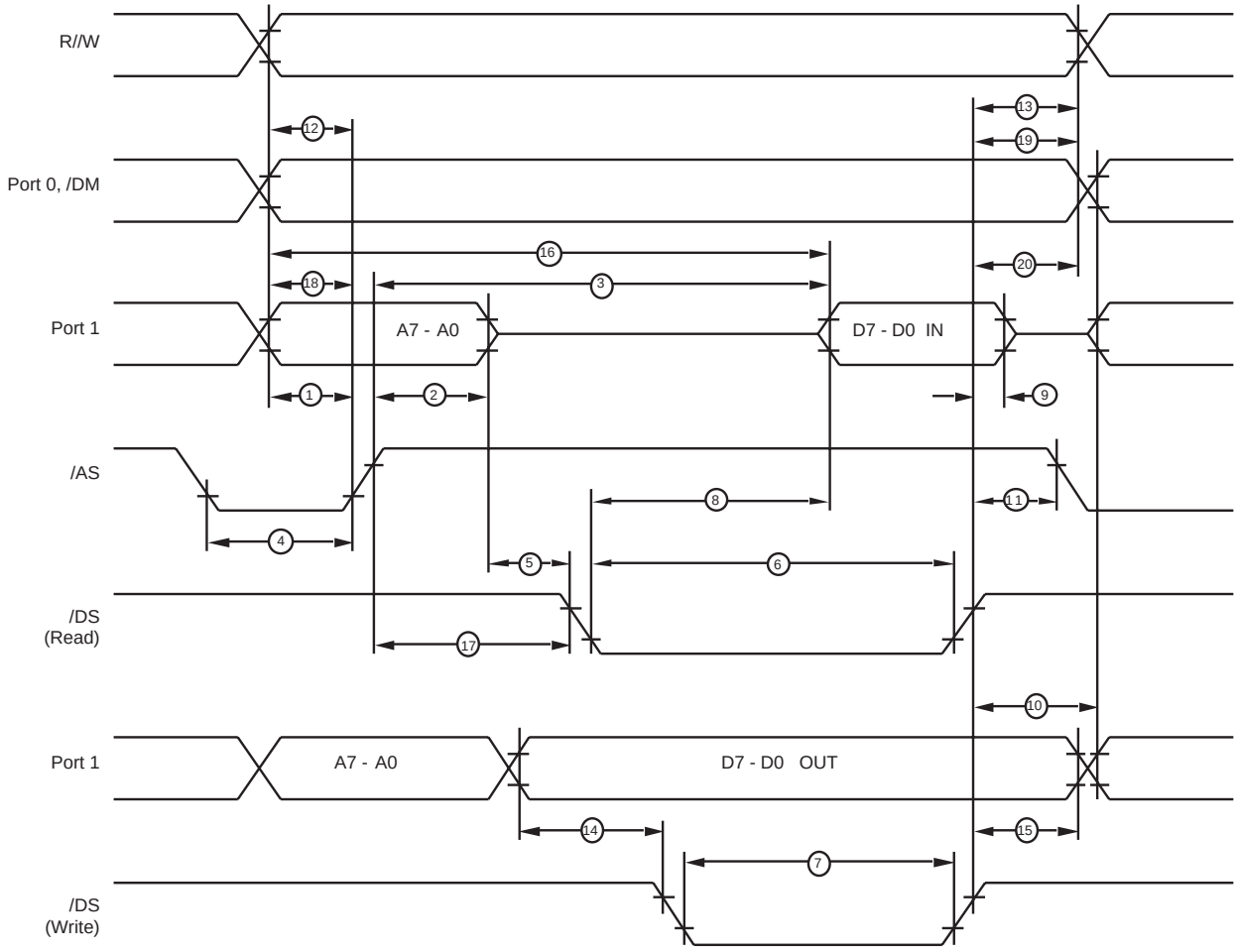


Figure 10. External I/O or Memory Read/Write Timing

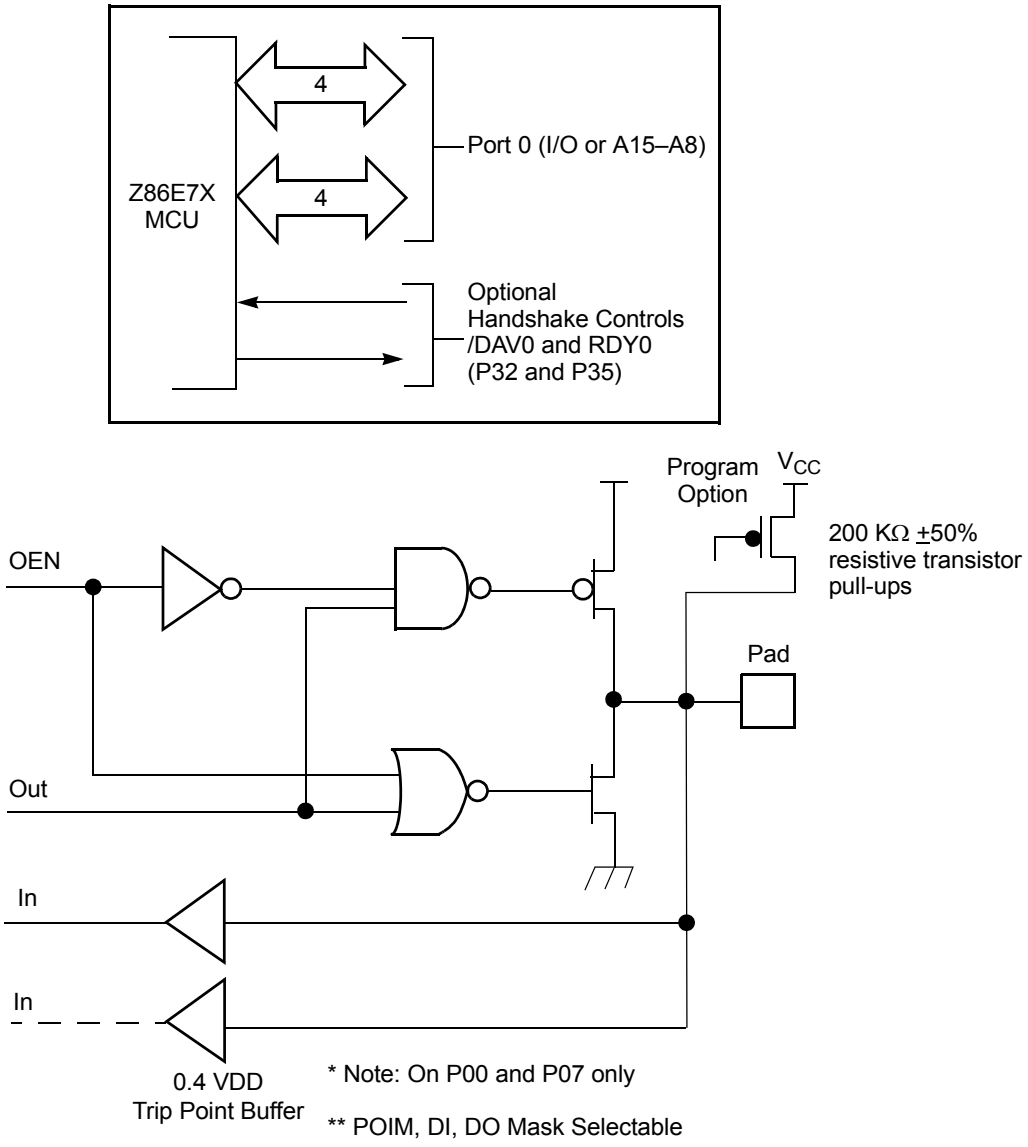


Figure 14. Port 0 Configuration

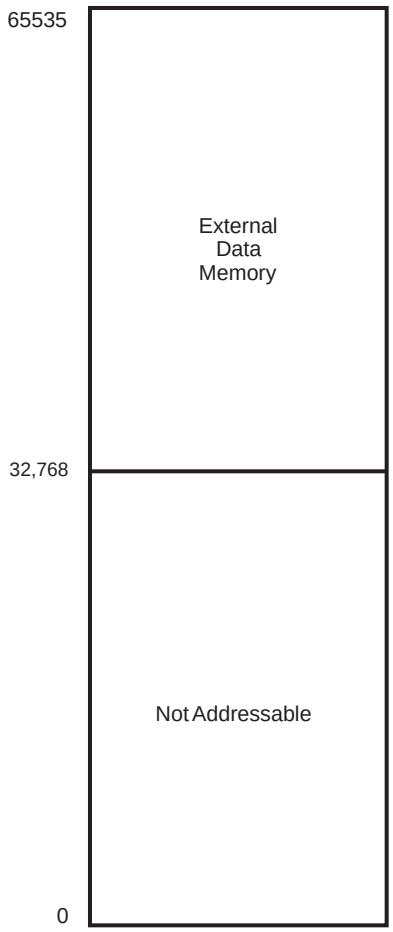


Figure 21. External Memory Map

Expanded Register File

The register file has been expanded to allow for additional system control registers and for mapping of additional peripheral devices into the register address area. The Z8 register address space R0 through R15 has been implemented as 16 banks of 16 registers per bank. These register groups are known as the Expanded Register File (ERF).

Bits 7–4 of register RP select the working register group. Bits 3–0 of register RP select the expanded register file bank.

Note: The expanded register bank is also referred to as the expanded register group (see Figure 22).

Counter_INT_Mask

Set this bit to allow interrupt when T8 has a time out.

P34_Out

This bit defines whether P34 is used as a normal output pin or the T8 output.

CTR1(D)01h Register

This register (Table 23) controls the functions in common with the T8 and T16.

Table 23. CTR1(D)01h Register

Field	Bit Position		Value	Description
Mode	7-------	R/W	0*	Transmit Mode
			1	Demodulation Mode
P36_Out/Demodulator_Input	-6------	R/W		Transmit Mode
			0*	Port Output
			1	T8/16 Output
				Demodulation Mode
			0	P31
			1	P20
T8/T16_Logic/Edge _Detect	--54----	R/W		Transmit Mode
			0 0	AND
			0 1	OR
			1 0	NOR
			1 1	NAND
				Demodulation Mode
			0 0	Falling Edge
			0 1	Rising Edge
			1 0	Both Edges
			1 1	Reserved
Transmit_Submode/Glitch_Filter	----32--	R/W		Transmit Mode
			0 0	Normal Operation
			0 1	Ping-Pong Mode
			1 0	T16_OUT = 0
			1 1	T16_OUT = 1
				Demodulation Mode
			0 0	No Filter
			0 1	4 SCLK Cycle
			1 0	8 SCLK Cycle
			1 1	16 SCLK Cycle

Table 23. CTR1(D)01h Register (Continued)

Field	Bit Position		Value	Description
Initial_T8_Out/Rising_Edge	------1-			Transmit Mode
		R/W	0	T8_OUT is 0 Initially
			1	T8_OUT is 1 Initially
				Demodulation Mode
		R	0	No Rising Edge
			1	Rising Edge Detected
		W	0	No Effect
			1	Reset Flag to 0
Initial_T16_Out/Falling _Edge	-------0			Transmit Mode
		R/W	0	T16_OUT is 0 Initially
			1	T16_OUT is 1 Initially
				Demodulation Mode
		R	0	No Falling Edge
			1	Falling Edge Detected
		W	0	No Effect
			1	Reset Flag to 0

Note: * Indicates the value upon Power-On Reset.

Mode

If it is 0, the counter/timers are in the transmit mode; otherwise, they are in the demodulation mode.

P36_Out/Demodulator_Input

In transmit mode, this bit defines whether P36 is used as a normal output pin or the combined output of T8 and T16.

In demodulation mode, this bit defines whether the input signal to the counter/timers is from P20 or P31.

T8/T16_Logic/Edge _Detect

In transmit mode, this field defines how the outputs of T8 and T16 are combined (AND, OR, NOR, NAND).

In demodulation mode, this field defines which edge needs to be detected by the edge detector.

Transmit_Submode/Glitch Filter

In transmit mode, this field defines whether T8 and T16 are in the “Ping-Pong” mode or in independent normal operation mode. Setting this field to “Normal

In demodulation mode, when set to 0, T16 captures and reloads on detection of all the edges. When set to 1, T16 captures and detects on the first edge, but ignores the subsequent edges. For details, see “T16 Demodulation Mode” on page 60.

Time_Out

This bit is set when T16 times out (terminal count reached). To reset it, a 1 must be written to this location.

T16_Clock

This bit defines the frequency of the input signal to Counter/Timer16.

Capture_INT_Mask

Set this bit to allow interrupt when data is captured into LO16 and HI16.

Counter_INT_Mask

Set this bit to allow interrupt when T16 times out.

P35_Out

This bit defines whether P35 is used as a normal output pin or T16 output.

SMR2(F)0Dh Register

Table 25 describes Stop-Mode Recovery Register 2.

Table 25. SMR2(F)0Dh Register

Field	Bit Position		Value	Description
Reserved	7-------		0	Reserved (Must be 0)
Recovery Level	-6------	W	0* 1	Low High
Reserved	--5-----		0	Reserved (Must be 0)
Source	---432--	W	000* 001 010 011 100 101 110 111	A. POR Only B. NAND of P23–P20 C. NAND or P27–P20 D. NOR of P33–P31 E. NAND of P33–P31 F. NOR of P33–P31, P00, P07 G. NAND of P33–P31, P00, P07 H. NAND of P33–P31, P22–P20
Reserved	------10		00	Reserved (Must be 0)

Note: * Indicates the value upon Power-On Reset.

Eight-Bit Counter/Timer Circuits

Figure 26 shows the 8-bit counter/timer circuits.

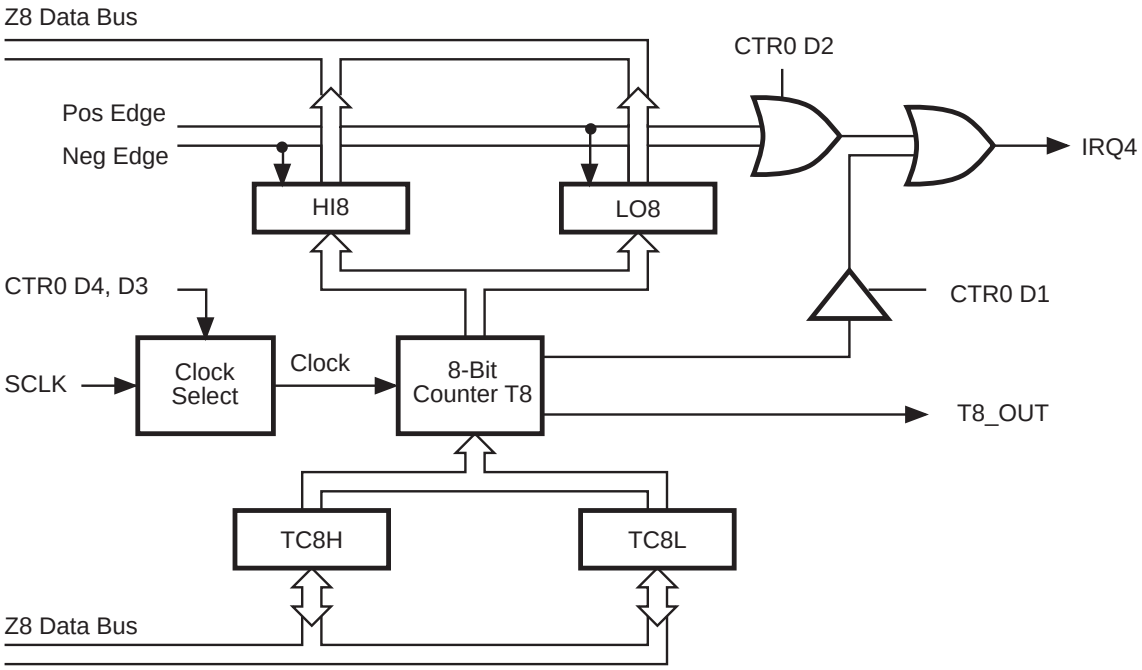


Figure 26. Eight-Bit Counter/Timer Circuits

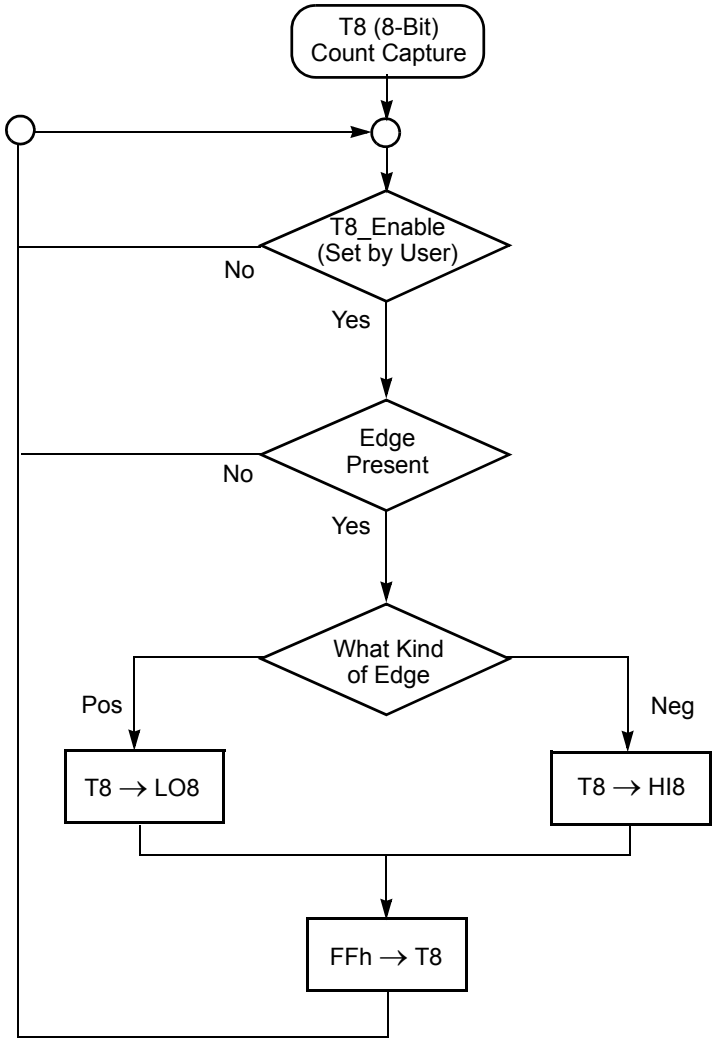
T8 Transmit Mode

When T8 is enabled, the output of T8 depends on CTR1, D1. If it is 0, T8_OUT is 1. If it is 1, T8_OUT is 0.

When T8 is enabled, the output T8_OUT switches to the initial value (CTR1 D1). If the initial value (CTR1 D1) is 0, TC8L is loaded; otherwise, TC8H is loaded into the counter (see Figure 27). In Single-Pass Mode (CTR0 D6), T8 counts down to 0 and stops, T8_OUT toggles, the time-out status bit (CTR0 D5) is set, and a time-out interrupt can be generated if it is enabled (CTR0 D1). See Figure 28. In Modulo-N Mode, upon reaching terminal count, T8_OUT is toggled, but no interrupt is generated. Then T8 loads a new count (if the T8_OUT level now is 0), TC8L is loaded; if it is 1, TC8H is loaded. T8 counts down to 0, toggles T8_OUT, sets the time-out status bit (CTR0 D5), and generates an interrupt if enabled (CTR0 D1). See Figure 29. This completes one cycle. T8 then loads from TC8H or TC8L according to the T8_OUT level, and repeats the cycle.

T8 Demodulation Mode

You need to program TC8L and TC8H to FFh. After T8 is enabled, when the first edge (rising, falling, or both depending on CTR1 D5, D4) is detected, it starts to count down. When a subsequent edge (rising, falling, or both depending on CTR1 D5, D4) is detected during counting, the current value of T8 is one's complemented and put into one of the capture registers. If it is a positive edge, data is put into LO8; if negative edge, HI8. One of the edge-detect status bits (CTR1 D1, D0) is set, and an interrupt can be generated if enabled (CTR0 D2). Meanwhile, T8 is loaded with FFh and starts counting again. When T8 reaches 0, the time-out status bit (CTR0 D5) is set, an interrupt can be generated if enabled (CTR0 D1), and T8 continues counting from FFh (see Figure 30 and Figure 31).



If D6 of CTR2 Is 1

T16 ignores the subsequent edges in the input signal and continues counting down. A time out of T8 causes T16 to capture its current value and generate an interrupt if enabled (CTR2, D2). In this case, T16 does not reload and continues counting. If D6 bit of CTR2 is toggled (by writing a 0 and then a 1 to it), T16 captures and reloads on the next edge (rising, falling, or both, depending on CTR1 D5, D4) but continues to ignore subsequent edges.

When T16 reaches 0, it continues counting from FFFFh. Meanwhile, a status bit (CTR2 D5) is set, and an interrupt time-out can be generated if enabled (CTR2 D1).

Ping-Pong Mode

This operation mode is only valid in transmit mode. T8 and T16 need to be programmed in Single-Pass Mode (CTR0 D6, CTR2 D6), and Ping-Pong Mode needs to be programmed in CTR1 D3, D2. You can begin the operation by enabling either T8 or T16 (CTR0 D7 or CTR2 D7). For example, if T8 is enabled, T8_OUT is set to this initial value (CTR1 D1). According to T8_OUT's level, TC8H or TC8L is loaded into T8. After the terminal count is reached, T8 is disabled and T16 is enabled. T16_OUT switches to its initial value (CTR1 D0), data from TC16H and TC16L is loaded, and T16 starts to count. After T16 reaches the terminal count, it stops, T8 is enabled again, and the whole cycle repeats. Interrupts can be allowed when T8 or T16 reaches terminal control (CTR0 D1, CTR2 D1). To stop the Ping-Pong operation, write 00 to bits D3 and D2 of CTR1. See Figure 35.

Note: Enabling Ping-Pong operation while the counter/timers are running might cause intermittent counter/timer function. Disable the counter/timers and then reset the status flags before instituting this operation.

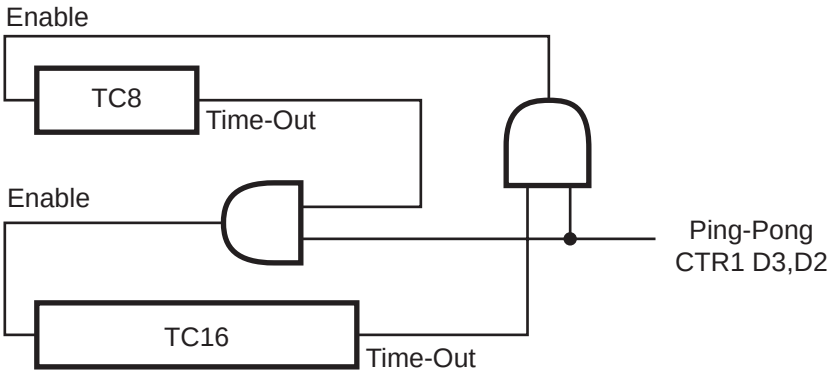


Figure 35. Ping-Pong Mode

The crystal must be connected across XTAL1 and XTAL2 using the recommended capacitors (capacitance greater than or equal to 22 pF) from each pin to ground. The RC oscillator configuration is an external resistor connected from XTAL1 to XTAL2, with a frequency-setting capacitor from XTAL1 to ground (see Figure 38).

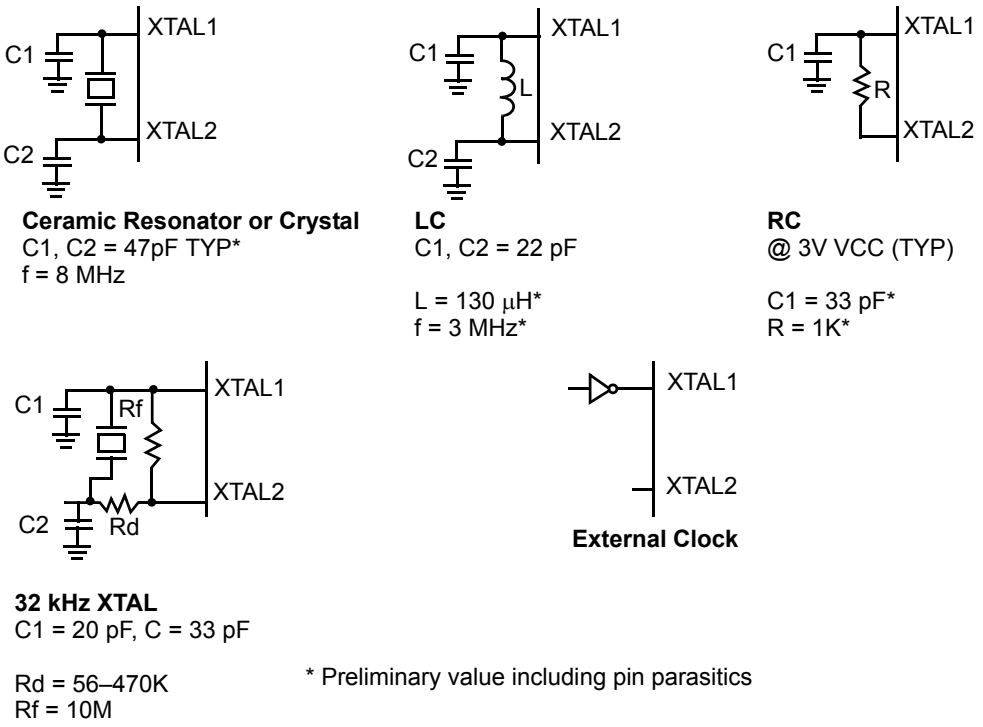


Figure 38. Oscillator Configuration

Power-On Reset (POR)

A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR time allows VCC and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

- Power Fail to Power OK status.
- Stop-Mode Recovery (if D5 of SMR = 1).
- WDT Time-Out.

The POR time is a nominal 5 ms. Bit 5 of the Stop-Mode Register determines whether the POR timer is bypassed after Stop-Mode Recovery (typical for external clock, RC, and LC oscillators).

Comparator Output Port 3 (D0)

Bit 0 controls the comparator used in Port 3. A 1 in this location brings the comparator outputs to P34 and P37, and a 0 releases the port to its standard I/O configuration.

Port 0 Output Mode (D2)

Bit 2 controls the output mode of Port 0. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.

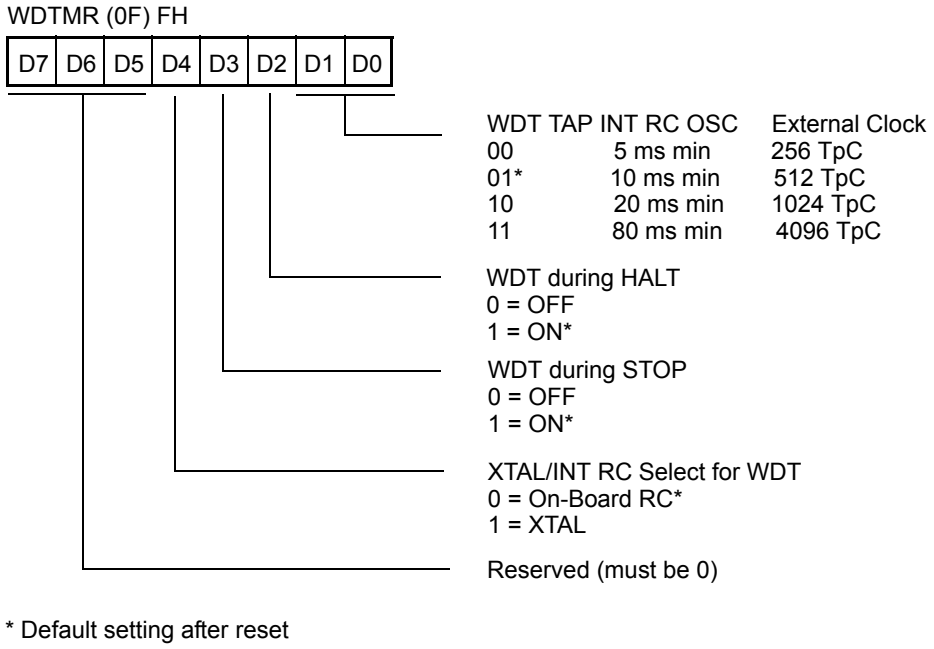
Stop-Mode Recovery Register (SMR)

This register selects the clock divide value and determines the mode of Stop-Mode Recovery (Figure 40). All bits are write only except bit 7, which is read only. Bit 7 is a flag bit that is hardware set on the condition of STOP recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits D2, D3, and D4 of the SMR register specify the source of the Stop-Mode Recovery signal. Bit D0 determines if SCLK/TCLK are divided by 16 or not. The SMR is located in Bank F of the Expanded Register Group at address 0BH.

Watch-Dog Timer Mode Register (WDTMR)

The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT must initially be enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT circuit is driven by an on-board RC oscillator or external oscillator from the XTAL1 pin. The WDT instruction affects the Zero (Z), Sign (S), and Overflow (V) flags.

The POR clock source is selected with bit 4 of the WDT register. Bit 0 and 1 control a tap circuit that determines the time-out period. Bit 2 determines whether the WDT is active during HALT, and Bit 3 determines WDT activity during STOP. Bits 5 through 7 are reserved. See Figure 43.



* Default setting after reset

Figure 43. Watch-Dog Timer Mode Register—Write Only

This register is accessible only during the first 60 processor cycles (SCLK) from the execution of the first instruction after Power-On-Reset, Watch-Dog Reset, or a Stop-Mode Recovery (Figure 40 on page 68). After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in Bank F of the Expanded Register Group at address location 0FH. It is organized as shown in Figure 43.

EPROM Programming

Table 31 describes the programming and test modes.

Table 31. Programming and Test Modes

	Device Pins									
User/Test Mode Device Pin # User Modes	**P33 V_{PP}**	**P32 EPM**	**Pref1 /CE**	**P31 /OE**	**P20 /PGM**	**Addr**	**V_{CC}**	**Port 1 CNFG DATA**	**Test ADDR A0–A3**	**Note**
EPROM Read	V_{CC}	V_H	V_{IL}	V_{IL}	V_{IH}	Addr	3.0 V	Out	XX	
Program	V_{PP}	V_{CC}	V_{IL}	V_{IH}	V_{IL}	Addr	6.0 V	In	XX	
Program Verify	V_{PP}	V_{CC}	V_{IL}	V_{IL}	V_{IH}	Addr	6.0 V	Out	XX	
RC Option	V_{PP}	V_{CC}	V_H	V_{IH}	V_{IL}	XX	6.0 V	XX	XX	
Margin Read	V_{VA}	V_H	V_{IL}	V_H	V_{IH}	Addr	6.0 V	Out	00	1
Shadow Row Rd	V_{CC}	V_H	V_{IL}	V_{IL}	V_{IH}	COL	3.0 V	Out	01	1
Shadow Row Prg	V_{PP}	V_H	V_{IL}	V_{IH}	V_{IL}	COL	6.0 V	In	01	1
Shadow Row Ver	V_{PP}	V_H	V_{IL}	V_{IL}	V_{IH}	COL	6.0 V	Out	01	1
Shadow Col Rd	V_{CC}	V_H	V_{IL}	V_{IL}	V_{IH}	ROW	3.0 V	Out	02	1
Shadow Col Prg	V_{PP}	V_H	V_{IL}	V_{IH}	V_{IL}	ROW	6.0 V	In	03	1
Shadow Col Ver	V_{PP}	V_H	V_{IL}	V_{IL}	V_{IH}	ROW	6.0 V	Out	02	1
Page Prg 2 Byte	V_{PP}	V_H	V_{IL}	V_{IH}	V_{IL}	TBD	6.0 V	In	04	1
Page Prg 4 Byte	V_{PP}	V_H	V_{IL}	V_{IH}	V_{IL}	TBD	6.0 V	In	05	1
Page Prg 8 Byte	V_{PP}	V_H	V_{IL}	V_{IH}	V_{IL}	TBD	6.0 V	In	06	1
Page Prg 16 Byte	V_{PP}	V_H	V_{IL}	V_{IH}	V_{IL}	TBD	6.0 V	In	07	1

Notes:
1. All test modes are entered by first setting up the corresponding test address and then latching the address by bringing the /OE to V_H and then to V_{IL}, except for the margin read which requires /OE to be kept at V_H.

V_{VA} = Variable from V_{CC} to V_{PP}
V_{PP} = 12.5 V ± 0.5 V
V_H = 12.5 V ± 0. 5 V
V_{IH} = 3 V
V_{IL} = 0 V
XX = Irrelevant
I_{PP} during programming = 40 mA maximum
I_{CC} during programming, verify, or read = 40 mA maximum.

Table 32 lists the timing of the programming waveform.

Table 32. Timing of Programming Waveform

Parameters	Name	Min	Max	Units
1	Address Setup Time	2		µs
2	Data Setup Time	2		µs
3	V_{PP} Setup Time	2		µs
4	V_{CC} Setup Time	2		µs
5	Chip Enable Setup Time	2		µs
6	Program Pulse Width	0.95		µs
7	Data Hold Time	2		µs
8	/OE Setup Time	2		µs
9	Data Access Time		200	ns
10	Data Output Float Time		100	ns
11	Overprogram Pulse Width	2.85		ms
12	EPM Setup Time	2		µs
13	/PGM Setup Time	2		µs
14	Address to /OE Setup Time	2		µs
15	Option Program Pulse Width	78		ms

Figure 45 shows the EPROM read timing diagram. Figure 46 on page 79 shows the EPROM program and verify timing diagram. Figure 47 on page 80 shows the programming EPROM, RAM protect, and 16K size selection timing diagram.

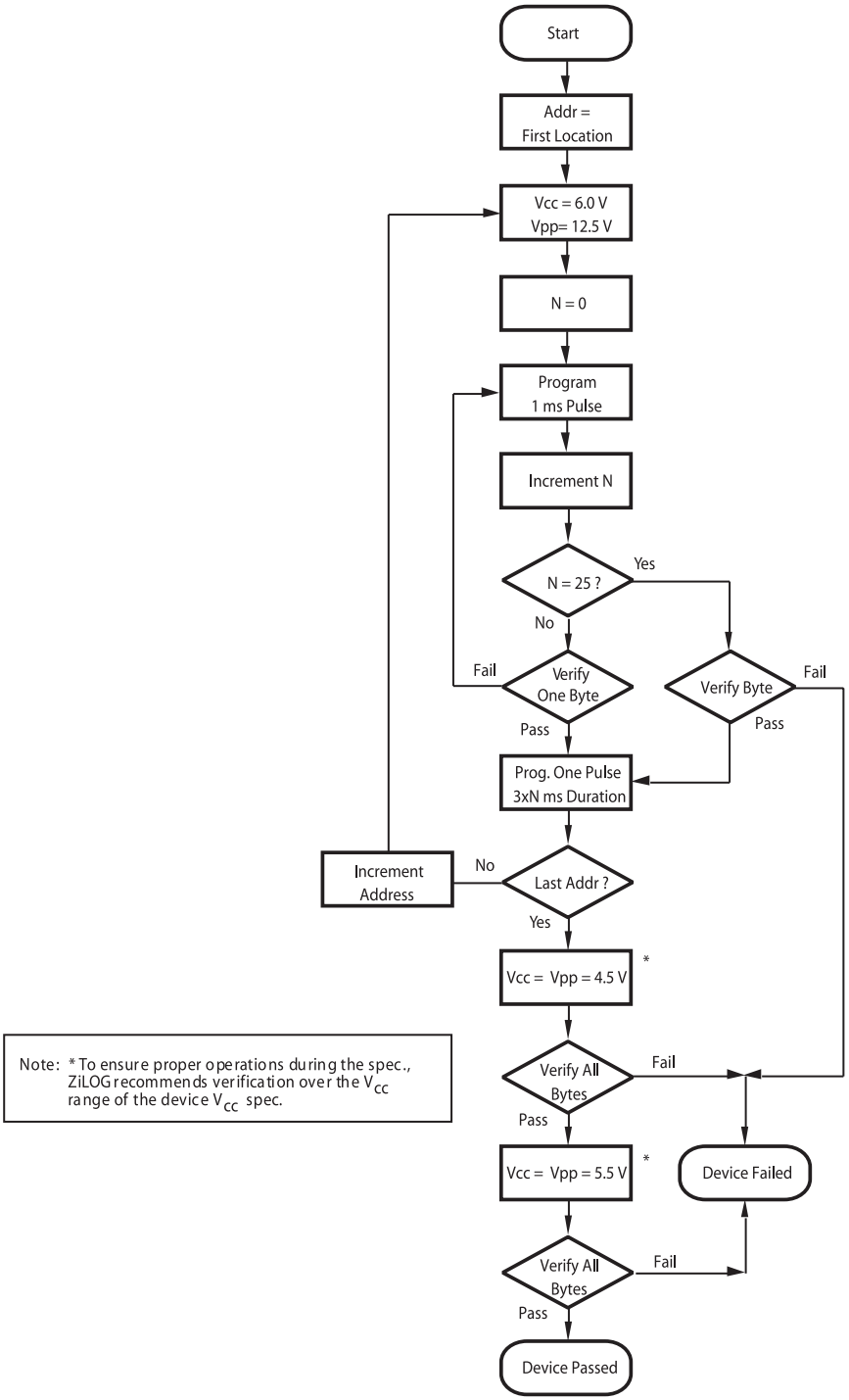
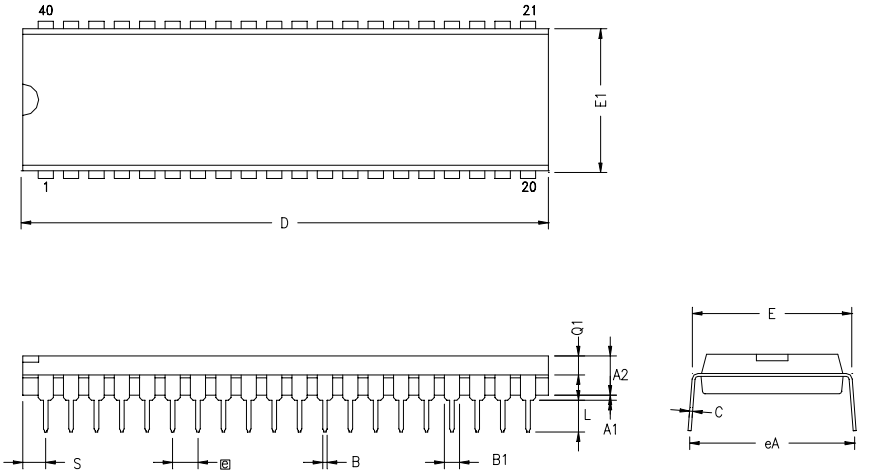


Figure 48. Programming Flowchart

Package Information

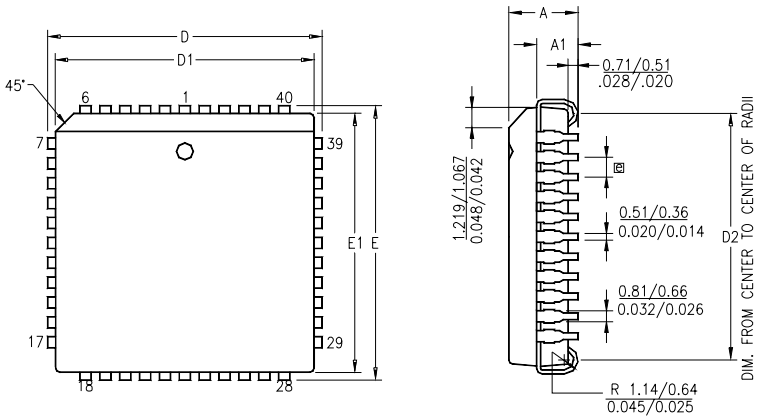
The Z86E72/73 is available in 40-pin DIP (Figure 67), 44-pin LQFP (Figure 68 on page 95), and 44-pin PLCC (Figure 69 on page 96) packages.



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	1.02	.020	.040
A2	3.18	3.94	.125	.155
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
e	2.54 TYP		.100 TYP	
eA	15.49	16.76	.610	.660
L	3.05	3.81	.120	.150
Q1	1.40	1.91	.055	.075
S	1.52	2.29	.060	.090

CONTROLLING DIMENSIONS : INCH

Figure 67. 40-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.27	4.57	0.168	0.180
A1	2.41	2.92	0.095	0.115
D/E	17.40	17.65	0.685	0.695
D1/E1	16.51	16.66	0.650	0.656
D2	15.24	16.00	0.600	0.630
e	1.27 BSC		0.050 BSC	

NOTES:
1. CONTROLLING DIMENSION : INCH
2. LEADS ARE COPLANAR WITHIN 0.004".
3. DIMENSION : MM
INCH

Figure 69. 44-Pin PLCC Package Diagram