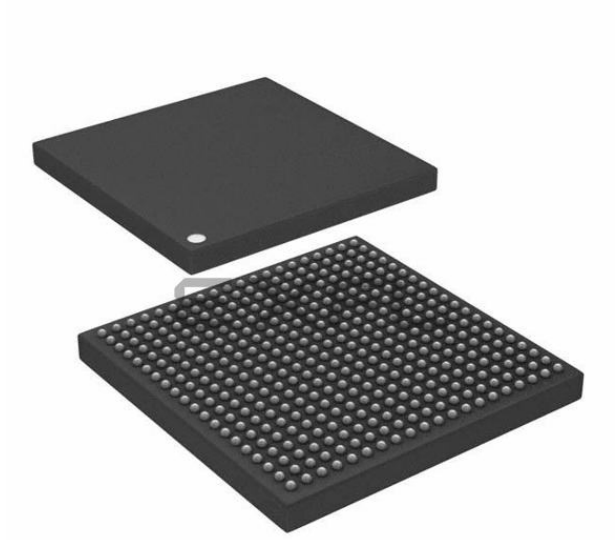

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM926EJ-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	LPDDR, DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	Keypad
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	2.0V, 2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	Boot Security, Cryptography, Secure Fusebox, Secure JTAG, Secure Memory, Tamper Detection
Package / Case	400-LFBGA
Supplier Device Package	400-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx251ajm4

2 Features

Table 3 describes the digital and analog modules of the device.

Table 3. i.MX25 Digital and Analog Modules

Block Mnemonic	Block Name	Subsystem	Brief Description
1-WIRE	1-Wire Interface	Connectivity peripherals	1-Wire support provided for interfacing with an on-board EEPROM, and smart battery interfaces, for example: Dallas DS2502.
ARM9 or ARM926	ARM926 platform and memory	ARM	The ARM926 Platform consists of the ARM 926EJ-S core, the ETM real-time debug modules, a 5x5 Multi-Layer AHB crossbar switch, and a “primary AHB” complex. It contains the 16 Kbyte L1 instruction cache, 16 Kbyte L1 data cache, 32 Kbyte ROM and 128 Kbyte RAM.
ATA	ATA module	Connectivity peripherals	The ATA module is an AT attachment host interface. Its main use is to interface with IDE hard disc drives and ATAPI optical disc drives. It interfaces with the ATA device over a number of ATA signals.
AUDMUX	Digital audio mux	Multimedia peripherals	The AUDMUX is a programmable interconnect for voice, audio, and synchronous data routing between host serial interfaces (SSIs) and peripheral serial interfaces (audio codecs). The AUDMUX has two sets of interfaces: internal ports to on-chip peripherals, and external ports to off-chip audio devices. Data is routed by configuring the appropriate internal and external ports.
CCM	Clock control module	Clocks	This block generates all clocks for the iMX25 system. The CCM also manages the ARM926 Platform's low-power modes (wait, stop, and doze) by disabling peripheral clocks appropriately for power conservation.
CSPI(3)	Configurable serial peripheral interface	Connectivity peripherals	This module is a serial interface equipped with data FIFOs. Each master/slave-configurable SPI module is capable of interfacing to both serial port interface master and slave devices. The CSPI ready (SPI_RDY) and Slave Select (SS) control signals enable fast data communication with fewer software interrupts.
DRYICE	DryIce module	Security	DryIce provides volatile key storage for Point-of-Sale (POS) terminals, and a trusted time source for Digital Rights Management (DRM) schemes. Several tamper-detect circuits are also provided to support key erasure and time invalidation in the event of tampering. Alarms and/or interrupts can also assert if tampering is detected. DryIce also includes a Real Time clock (RTC) that can be used in secure and non-secure applications.
EMI	External memory interface	Connectivity peripherals	The External Memory Interface (EMI) module provides access to external memory for the ARM and other masters. It is composed of four main submodules: • M3IF provides arbitration between multiple masters requesting access to the external memory. • Enhanced SDRAM/LPDDR memory controller (ESDCTL) interfaces to DDR2 and SDR interfaces. • NAND Flash controller (NFC) provides an interface to NAND Flash memories. • Wireless External Interface Memory controller (WEIM) interfaces to NOR Flash and PSRAM.

Table 6. DC Operating Conditions (continued)

Parameter	Symbol	Min.	Typ.	Max.	Units
I/O supply voltage, GPIO CRM,LCDC,JTAG,MISC	NV_{DD_GPIO2}	3.0	3.3	3.6	—
I/O supply voltage DDR (Mobile DDR mode) EMI1, EMI2	NV_{DD_MDDR}	1.75	—	1.95	V
I/O supply voltage DDR (DDR2 mode) EMI1,EMI2	NV_{DD_DDR2}	1.75	—	1.9	V
I/O supply voltage DDR (SDRAM mode) EMI1,EMI2	NV_{DD_SDRAM}	1.75	—	3.6	V
Supply of USBPHY1 (HS) USBPHY1_VDDA_BIAS, USBPHY1_UPLL_VDD,USBPHY1_VDDA	$V_{DD\_usbphy1}$	3.17	3.3	3.43	V
Supply of USBPHY2 (FS) USBPHY2_VDD	$V_{DD\_usbphy2}$	3.0	3.3	3.6	V
Supply of OSC24M OSC24M_VDD	V_{DD_OSC24M}	3.0	3.3	3.6	V
Supply of PLL MPLL_VDD,UPLL_VDD	V_{DD_PLL}	1.4	—	1.65	V
Supply of touchscreen ADC NVCC_ADC	V_{DD_tsc}	3.0	3.3	3.6	V
External reference of touchscreen ADC Ref	Vref	2.5	V_{DD_tsc}	V_{DD_tsc}	V
Fusebox program supply voltage FUSE_VDD[2]	$FUSEV_{DD}$ (program mode)	3.3 ± 5%	—	3.6	V
Supply output[3] NVCC_DRYICE	$V_{DD\_}$	1.0	—	1.55	V
Operating ambient temperature	T_A	–40	—	85	°C

1 V_{DD_BAT} must always be powered by battery in security application. In non-security case, V_{DD_BAT} can be connected to QV_{DD}.

2 The fusebox read supply is connected to supply of the full speed USBPHY2_VDD. FUSE_VDD is only used for programming. It is recommended that FUSE_VDD be connected to ground when not being used for programming. See Table 7 for current parameters.

3 NVCC_DRYICE is a supply output. An external capacitor no less than 4 µF must be connected to it. A 4.7 µF capacitor is recommended.

3.1.3 Fusebox Supply Current Parameters

Table 7 lists the fusebox supply current parameters.

Table 7. Fusebox Supply Current Parameters

Parameter	Symbol	Min.	Typ.	Max.	Units
eFuse program current[1] Current to program one eFuse bit The associated VDD_FUSE supply = 3.6 V	$I_{program}$	26	35	62	mA
eFuse read current[2] Current to read an 8-bit eFuse word	I_{read}	—	12.5	15	mA

1 The current $I_{program}$ is during program time ($t_{program}$).

2 The current I_{read} is present for approximately 50 ns of the read access to the 8-bit word.

3.1.4 Interface Frequency Limits

Table 8 provides information for interface frequency limits.

Table 8. Interface Frequency Limits

Parameter	Min.	Typ.	Max.	Units
JTAG: TCK Frequency of Operation	DC	5	10	MHz
OSC24M_XTAL Oscillator	—	24	—	MHz
OSC32K_XTAL Oscillator	—	32.768	—	kHz

Table 9 provides the recommended external crystal specifications.

Table 9. Recommended External Crystal Specifications

	24 MHz	32.768 kHz
Frequency Tolerance	<= ± 30 ppm	<= ± 30 ppm
ESR	< 80 Ω	50 K~60 K
Load Capacitor	8 pF–12 pF	6 pF–8 pF (12 pF–16 pF on each pin)
Shunt Capacitor	< 7 pF	1 pF
Drive Level	> 150 µW	> 1 µW

Table 10 provides the recommended external reference clock oscillator specifications (when reference is used from an external clock source).

Table 10. Recommended External Reference Clock Specifications

	24 MHz	32.768 kHz
V_{OH}	min = 0.7* VDD	min = 0.7* VDD
V_{OL}	max = 0.3* VDD	max = 0.3* VDD
Frequency Tolerance	= 30 ppm	= 30 ppm

NOTE

The term ‘OVDD’ in this section refers to the associated supply rail of an input or output. The association is shown in the “Signal Multiplexing” chapter of the reference manual.

3.5.1 DDR I/O DC Parameters

The DDR pad type is configured by the IOMUXC_SW_PAD_CTL_GRP_DDRTYPE register (see the External Signals and Pin Multiplexing chapter of the *i.MX25 Reference Manual* for details).

3.5.1.1 DDR_TYPE = 00 Standard Setting DDR I/O DC Parameters

Table 17 shows the I/O parameters for mobile DDR. These settings are suitable for mDDR and DDR2 1.8V (± 5%) applications.

Table 17. Mobile DDR I/O DC Electrical Characteristics

DC Electrical Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
High-level output voltage	Voh	I_{OH} = –1mA I_{OH} = Specified Drive	OVDD – 0.08 0.8 × OVDD	—	—	V
Low-level output voltage	Vol	I_{OL} = 1mA I_{OL} = Specified Drive	—	—	0.08 0.2 × OVDD	V
High-level output current	I Ioh	Voh = 0.8 × OVDDV Standard Drive High Drive Max. Drive	 –3.6 –7.2 –10.8	—	—	 mA
Low-level output current	I Iol	Vol = 0.2 × OVDDV Standard Drive High Drive Max. Drive	 3.6 7.2 10.8	—	—	 mA
High-level DC CMOS input voltage	VIH	—	0.7 × OVDD	OVDD	OVDD+0.3	V
Low-level DC CMOS input voltage	VIL	—	–0.3	0	0.3 × OVDD	V
Differential receiver VTH+	VTH+	—		—	100	mV
Differential receiver VTH-	VTH-		–100	—	—	mV
Input current (no pull-up/down)	IIN	VI = 0 VI = OVDD	—	—	110 60	nA
High-impedance I/O supply current	Icc-ovdd	VI = OVDD or 0	—	—	990	nA
High-impedance core supply current	Icc-vddi	VI = VDD or 0	—	—	1220	nA

Table 19. DDR2 (SSTL_18) I/O DC Electrical Characteristics (continued)

DC Electrical Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Termination voltage[5]	Vtt	—	OVDD/2 – 0.04	OVDD/2	OVDD/2 + 0.04	
Input current[6](no pull-up/down)	IIN	VI = 0 VI = OVDD	—	—	110 60	nA
High-impedance I/O supply current[6]	Icc-ovdd	VI = OVDD or 0	—	—	980	nA
High-impedance core supply current[6]	Icc-vddi	VI = VDD or 0	—	—	1210	nA

1 OVDD = 1.7 V; V_{out} = 1.42 V. (V_{out}-OVDD)/IOH must be less than 21 W for values of V_{out} between OVDD and OVDD-0.28 V.

2 OVDD = 1.7 V; V_{out} = 280 mV. V_{out}/IOL must be less than 21 W for values of V_{out} between 0 V and 280 mV. Simulation circuit for parameters V_{oh} and V_{ol} for I/O cells is below.

3 Vin(dc) specifies the allowable DC excursion of each differential input.

4 Vid(dc) specifies the input differential voltage required for switching. The minimum value is equal to Vih(dc) - Vil(dc).

5 Vtt is expected to track OVDD/2.

6 Minimum condition: BCS model, 1.95 V, and –40 °C. Typical condition: typical model, 1.8 V, and 25 °C. Maximum condition: wcs model, 1.65 V, and 105 °C.

3.5.2 GPIO I/O DC Parameters

Table 20 shows the I/O parameters for GPIO.

Table 20. GPIO DC Electrical Characteristics

DC Electrical Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
High-level output voltage[1]	Voh	Ioh=–1mA Ioh = Specified Drive	OVDD – 0.15 0.8 × OVDD	—	—	V
Low-level output voltage[1]	Vol	Iol=1mA Iol=Specified Drive	—	—	0.15 0.2 × OVDD	V
High-level output current for slow mode	I Ioh	Voh=0.8 × OVDD Standard Drive High Drive Max. Drive	 –2.0 –4.0 –8.0	—	—	mA
High-level output current for fast mode	I Ioh	Voh=0.8 × OVDD Standard Drive High Drive Max. Drive	 –4.0 –6.0 –8.0	—	—	mA
Low-level output current for slow mode	I Iol	Voh=0.2 × OVDD Standard Drive High Drive Max. Drive	 2.0 4.0 8.0	—	—	mA
Low-level output current for fast mode	I Iol	Voh=0.2 × OVDD Standard Drive High Drive Max. Drive	 4.0 6.0 8.0	—	—	mA
High-level DC input voltage	VIH	—	0.7 × OVDD	—	OVDD	V
Low-level DC input voltage	VIL	—	–0.3 V	—	0.3 × OVDD	V

Table 20. GPIO DC Electrical Characteristics (continued)

DC Electrical Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Input hysteresis	VHYS	OVDD = 3.3 V OVDD = 1.8V	370 290	—	420 320	mV
Schmitt trigger VT+[1]	VT+	—	0.5 × OVDD	—	—	V
Schmitt trigger VT–[1]	VT–	—	—	—	0.5 × OVDD	V
Pull-up resistor (22 kΩ PU)	Rpu	Vi=0	18.5	22	25.6	kΩ
Pull-up resistor (47 kΩ PU)	Rpu	Vi=0	41	47	55	kΩ
Pull-up resistor (100 kΩ PU)	Rpu	Vi=0	85	100	120	kΩ
Pull-down resistor (100 kΩ PD)	Rpd	VI = OVDD	85	100	120	kΩ
Input current (no pull-up/down)	IIN	VI = 0, OVDD = 3.3 V VI = OVDD = 3.3 V VI = 0, OVDD = 1.8 V VI = OVDD = 1.8 V	—	—	100 60 77 50	nA
Input current (22 kΩ PU)	IIN	VI = 0, OVDD = 3.3 V VI = OVDD = 3.3 V VI = 0, OVDD = 1.8 V VI = OVDD = 1.8 V	117 0.0001 64 0.0001	—	184 0.0001 104 0.0001	µA
Input current (47 kΩ PU)	IIN	VI = 0, OVDD = 3.3 V VI = OVDD = 3.3 V VI = 0, OVDD = 1.8 V VI = OVDD = 1.8 V	54 0.0001 30 0.0001	—	88 0.0001 49 0.0001	µA
Input current (100 kΩ PU)	IIN	VI = 0, OVDD = 3.3 V VI = OVDD = 3.3 V VI = 0, OVDD = 1.8 V VI = OVDD = 1.8 V	25 0.0001 14 0.0001	—	42 0.0001 23 0.0001	µA
Input current (100 kΩ PD)	IIN	VI = 0, OVDD = 3.3 V VI = OVDD = 3.3 V VI = 0, OVDD = 1.8 V VI = OVDD = 1.8 V	25 0.0001 14 0.0001	—	42 0.001 23 0.0001	µA
High-impedance I/O supply current	Icc–ovdd	VI = 0, OVDD = 3.3 V VI = OVDD = 3.3 V VI = 0, OVDD = 1.8 V VI = OVDD = 1.8 V	—	—	688 688 560 560	nA
High-impedance core supply current	Icc–vddi	VI = 0, OVDD = 3.3 V VI = OVDD = 3.3 V VI = 0, OVDD = 1.8 V VI = OVDD = 1.8 V	—	—	490 490 410 410	nA

[1] Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.

3.6 AC Electrical Characteristics

This section provides the AC parameters for slow and fast I/O.

Figure 3 shows the load circuit for output. Figure 4 through Figure 6 show the output transition time and propagation waveforms.

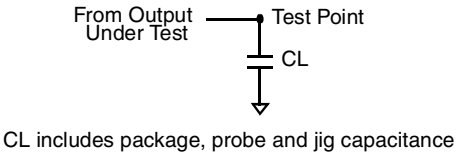

Figure 3. Load Circuit for Output

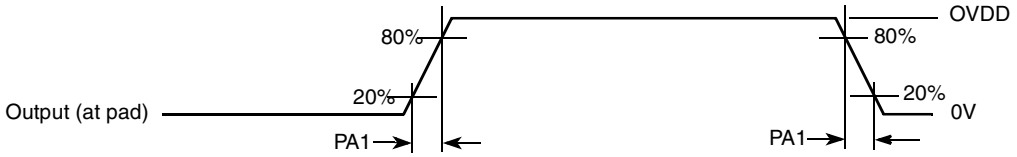

Figure 4. Output Pad Transition Time Waveform

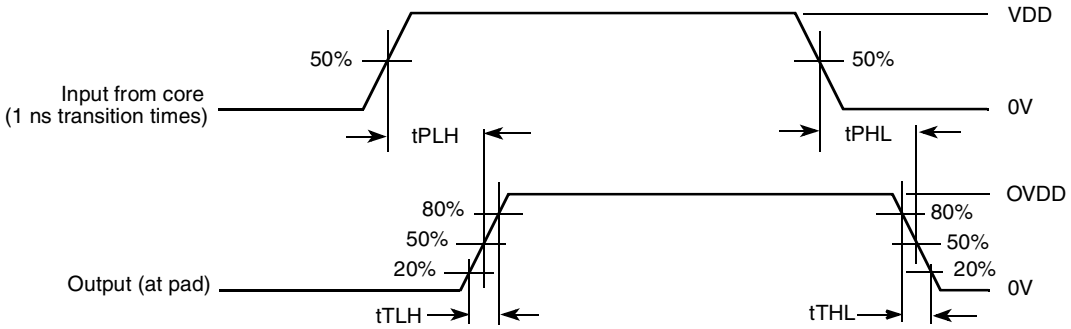

Figure 5. Output Pad Propagation and Transition Time Waveform

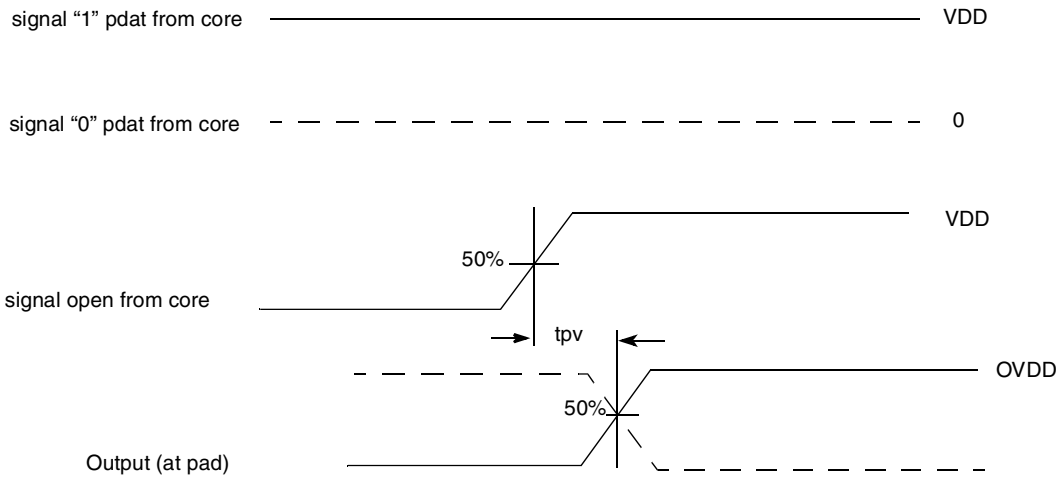

Figure 6. Output Enable to Output Valid

Table 21. Slow I/O AC Parameters (continued)

Parameter	Symbol	Test Voltage	Test Capacitance	Min. Rise/Fall	Typ. Rise/Fall	Max. Rise/Fall	Units
Output pad dI/dt[3] (max. drive)	tdit	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	15 16 7 7	36 38 21 22	76 80 56 58	mA /ns
Output pad dI/dt[3] (high drive)	tdit	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	8 9 5 5	20 21 14 15	45 47 38 40	
Output pad dI/dt[3] (standard drive)	tdit	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	4 4 2 2	10 10 7 7	22 23 18 19	
Input pad propagation delay without hysteresis, 50%–50%[4]	tpi	—	1.6 pF	0.82/0.47 0.74/1	1.1/0.76 1.1/1.5	1.6/1.04 1.75/2.16	ns
Input pad propagation delay with hysteresis, 50%–50%[4]	tpi	—	1.6 pF	1.1/1.3 1.75/1.63	1.43/1.6 2.67/2.22	2/2 2.92/3	
Input pad propagation delay without hysteresis, 40%–60%[4]	tpi	—	1.6 pF	1.62/1.28 1.82/1.55	1.9/1.56 2.28/1.87	2.38/1.82 2.95/2.54	
Input pad propagation delay with hysteresis, 40%–60%[4]	tpi	—	1.6 pF	1.88/2.1 2.4/2.6	2.2/2.4 3/3.07	2.7/2.75 3.77/3.71	
Input pad transition times without hysteresis[4]	trfi	—	1.6 pF	0.16/0.12	0.23/0.18	0.33/0.29	
Input pad transition times with hysteresis[4]	trfi		1.6 pF	0.16/0.13	0.22/0.18	0.33/0.29	
Maximum input transition times[5]	trm	—	—	—	—	25	ns

1 Maximum condition for tpr, tpo, and tpv: wcs model, 1.1 V, I/O 3.0 V (3.0–3.6 V range) or 1.65 V (1.65–1.95 V range), and 105 °C. Minimum condition for tpr, tpo, and tpv: bcs model, 1.3 V, I/O 3.6 V (3.0–3.6 V range) or 1.95 V (1.65–1.95 V range), and –40 °C. Input transition time from core is 1 ns (20%–80%).

2 Minimum condition for tps: wcs model, 1.1 V, I/O 3.0 V (3.0–3.6 V range) or 1.65 V (1.65–1.95 V range), and 105 °C. tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.

3 Maximum condition for tdit: bcs model, 1.3 V, I/O 3.6 V (3.0–3.6 V range) or 1.95 V (1.65–1.95 V range), and –40 °C.

4 Maximum condition for tpi and trfi: wcs model, 1.1 V, I/O 3.0 V (3.0–3.6 V range) or 1.65 V (1.65–1.95 V range), and 105 °C. Minimum condition for tpi and trfi: bcs model, 1.3 V, I/O 3.6 V or 1.95 V (1.65–1.95 V range), and –40 °C. Input transition time from pad is 5 ns (20%–80%).

5 Hysteresis mode is recommended for input with transition time greater than 25 ns.

Table 25 shows the AC parameters for mobile DDR pbijtov18_33_ddr_clk I/O.

Table 25. AC Parameters for Mobile DDR pbijtov18_33_ddr_clk I/O

Parameter	Symbol	Load Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	50	60	%
Clock frequency[1]	f	—	—	—	133	MHz
Output pad transition times[1] (max. drive)	tpr	25 pF 50 pF	0.52/0.51 0.98/0.96	0.79/0.72 1.49/1.34	1.25/1.09 2.31/1.98	ns
Output pad transition times[1] (high drive)	tpr	25 pF 50 pF	1.13/1.10 2.15/2.10	1.74/1.55 3.28/2.92	2.71/2.30 5.11/4.31	ns
Output pad transition times[1] (standard drive)	tpr	25 pF 50 pF	2.26/2.19 4.30/4.18	3.46/3.07 6.59/5.79	5.39/4.56 10.13/8.55	ns
Output pad propagation delay[1] (max. drive), 50%–50% input signals and crossing of output signals	tpo	15 pF 35 pF	1.28/1.19 1.56/1.47	1.97/1.83 2.37/2.23	2.98/2.78 3.57/3.37	ns
Output pad propagation delay[1] (high drive), 50%–50% input signals and crossing of output signals	tpo	15 pF 35 pF	1.54/1.43 2.14/2.04	2.34/2.20 3.22/3.08	3.54/3.33 4.85/4.65	ns
Output pad propagation delay[1] (standard drive), 50%–50% input signals and crossing of output signals	tpo	15 pF 35 pF	2.05/1.94 3.27/3.16	3.11/2.96 4.86/4.72	4.70/4.50 7.33/7.12	ns
Output pad propagation delay[1] (max. drive), 40%–60% input signals and crossing of output signals	tpo	15 pF 35 pF	1.45/1.36 1.73/1.64	2.13/2.00 2.53/2.40	3.14/2.94 3.74/3.54	ns
Output pad propagation delay[1] (high drive), 40%–60% input signals and crossing of output signals	tpo	15 pF 35 pF	1.70/1.60 2.31/2.21	2.51/2.37 3.38/3.24	3.70/3.50 5.02/4.82	ns
Output pad propagation delay[1] (standard drive), 40%–60% input signals and crossing of output signals	tpo	15 pF 35 pF	2.22/2.11 3.43/3.32	3.27/3.13 5.02/4.88	4.87/4.66 7.49/7.29	ns
Output enable to output valid delay[1] (max. drive), 50%–50%	tpv	15 pF 35 pF	1.16/1.12 1.42/1.41	1.91/1.81 2.31/2.20	3.10/2.89 3.72/3.47	ns
Output enable to output valid delay[1] (high drive), 50%–50%	tpv	15 pF 35 pF	1.39/1.39 1.98/2.02	2.28/2.18 3.18/3.04	3.69/3.43 5.08/4.69	ns
Output enable to output valid delay[1] (standard drive), 50%–50%	tpv	15 pF 35 pF	1.90/1.94 3.07/3.20	3.09/2.94 4.88/4.66	4.95/4.55 7.73/7.05	ns
Output enable to output valid delay[1] (max. drive), 40%–60%	tpv	15 pF 35 pF	1.28/1.24 1.49/1.47	2.00/1.90 2.32/2.21	3.14/2.93 3.64/3.41	ns
Output enable to output valid delay[1] (high drive), 40%–60%	tpv	15 pF 35 pF	1.45/1.44 1.92/1.95	2.28/2.19 2.99/2.87	3.60/3.36 4.69/4.36	ns
Output enable to output valid delay[1] (standard drive), 40%–60%	tpv	15 pF 35 pF	1.85/1.88 2.78/2.88	2.92/2.79 4.34/4.16	4.5894.25 6.79/6.24	ns
Output pad slew rate[2] (max. drive)	tps	25 pF 50 pF	0.37/0.45 0.30/0.36	0.64/0.79 0.52/0.61	1.14/1.36 0.90/1.02	V/ns

Table 27. AC Parameters for SDRAM I/O (continued)

Parameter	Symbol	Load Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Output pad slew rate[2] (standard drive)	tps	25 pF 50 pF	0.38/0.41 0.20/0.22	0.59/0.60 0.31/0.32	0.89/0.82 0.47/0.43	V/ns
Output pad dI/dt[3] (max. drive)	tdit	25 pF 50 pF	89 94	198 209	398 421	mA/ns
Output pad dI/dt[3] (high drive)	tdit	25 pF 50 pF	59 62	132 139	265 279	mA/ns
Output pad dI/dt[3] (standard drive)	tdit	25 pF 50 pF	29 31	65 69	132 139	mA/ns
Input pad transition times[4]	trfi	1.0 pF	0.07/0.08	0.11/0.12	0.16/0.20	ns
Input pad propagation delay, 50%–50%[4]	tpi	1.0 pF	0.35/1.17	0.63/1.53	1.16/2.04	ns
Input pad propagation delay, 40%–60%[4]	tpi	—	1.18/1.99	1.45/2.35	1.97/2.85	—

1 Maximum condition for tpr, tpo, tpi, and tpv: wcs model, 1.1 V, I/O 3.0 V, and 105 °C. Minimum condition for tpr, tpo, and tpv: bcs model, 1.3 V, I/O 3.6 V and –40 °C. Input transition time from core is 1 ns (20%–80%).

2 Minimum condition for tps: wcs model, 1.1 V, I/O 3.0 V, and 105 °C. tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.

3 Maximum condition for tdit: bcs model, 1.3 V, I/O 3.6 V, and –40 °C.

4 Maximum condition for tpi and trfi: wcs model, 1.1 V, I/O 3.0 V and 105 °C. Minimum condition for tpi and trfi: bcs model, 1.3 V, I/O 3.6 V and –40 °C. Input transition time from pad is 5 ns (20%–80%).

Table 28 shows AC parameters for SDRAM pbijtov18_33_ddr_clk I/O.

Table 28. AC Parameters for SDRAM pbijtov18_33_ddr_clk I/O

Parameter	Symbol	Load Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	50	60	%
Clock frequency[1]	f	—	—	—	133	MHz
Output pad transition times[1] (max. drive)	tpr	25 pF 50 pF	0.82/0.87 1.56/1.67	1.14/1.13 2.13/2.09	1.62/1.50 3.015/2.77	ns
Output pad transition times[1] (high drive)	tpr	25 pF 50 pF	1.23/1.31 2.31/2.47	1.71/1.68 3.22/3.12	2.39/2.22 4.53/4.16	ns
Output pad transition times[1] (standard drive)	tpr	25 pF 50 pF	2.44/2.60 4.65/4.99	3.38/3.27 6.38/6.23	4.73/4.38 9.05/8.23	ns
Output pad propagation delay[1] (max. drive), 50%–50% input signals and crossing of output signals	tpo	15 pF 35 pF	1.50/1.40 1.95/1.85	2.23/2.07 2.81/2.66	3.28/3.04 4.06/3.82	ns
Output pad propagation delay[1] (high drive), 50%–50% input signals and crossing of output signals	tpo	15 pF 35 pF	1.69/1.59 2.35/2.25	2.48/2.32 3.35/3.19	3.63/3.38 4.80/4.56	ns
Output pad propagation delay[1] (standard drive), 50%–50% input signals and crossing of output signals	tpo	15 pF 35 pF	2.26/2.15 3.59/3.49	3.24/3.08 4.98/4.82	4.66/4.42 7.00/6.75	ns
Output pad propagation delay[1] (max. drive), 40%–60% input signals and crossing of output signals	tpo	15 pF 35 pF	1.67/1.57 2.11/2.02	2.39/2.24 2.97/2.82	3.45/3.21 4.23/3.99	ns

3.7 Module Timing and Electrical Parameters

This section contains the timing and electrical parameters for i.MX25 modules.

3.7.1 1-Wire Timing Parameters

Figure 7 shows the reset and presence pulses (RPP) timing for 1-Wire.

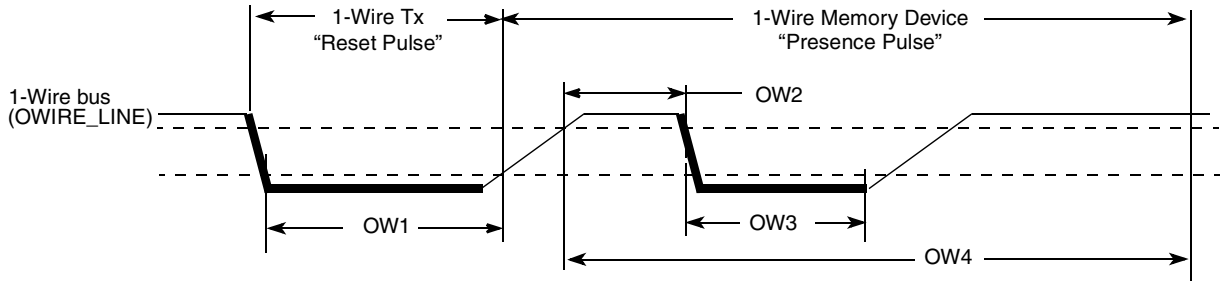

Figure 7. 1-Wire RPP Timing Diagram

Table 32 lists the RPP timing parameters.

Table 32. RPP Sequence Delay Comparisons Timing Parameters

ID	Parameters	Symbol	Min.	Typ.	Max.	Units
OW1	Reset Time Low	t_{RSTL}	480	511	—	µs
OW2	Presence Detect High	t_{PDH}	15	—	60	µs
OW3	Presence Detect Low	t_{PDL}	60	—	240	µs
OW4	Reset Time High	t_{RSTH}	480	512	—	µs

Figure 8 shows write 0 sequence timing, and Table 33 describes the timing parameters (OW5–OW6) that are shown in the figure.

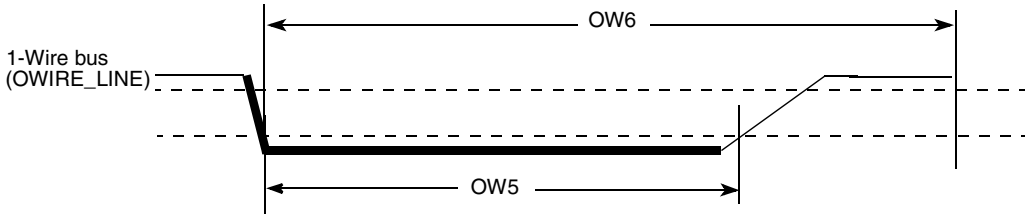

Figure 8. Write 0 Sequence Timing Diagram

Table 33. WR0 Sequence Timing Parameters

ID	Parameter	Symbol	Min.	Typ.	Max.	Units
OW5	Write 0 Low Time	t_{WR0_low}	60	100	120	µs
OW6	Transmission Time Slot	t_{SLOT}	OW5	117	120	µs

3.7.5 Configurable Serial Peripheral Interface (CSPI) Timing

Figure 23 and Figure 24 provide CSPI master and slave mode timing diagrams, respectively. Table 43 describes the timing parameters (t1–t14) that are shown in the figures. The values shown in timing diagrams were tested using a worst-case core voltage of 1.1 V, slow pad voltage of 2.68 V, and fast pad voltage of 1.65 V.

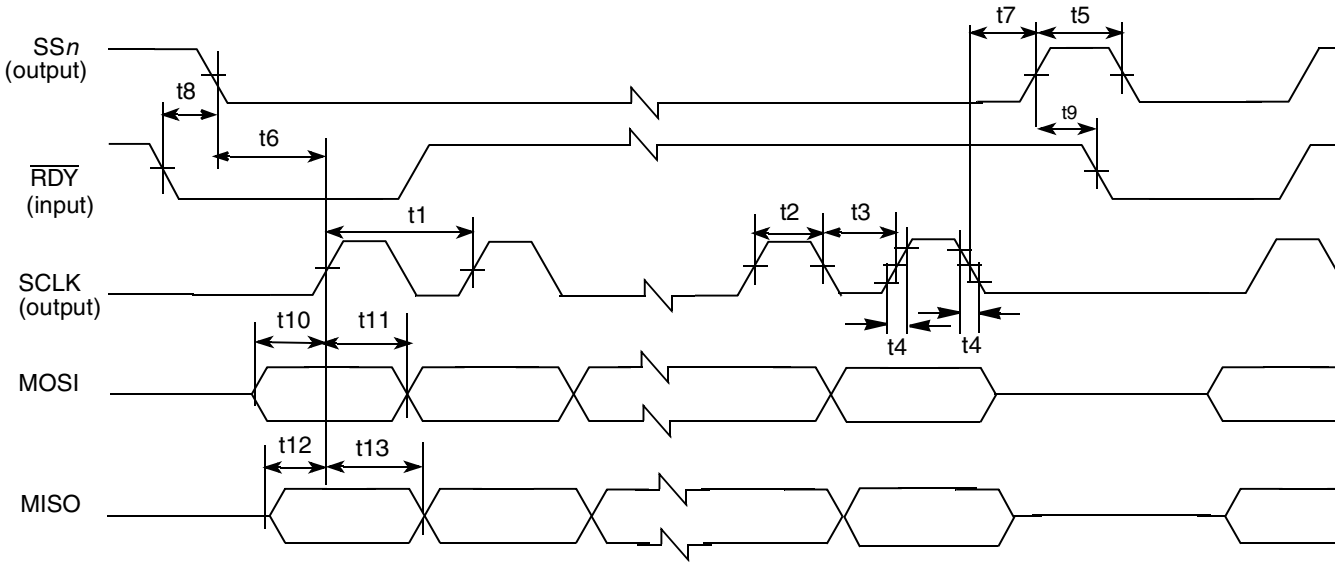

Figure 23. CSPI Master Mode Timing Diagram

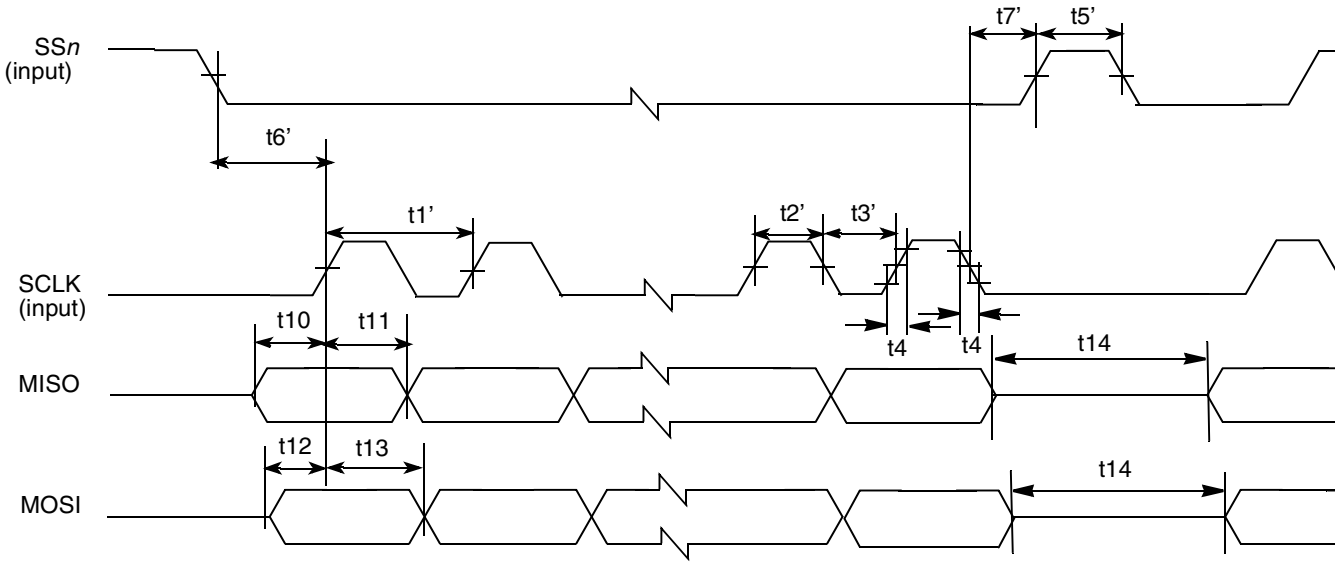

Figure 24. CSPI Slave Mode Timing Diagram

Table 57. WEIM Asynchronous Timing Parameters Relative to Chip Select Table (continued)

Ref No.	Parameter	Determination By Synchronous Measured Parameters[1]	Min	Max (If 133 MHz is supported by SoC)	Unit
WE32A(muxed A/D	$\overline{CS}$[x] valid to Address Invalid	WE4 – WE7 + (LBN + LBA + 1 – CSA[2])	–3 + (LBN + LBA + 1 – CSA)	—	ns
WE33	$\overline{CS}$[x] Valid to $\overline{RW}$ Valid	WE8 – WE6 + (RWA – CSA)	—	3 + (RWA – CSA)	ns
WE34	$\overline{RW}$ Invalid to $\overline{CS}$[x] Invalid	WE7 – WE9 + (RWN – CSN)	—	3 – (RWN_CSN)	ns
WE35	$\overline{CS}$[x] Valid to $\overline{OE}$ Valid	WE10 – WE6 + (OEA – CSA)	—	3 + (OEA – CSA)	ns
WE35A (muxed A/D)	$\overline{CS}$[x] Valid to $\overline{OE}$ Valid	WE10 – WE6 + (OEA + LBN + LBA + LAH + 1 – CSA)	–3 + (OEA + LBN + LBA + LAH + 1 – CSA)	3 + (OEA + LBN + LBA + LAH + 1 – CSA)	ns
WE36	$\overline{OE}$ Invalid to $\overline{CS}$[x] Invalid	WE7 – WE11 + (OEN – CSN)	—	3 – (OEN – CSN)	ns
WE37	$\overline{CS}$[x] Valid to $\overline{EB}$[y] Valid (Read access)	WE12 – WE6 + (EBRA – CSA)	—	3 + (EBRA[4] – CSA)	ns
WE38	$\overline{EB}$[y] Invalid to $\overline{CS}$[x] Invalid (Read access)	WE7 – WE13 + (EBRN – CSN)	—	3 – (EBRN[5] – CSN)	ns
WE39	$\overline{CS}$[x] Valid to $\overline{LBA}$ Valid	WE14 – WE6 + (LBA – CSA)	—	3 + (LBA – CSA)	ns
WE40	$\overline{LBA}$ Invalid to $\overline{CS}$[x] Invalid	WE7 – WE15 – CSN	—	3 – CSN	ns
WE40A (muxed A/D)	$\overline{CS}$[x] Valid to $\overline{LBA}$ Invalid	WE14 – WE6 + (LBN + LBA + 1 – CSA)	–3 + (LBN + LBA + 1 – CSA)	3 + (LBN + LBA + 1 – CSA)	ns
WE41	$\overline{CS}$[x] Valid to Output Data Valid	WE16 – WE6 – CSA	—	3 – CSA	ns
WE41A (muxed A/D)	$\overline{CS}$[x] Valid to Output Data Valid	WE16 – WE6 + (LBN + LBA + LAH + 1 – CSA)	—	3 + (LBN + LBA + LAH + 1 – CSA)	ns
WE42	Output Data Invalid to $\overline{CS}$[x] Invalid	WE17 – WE7 – CSN	—	3 – CSN	ns
WE43	Input Data Valid to $\overline{CS}$[x] Invalid	MAXCO – MAXCSO + MAXDI	MAXCO[6] – MAXCSO[7] + MAXDI[8]	—	ns
WE44	$\overline{CS}$[x] Invalid to Input Data invalid	0	0	—	ns
WE45	$\overline{CS}$[x] Valid to $\overline{EB}$[y] Valid (Write access)	WE12 – WE6 + (EBWA – CSA)	—	3 + (EBWA – CSA)	ns
WE46	$\overline{EB}$[y] Invalid to $\overline{CS}$[x] Invalid (Write access)	WE7 – WE13 + (EBWN – CSN)	—	–3 + (EBWN – CSN)	ns
WE47	$\overline{DTACK}$ Valid to $\overline{CS}$[x] Invalid	MAXCO – MAXCSO + MAXDTI	MAXCO[6] – MAXCSO[7] + MAXDTI[9]	—	ns
WE48	$\overline{CS}$[x] Invalid to $\overline{DTACK}$ invalid	0	0	—	ns

Table 60. ESAI General Timing Requirements (continued)

No.	Characteristics[1] [2]	Symbol	Expression[3]	Min.	Max.	Condition	Unit
86	SCKT rising edge to data out valid	—	—	— —	18.0 13.0	x ck i ck	ns
87	SCKT rising edge to data out high impedance[6]	—	—	— —	21.0 16.0	x ck i ck	ns
88	SCKT rising edge to transmitter #0 drive enable negation[6]	—	—	— —	14.0 9.0	x ck i ck	ns
89	FST input (bl, wr) setup time before SCKT falling edge[5]	—	—	2.0 18.0	— —	x ck i ck	ns
90	FST input (wl) setup time before SCKT falling edge	—	—	2.0 18.0	— —	x ck i ck	ns
91	FST input hold time after SCKT falling edge	—	—	4.0 5.0	— —	x ck i ck	ns
92	FST input (wl) to data out enable from high impedance	—	—	—	21.0	—	ns
93	FST input (wl) to transmitter #0 drive enable assertion	—	—	—	14.0	—	ns
94	Flag output valid after SCKT rising edge	—	—	— —	14.0 9.0	x ck i ck	ns
95	HCKR/HCKT clock cycle	—	2 x T_C	15	—	—	ns
96	HCKT input rising edge to SCKT output	—	—	—	18.0	—	ns
97	HCKR input rising edge to SCKR output	—	—	—	18.0	—	ns

1 V_{CORE_VDD} = 1.00 ± 0.10 V; T_J = –40 °C to 125 °C, C_L = 50 pF

2 In the “Characteristics” column, bl = bit length, wl = word length, wr = word length relative

3 In the “Expression” column, T_C = 7.5 ns.

4 For the internal clock, the external clock cycle is defined by Icyc and the ESAI control register.

5 The word-relative frame sync signal waveform relative to the clock operates in the same manner as the bit-length frame sync signal waveform, but spreads starting from one serial clock before the first bit clock (same as the bit length frame sync signal), until the second-to-last bit-clock of the first word in the frame.

6 Periodically sampled and not 100% tested.

3.7.8 Enhanced Secured Digital Host Controller (eSDHCv2) Timing

Figure 54 shows eSDHCv2 timing, and Table 61 describes the timing parameters (SD1–SD8) used in the figure. The following definitions apply to values and signals described in Table 61:

- LS: low-speed mode. Low-speed card can tolerate clocks up to 400 kHz
- FS: full-speed mode. Full-speed MMC card’s clock can reach 20 MHz; full speed SD/SDIO card clock can reach 25 MHz
- HS: high-speed mode. High-speed MMC card’s clock can reach 52 MHz; SD/SDIO card clock can reach 50 MHz

Table 64. MII Asynchronous Inputs Signal Timing

ID	Characteristic	Min.	Max.	Unit
M9[1]	FEC_CRS to FEC_COL minimum pulse width	1.5	—	FEC_TX_CLK period

[1] FEC_COL has the same timing in 10-Mbit 7-wire interface mode.

3.7.9.2 MII Serial Management Channel Timing (FEC_MDIO and FEC_MDC)

The MDC frequency is designed to be equal to or less than 2.5 MHz to comply with the IEEE 802.3 standard MII specification. However the FEC can function correctly with a maximum MDC frequency of 15 MHz.

Figure 58 shows MII asynchronous input timings. Table 65 describes the timing parameters (M10—M15) shown in the figure.

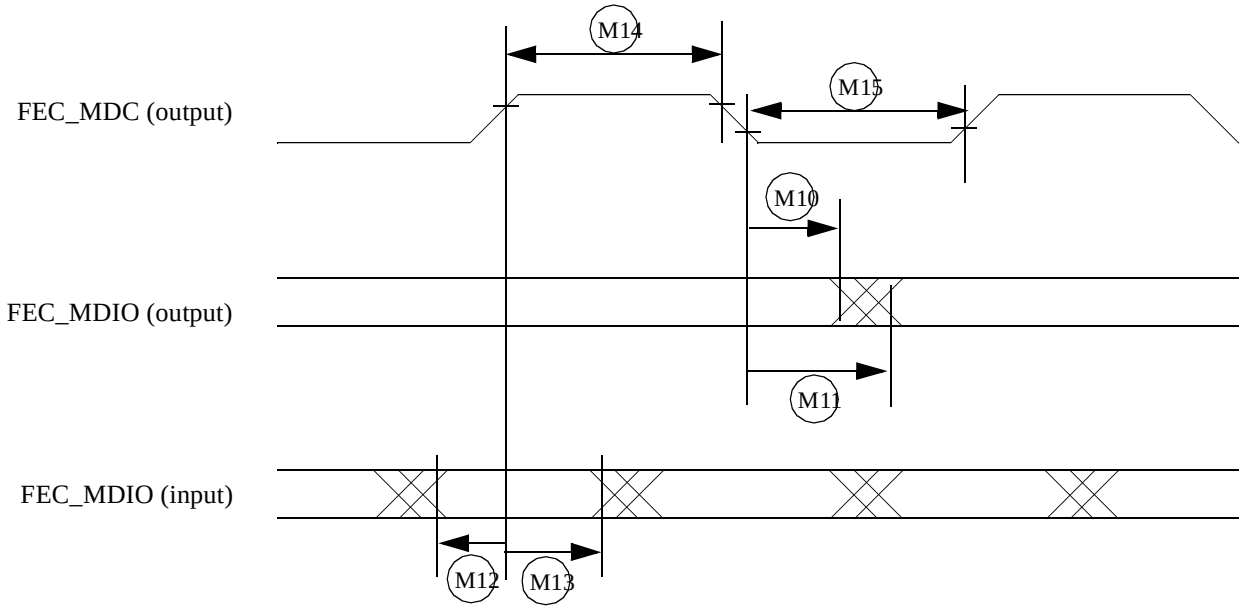

Figure 58. MII Serial Management Channel Timing Diagram

Table 65. MII Serial Management Channel Timing

ID	Characteristic	Min.	Max.	Unit
M10	FEC_MDC falling edge to FEC_MDIO output invalid (min. propagation delay)	0	—	ns
M11	FEC_MDC falling edge to FEC_MDIO output valid (max. propagation delay)	—	5	ns
M12	FEC_MDIO (input) to FEC_MDC rising edge setup	18	—	ns
M13	FEC_MDIO (input) to FEC_MDC rising edge hold	0	—	ns
M14	FEC_MDC pulse width high	40%	60%	FEC_MDC period
M15	FEC_MDC pulse width low	40%	60%	FEC_MDC period

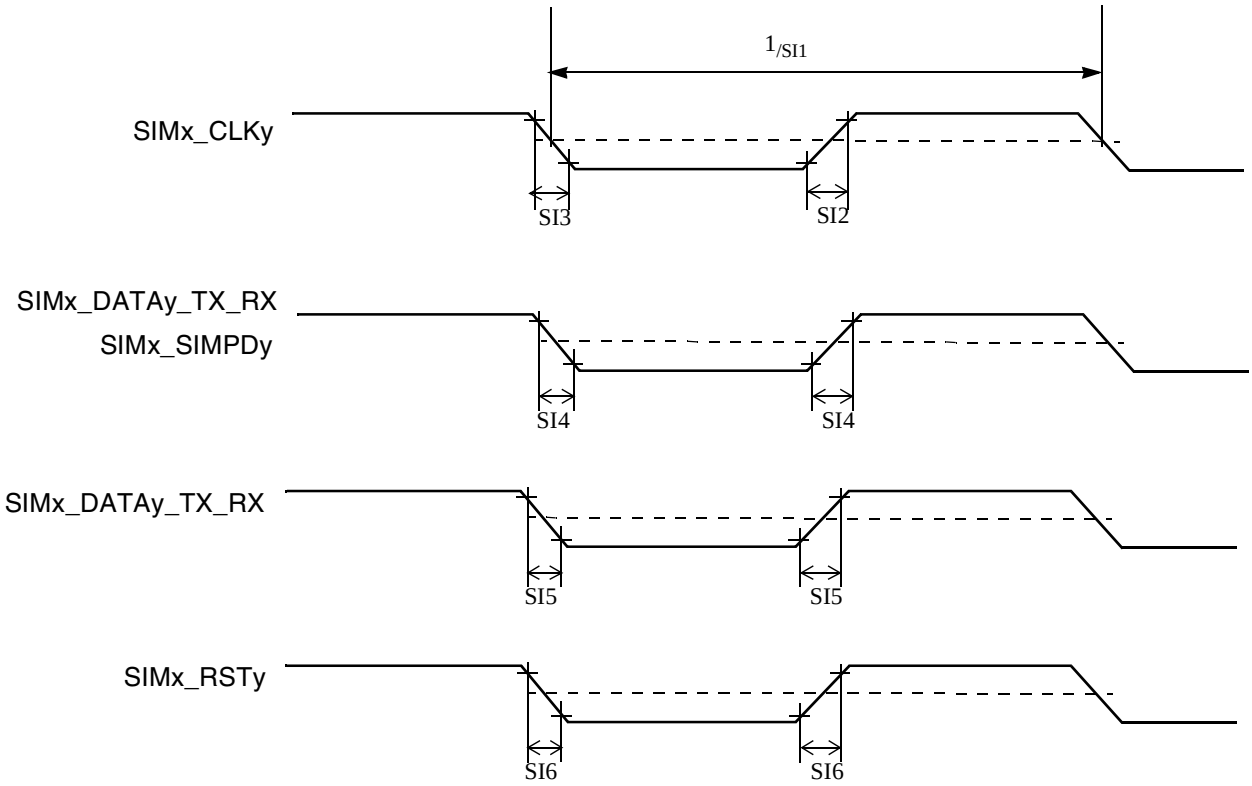

Figure 68. SIM Clock Timing Diagram

Table 74 defines the general timing requirements for the SIM interface.

Table 74. Timing Specifications, High Drive Strength

ID	Parameter	Symbol	Min.	Max.	Unit
SI1	SIM clock frequency (SIMx_CLKy)[1]	S_{freq}	0.01	25	MHz
SI2	SIM clock rise time (SIMx_CLKy)[2]	S_{rise}	—	$0.09 \times (1/S_{freq})$	ns
SI3	SIM clock fall time (SIMx_CLKy)[3]	S_{fall}	—	$0.09 \times (1/S_{freq})$	ns
SI4	SIM input transition time (SIMx_DATAy_RX_TX, SIMx_SIMPDy)	S_{trans}	10	25	ns
SI5	SIM I/O rise time / fall time (SIMx_DATAy_RX_TX)[4]	Tr/Tf	—	1	µs
SI6	SIM RST rise time / fall time (SIMx_RSTy)[5]	Tr/Tf	—	1	µs

1 50% duty cycle clock,
2 With C = 50 pF
3 With C = 50 pF
4 With Cin = 30 pF, Cout = 30 pF,
5 With Cin = 30 pF,

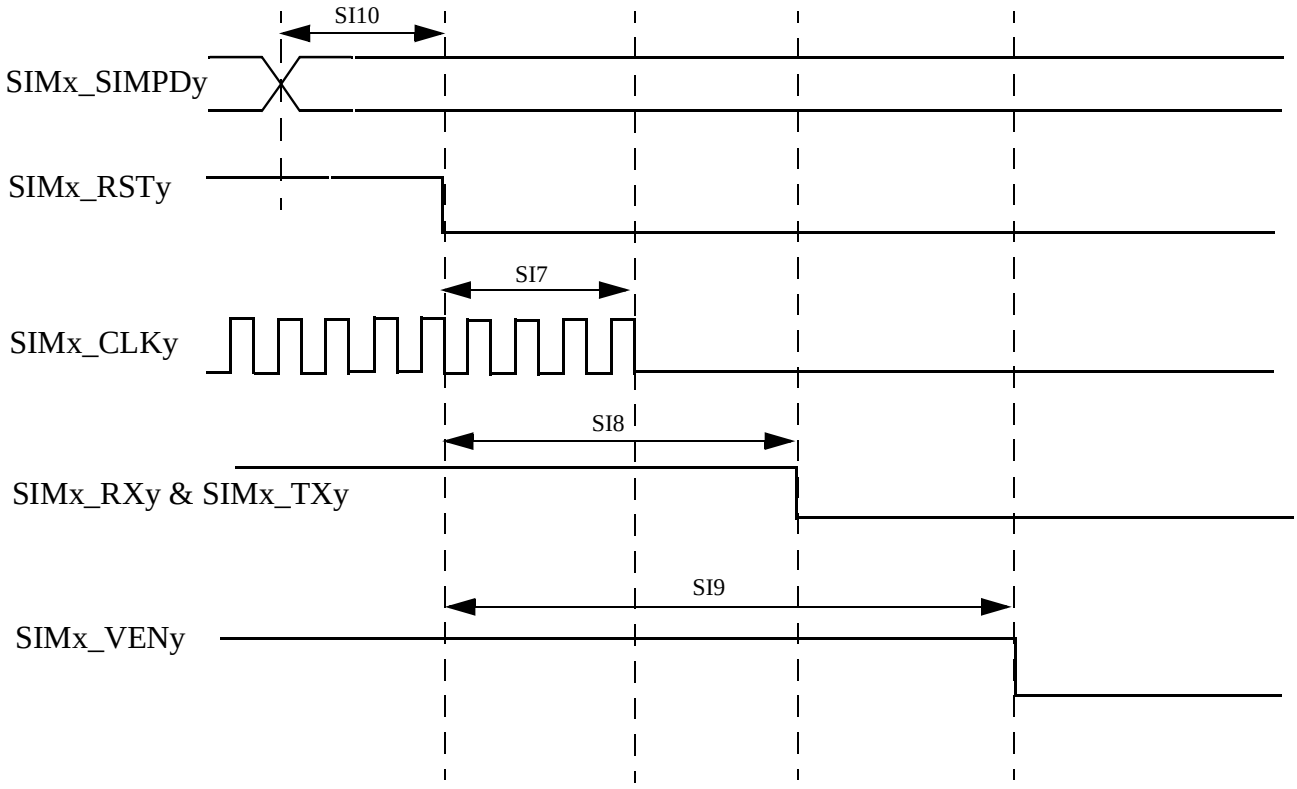

Figure 71. SmartCard Interface Power Down AC Timing

Table 77. Timing Requirements for Power-down Sequence

ID	PARAMETER	SYMBOL	Min.	Max.	Unit
SI7	SIM reset to SIM clock stop	$S_{rst2clk}$	0.9 × 1/Fckil	1.1 × 1/Fckil	ns
SI8	SIM reset to SIM Tx data low	$S_{rst2dat}$	1.8 × 1/Fckil	2.2 × 1/Fckil	ns
SI9	SIM reset to SIM voltage enable low	$S_{rst2ven}$	2.7 × 1/Fckil	3.3 × 1/Fckil	ns
SI10	SIM presence detect to SIM reset low	S_{pd2rst}	0.9 × 1/Fckil	1.1 × 1/Fckil	ns

3.7.15 System JTAG Controller (SJC) Timing

Figure 72 through Figure 75 show respectively the test clock input, boundary scan, test access port, and $\overline{\text{TRST}}$ timings for the SJC. Table 78 describes the SJC timing parameters (SJ1–SJ13) indicated in the figures.

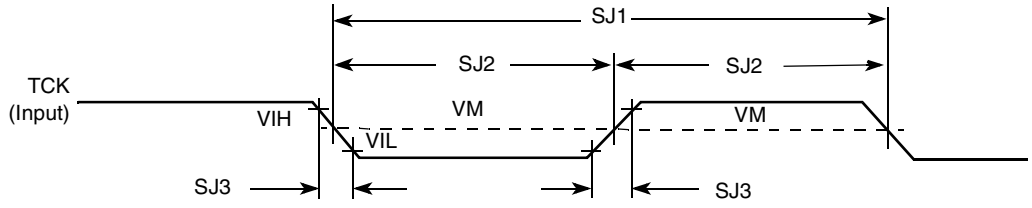

Figure 72. Test Clock Input Timing Diagram

3.7.16 Smart Liquid Crystal Display Controller (SLCDC)

Figure 76 and Figure 77 show SLCDC timing for serial and parallel transfers respectively. Table 79 and Table 80 describe the timing parameters shown in the respective figures.

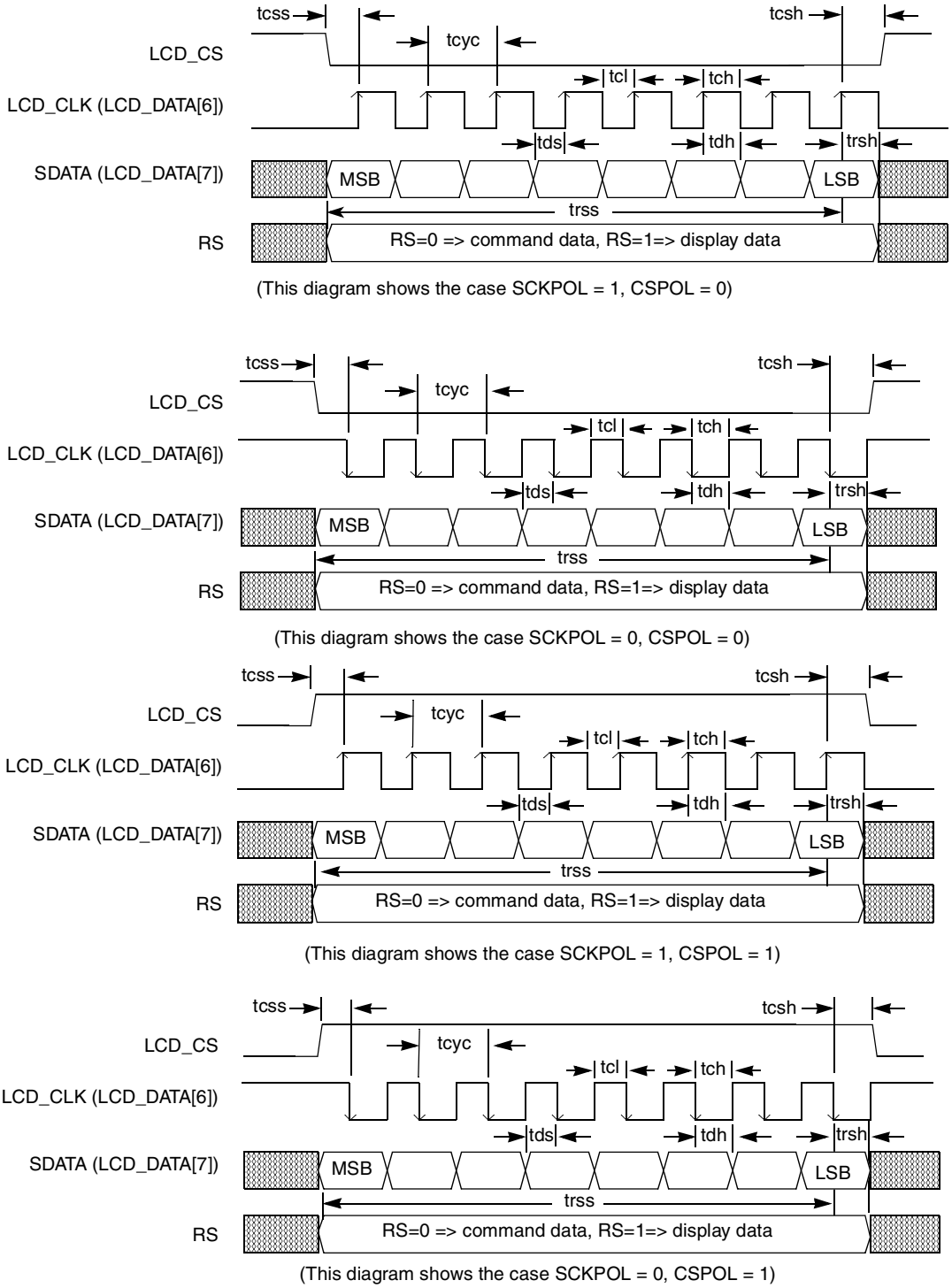

Figure 76. SLCDC Timing Diagram—Serial Transfers to LCD Device

- ”Tx” and “Rx” refer, respectively, to the transmit and receive sections of the SSI.
- For internal frame sync operation using external clock, the FS timing is the same as that of Tx data (for example, during AC97 mode of operation).

3.7.18 Touchscreen ADC Electrical Specifications and Timing

This section describes the electrical specifications, operation modes, and timing of the touchscreen ADC.

3.7.18.1 ADC Electrical Specifications

Table 85 shows the electrical specifications for the touchscreen ADC.

Table 85. Touchscreen ADC Electrical Specifications

Parameter	Conditions	Min.	Typ.	Max.	Unit
ADC					
Input sampling capacitance (C_S)	No pin/pad capacitance included	—	2	—	pF
Resolution	—		12		bits
Analog Bias					
Resistance value between *ref* and *agndref*	—	—	1.6	—	kΩ
Timing Characteristics					
Sampling rate (fs)	—	—	—	125	kHz
Internal ADC/TSC clock frequency	—	—	—	1.75	MHz
Multiplexed inputs	—		8		—
Data latency	—		12.5		clk cycles
Power-up time[1]	—		14		clk cycles
clk falling edge to sampling delay (tsd)	—	2	5	8	ns
soc input setup time before clk rising edge (tsocst)	—	0.5	1	3	ns
soc input hold time after clk rising edge (tsochld)	—	2	3	6	ns
eoc delay after clk rise edge (teoc)	With a 250 pF load	2	7	10	ns
Valid data out delay after eoc rise edge (tdata)	With a 250 pF load	5	8	13	ns
Power Supply Requirements					
Current consumption[2] NVCC_ADC QV_{DD}	—	—	—	2.1 0.5	mA mA

Table 104. Revision History (continued)

Rev. Number	Date	Substantive Change(s)
Rev. 6	—	This revision number was skipped so the Consumer/Industrial and Automotive revision numbers can be in sync.
Rev. 5	09/2010	• Added Section 3.2.3, “SRTC DryIce Power-Up/Down Sequence.”
Rev. 4	08/2010	• Updated Table 56, "WEIM Bus Timing Parameters," on page 69 to include new row for WE19. • Updated Table 6, "DC Operating Conditions," on page 11 to include Min and Max values of FUSE_VDD.
Rev. 3	06/2010	• Updated Table 1, “Ordering Information,” to include new part numbers.
Rev. 2	03/2010	• Updated Table 1, “Ordering Information,” to include new part numbers. • Added Table 2, “i.MX25 Parts Functional Differences.” • Added Section 3.3, “Power Characteristics.”
Rev. 1	10/2009	• Updated Table 1, “Ordering Information,” to include new part numbers. • Updated DRYICE description in Table 3, “i.MX25 Digital and Analog Modules.” • Updated REF signal description in Table 4, “Signal Considerations.” • Updated ESD damage immunity values in Table 5, “DC Absolute Maximum Ratings.” • Updated values in Table 13, “i.MX25 Power Mode Current Consumption.” • Added a note on timing in Section 3.2.1, “Power-Up Sequence.” • Added Table 14, “iMX25 Reduced Power Mode Current Consumption.” • Updated Table 55, “NFC Timing Parameters.” • Updated values in Table 56, “WEIM Bus Timing Parameters. • Updated Table 85, “Touchscreen ADC Electrical Specifications.”
Rev. 0	6/2009	Initial release.