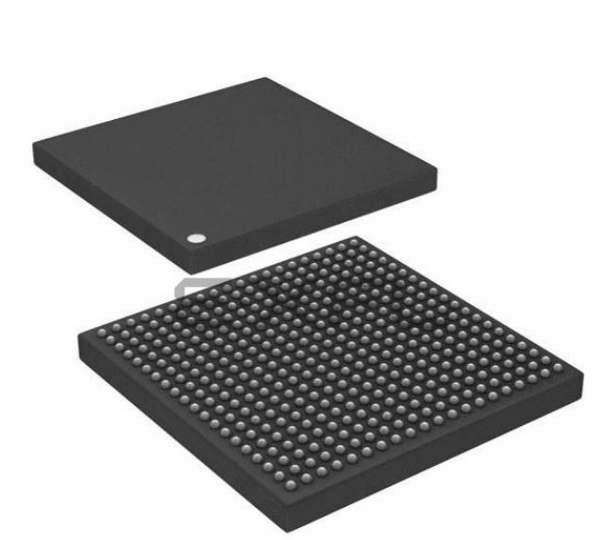

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM926EJ-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	LPDDR, DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	Keypad
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	2.0V, 2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	Boot Security, Cryptography, Secure Fusebox, Secure JTAG, Secure Memory, Tamper Detection
Package / Case	400-LFBGA
Supplier Device Package	400-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx251ajm4a

NOTE

- The user is advised to connect FUSEVDD to GND except when fuses are programmed, to prevent unintentional blowing of fuses.
- Other power-up sequences may be possible; however, the above sequence has been verified and is recommended.
- There is a 1 ms minimum time between supplies coming up, and a 1 ms minimum time between POR_B assert and de-assert.
- The dV/dT should be no faster than 0.25 V/µs for all power supplies, to avoid triggering ESD circuit.

Figure 2 shows the power-up sequence diagram. After POR_B is asserted, Core VDD and NVDDx can be powered up. After Core VDD and NVDDx are stable, the analog supplies can be powered up.

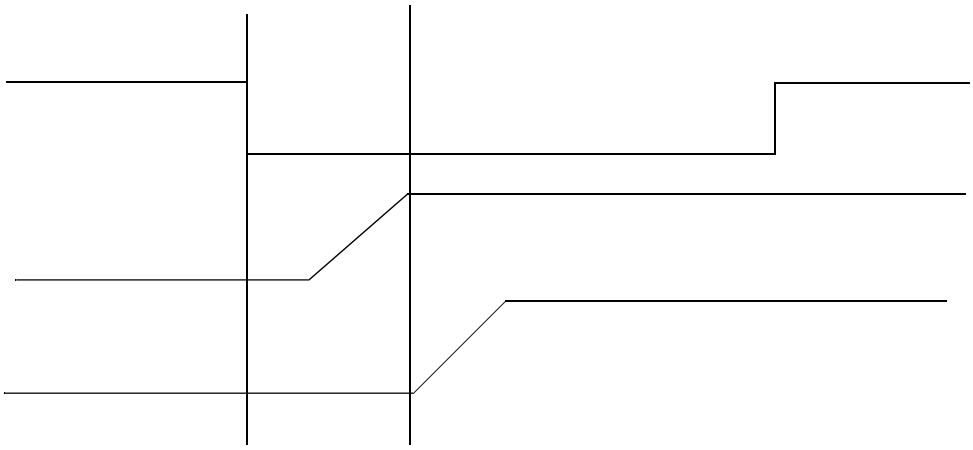


Figure 2. Power-Up Sequence Diagram

3.2.2 Power-Down Sequence

There are no special requirements for the power-down sequence. All power supplies can be shut down at the same time.

3.2.3 SRTC DryIce Power-Up/Down Sequence

In order to guarantee DryIce power-loss protection, including retention of SRTC time data during power down, users must do the following:

- Place a proper capacitor on the NVCC_DRYICE output pin, and
- Implement the below power-up/down sequence

1. Assert power on reset (POR).
2. Turn on NVCC_CRM.
3. Turn on QVDD digital logic domain supplies for not less than 1 ms and not more than 32 ms, after NVCC_CRM reaches 90% of 3.3 V.

Table 23. Fast I/O AC Parameters for OVDD = 3.0–3.6 V (continued)

Input Pad Propagation Delay with Hysteresis, 40%–60%[4]	tpi	1.6pF	1.353/1.457	1.637/1.659	2.163/1.991	ns
Input Pad Transition Times without Hysteresis[4]	trfi	1.6pF	0.16/0.12	0.23/0.18	0.33/0.29	ns
Input Pad Transition Times with Hysteresis[4]	trfi	1.6pF	0.16/0.13	0.22/0.18	0.33/0.29	ns
Maximum Input Transition Times[5]	trm	—	—	—	—	ns

1 Maximum condition for tpr, tpo, and tpv: wcs model, 1.1 V, IO 3.0 V and 105 °C. Minimum condition for tpr, tpo, and tpv: bcs model, 1.3 V, IO 3.6 V and –40 °C. Input transition time from core is 1ns (20%–80%).

2 Minimum condition for tps: wcs model, 1.1 V, IO 3.0 V and 105 °C. tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.

3 Maximum condition for tdit: bcs model, 1.3 V, IO 3.6 V and –40 °C.

4 Maximum condition for tpi and trfi: wcs model, 1.1 V, IO 3.0 V and 105 °C. Minimum condition for tpi and trfi: bcs model, 1.3 V, IO 3.6 V and –40 °C. Input transition time from pad is 5 ns (20%–80%).

5 Hysteresis mode is recommended for input with transition time greater than 25 ns.

3.6.3 DDR I/O AC Parameters

The DDR pad type is configured by the IOMUXC_SW_PAD_CTL_GRP_DDRTYPE register (see Chapter 4, “External Signals and Pin Multiplexing,” in the *i.MX25 Multimedia Applications Processor Reference Manual*).

3.6.3.1 DDR_TYPE = 00 Standard Setting I/O AC Parameters and Requirements

Table 24 shows AC parameters for mobile DDR I/O. These settings are suitable for mDDR and DDR2 1.8V (± 5%) applications.

Table 24. AC Parameters for Mobile DDR I/O

Parameter	Symbol	Load Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	50	60	%
Clock frequency[1]	f	—	—	—	133	MHz
Output pad transition times[1] (max. drive)	tpr	25 pF 50 pF	0.52/0.51 0.98/0.96	0.79/0.72 1.49/1.34	1.25/1.09 2.31/1.98	ns
Output pad transition times[1] (high drive)	tpr	25 pF 50 pF	1.13/1.10 2.15/2.10	1.74/1.55 3.28/2.92	2.71/2.30 5.11/4.31	ns
Output pad transition times[1] (standard drive)	tpr	25 pF 50 pF	2.26/2.19 4.30/4.18	3.46/3.07 6.59/5.79	5.39/4.56 10.13/8.55	ns
Output pad propagation delay[1] (max. drive), 50%–50%	tpo	15 pF 35 pF	0.80/1.03 1.06/1.32	1.36/1.50 1.76/1.90	2.21/2.40 2.83/2.82	ns
Output pad propagation delay[1] (high drive), 50%–50%	tpo	15 pF 35 pF	1.04/1.27 1.63/1.90	1.74/1.83 2.63/2.69	2.79/2.70 4.18/3.86	ns
Output pad propagation delay[1] (standard drive), 50%–50%	tpo	15 pF 35 pF	1.55/1.80 2.72/3.06	2.53/2.57 4.31/4.29	4.03/3.76 6.80/6.19	ns
Output pad propagation delay[1] (max. drive), 40%–60%	tpo	15 pF 35 pF	0.80/0.91 1.06/1.12	1.44/1.59 1.76/1.91	2.24/2.29 2.74/2.75	ns

Table 24. AC Parameters for Mobile DDR I/O (continued)

Parameter	Symbol	Load Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Output pad propagation delay[1] (high drive), 40%–60%	tpo	15 pF 35 pF	1.04/1.09 1.63/1.56	1.73/1.83 2.43/2.52	2.69/2.62 3.79/3.62	ns
Output pad propagation delay[1] (standard drive), 40%–60%	tpo	15 pF 35 pF	1.50/1.74 2.73/2.42	2.36/2.41 3.77/3.78	3.67/3.46 5.86/5.37	ns
Output enable to output valid delay[1] (max. drive), 50%–50%	tpv	15 pF 35 pF	1.17/1.01 1.43/1.30	1.93/1.61 2.33/2.00	3.06/2.55 3.69/3.13	ns
Output enable to output valid delay[1] (high drive), 50%–50%	tpv	15 pF 35 pF	1.38/1.28 1.97/1.92	2.25/1.99 3.16/2.86	3.58/3.10 5.01/4.39	ns
Output enable to output valid delay[1] (standard drive), 50%–50%	tpv	15 pF 35 pF	1.92/1.57 3.12/3.16	3.11/2.79 4.97/4.59	4.98/4.13 7.97/6.98	ns
Output enable to output valid delay[1] (max. drive), 40%–60%	tpv	15 pF 35 pF	1.28/1.12 1.49/1.36	2.01/1.70 2.33/2.01	3.09/2.60 3.60/3.06	ns
Output enable to output valid delay[1] (high drive), 40%–60%	tpv	15 pF 35 pF	1.43/1.33 1.90/1.84	2.24/1.99 2.96/2.68	3.47/3.02 4.59/4.03	ns
Output enable to output valid delay[1] (standard drive), 40%–60%	tpv	15 pF 35 pF	1.85/1.78 2.80/2.81	2.91/2.62 4.37/4.53	4.54/3.96 6.88/6.05	ns
Output pad slew rate[2] (max. drive)	tps	25 pF 50 pF	0.80/0.92 0.43/0.50	1.35/1.50 0.72/0.81	2.23/2.27 1.66/1.68	V/ns
Output pad slew rate[2] (high drive)	tps	25 pF 50 pF	0.37/0.43 0.19/0.23	0.62/0.70 0.33/0.37	1.03/1.05 0.75/0.77	V/ns
Output pad slew rate[2] (standard drive)	tps	25 pF 50 pF	0.18/0.22 0.10/0.12	0.31/0.35 0.16/0.18	0.51/0.53 0.38/0.39	V/ns
Output pad dI/dt[3] (max. drive)	tdit	25 pF 50 pF	64 69	171 183	407 432	mA/ns
Output pad dI/dt[3] (high drive)	tdit	25 pF 50 pF	37 39	100 106	232 246	mA/ns
Output pad di/dt[3] (standard drive)	tdit	25 pF 50 pF	18 20	50 52	116 123	mA/ns
Input pad transition times[4]	trfi	1.0 pF	0.07/0.08	0.11/0.13	0.16/0.20	ns
Input pad propagation delay, 50%–50%[4]	tpi	1.0 pF	0.77/1.00	1.22/1.45	1.89/2.21	ns
Input pad propagation delay, 40%–60%[4]	tpi	1.0 pF	1.59/1.82	2.04/2.27	2.69/3.01	ns

1 Maximum condition for tpr, tpo, tpi, and tpv: wcs model, 1.1 V, I/O 1.65 V, and 105 °C. Minimum condition for tpr, tpo, and tpv: bcs model, 1.3 V, I/O 1.95 V and –40 °C. Input transition time from core is 1 ns (20%–80%).

2 Minimum condition for tps: wcs model, 1.1 V, I/O 1.65 V, and 105 °C. tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.

3 Maximum condition for tdit: bcs model, 1.3 V, I/O 1.95 V, and –40 °C.

4 Maximum condition for tpi and trfi: wcs model, 1.1 V, I/O 1.65 V and 105 °C. Minimum condition for tpi and trfi: bcs model, 1.3 V, I/O 1.95 V and –40 °C. Input transition time from pad is 5 ns (20%–80%).

3.7 Module Timing and Electrical Parameters

This section contains the timing and electrical parameters for i.MX25 modules.

3.7.1 1-Wire Timing Parameters

Figure 7 shows the reset and presence pulses (RPP) timing for 1-Wire.

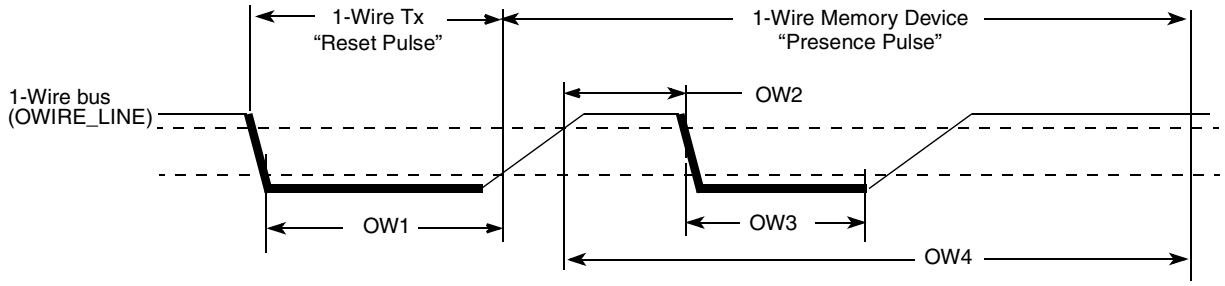


Figure 7. 1-Wire RPP Timing Diagram

Table 32 lists the RPP timing parameters.

Table 32. RPP Sequence Delay Comparisons Timing Parameters

ID	Parameters	Symbol	Min.	Typ.	Max.	Units
OW1	Reset Time Low	t_{RSTL}	480	511	—	µs
OW2	Presence Detect High	t_{PDH}	15	—	60	µs
OW3	Presence Detect Low	t_{PDL}	60	—	240	µs
OW4	Reset Time High	t_{RSTH}	480	512	—	µs

Figure 8 shows write 0 sequence timing, and Table 33 describes the timing parameters (OW5–OW6) that are shown in the figure.

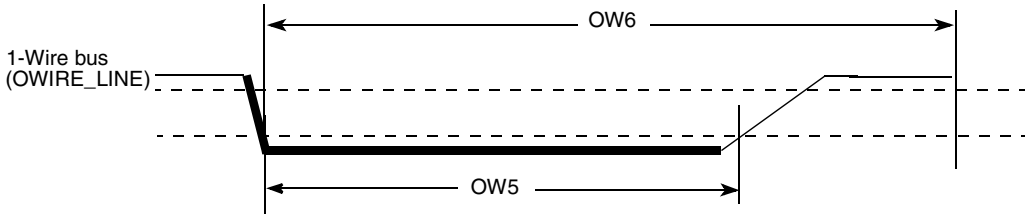


Figure 8. Write 0 Sequence Timing Diagram

Table 33. WR0 Sequence Timing Parameters

ID	Parameter	Symbol	Min.	Typ.	Max.	Units
OW5	Write 0 Low Time	t_{WR0_low}	60	100	120	µs
OW6	Transmission Time Slot	t_{SLOT}	OW5	117	120	µs

Figure 17 shows timing for device-terminated UDMA in-transfer.

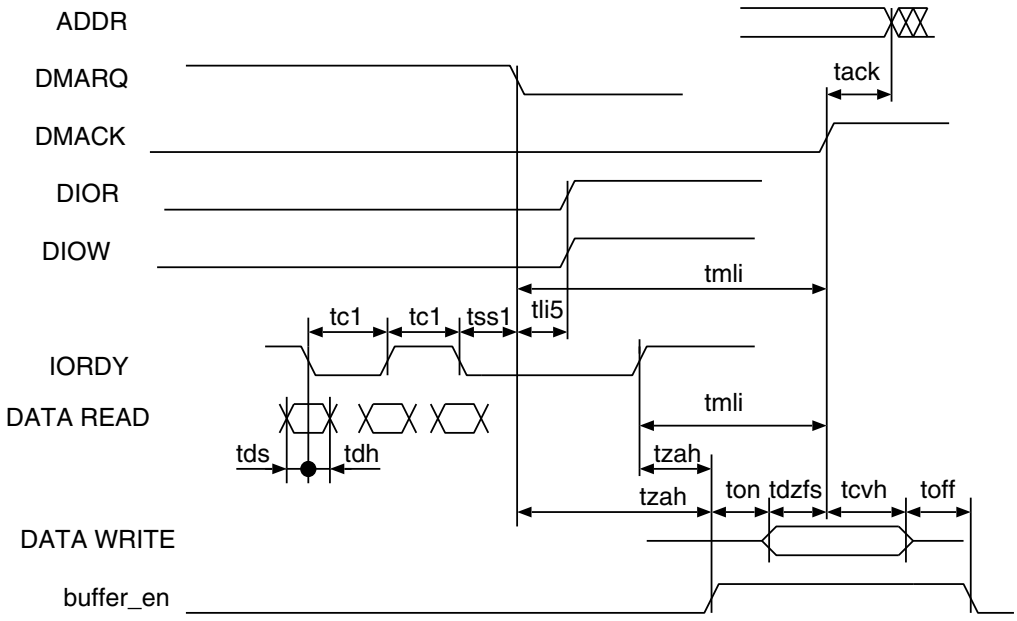


Figure 17. Timing for Device-Terminated UDMA Transfer

Timing parameters for UDMA in-burst are listed in Table 39.

Table 39. Timing Parameters for UDMA In-Burst

ATA Parameter	Spec. Parameter	Value	Required Conditions
tack	tack	tack(min.) = (time_ack × T) – (tskew1 + tskew2)	time_ack
tenv	tenv	tenv(min.) = (time_env × T) – (tskew1 + tskew2) tenv(max.) = (time_env × T) + (tskew1 + tskew2)	time_env
tds	tds1	tds – (tskew3) – ti_ds > 0	tskew3, ti_ds, ti_dh should be low enough
tdh	tdh1	tdh – (tskew3) –ti_dh > 0	
tcyc	tc1	(tcyc – tskew) > T	T big enough
trp	trp	trp(min.) = time_rp × T – (tskew1 + tskew2 + tskew6)	time_rp
—	tx1[1]	(time_rp × T) – (tco + tsu + 3T + 2 × tbuf + 2 × tcable2) > trfs (drive)	time_rp
tmli	tmli1	tmli1(min.) = (time_mlix + 0.4) × T	time_mlix
tzah	tzah	tzah(min.) = (time_zah + 0.4) × T	time_zah
tdzfs	tdzfs	tdzfs = (time_dzfs × T) – (tskew1 + tskew2)	time_dzfs
tcvh	tcvh	tcvh = (time_cvh × T) – (tskew1 + tskew2)	time_cvh
—	ton toff	ton = time_on × T – tskew1 toff = time_off × T – tskew1	—

[1] There is a special timing requirement in the ATA host that requires the internal DIOW to go only high three clocks after the last active edge on the DSTROBE signal. The equation given on this line tries to capture this constraint.

Make t_{on} and t_{off} big enough to avoid bus contention.

Table 44. DDR/SDR SDRAM Read Cycle Timing Parameters (continued)

ID	Parameter	Symbol	Min.	Max.	Unit
SD6	Address setup time	tAS	2.0	—	ns
SD7	Address hold time	tAH	1.8	—	ns
SD8	SDRAM access time	tAC	—	6.47	ns
SD9	Data out hold time[2]	tOH	1.2	—	ns
SD10	Active to read/write command period	tRC	10	—	clock

1 SD1 + SD2 does not exceed 7.5 ns for 133 MHz.

2 Timing parameters are relevant only to SDR SDRAM. For the specific DDR SDRAM data related timing parameters, see Table 48 and Table 49.

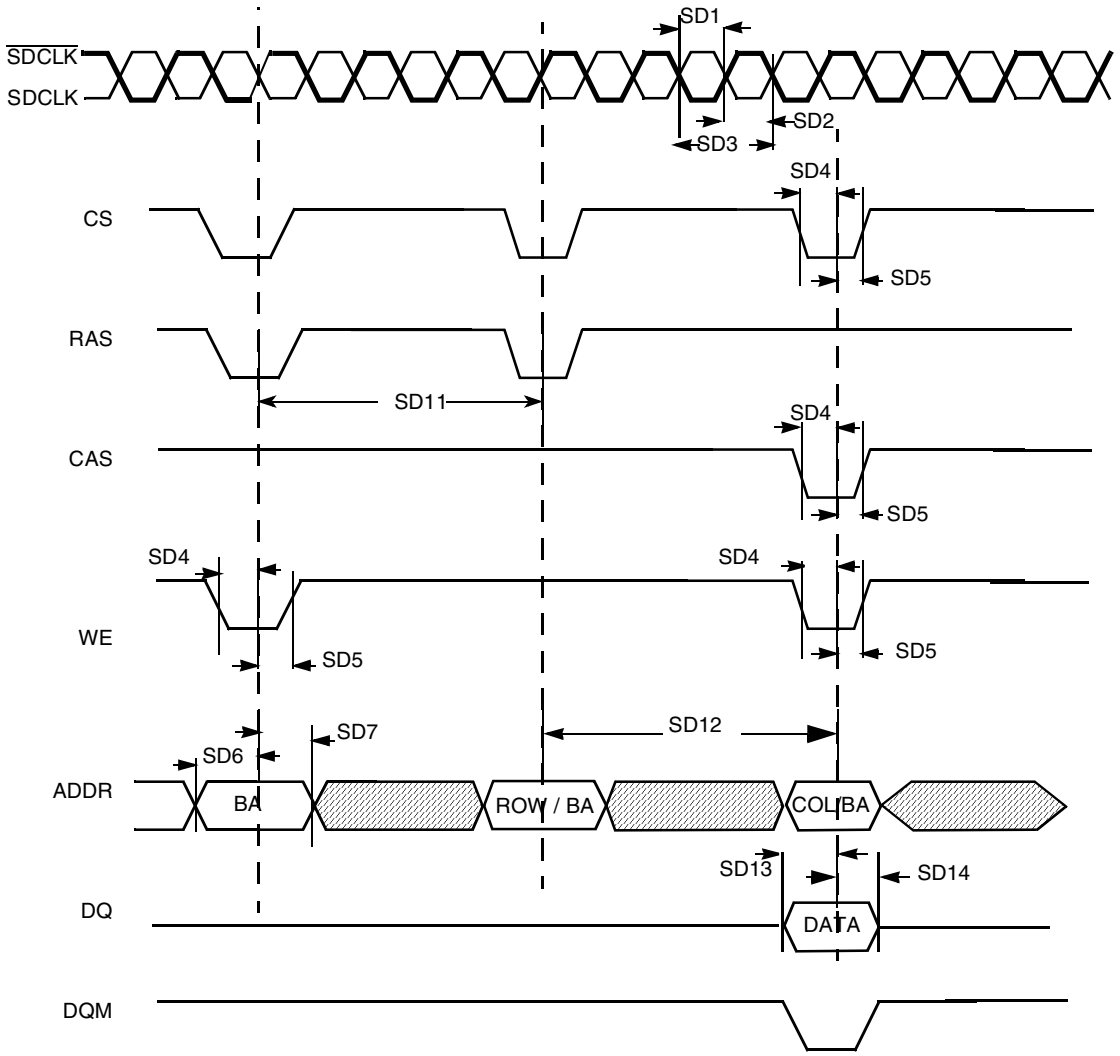


Figure 26. SDR SDRAM Write Cycle Timing Diagram

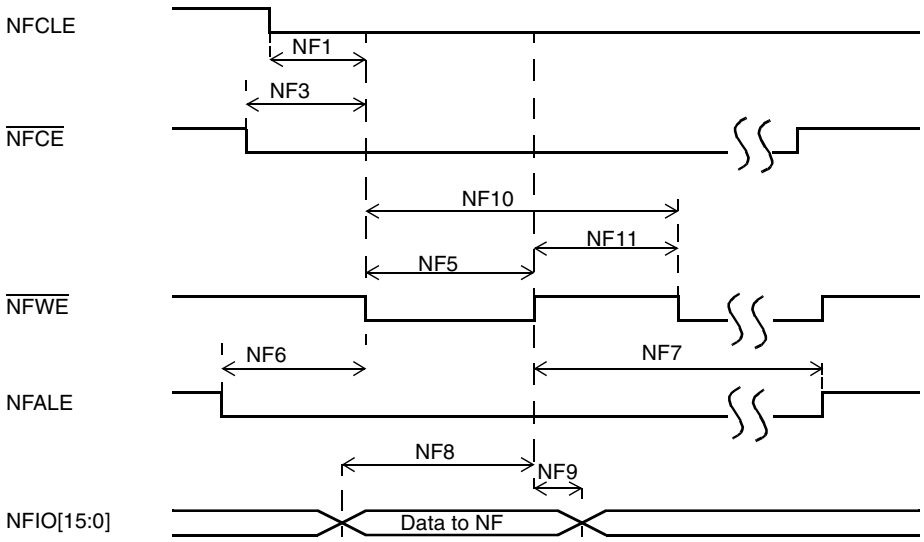


Figure 36. Write Data Latch Cycle Timing Diagram

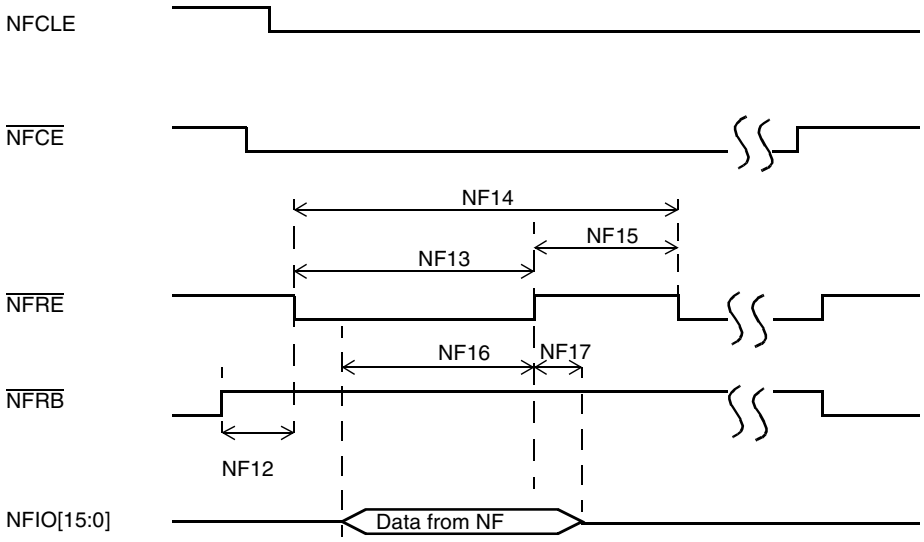


Figure 37. Read Data Latch Cycle Timing Diagram

Table 55. NFC Timing Parameters[1]

ID	Parameter	Symbol	Timing T = NFC Clock Cycle		Example Timing for NFC Clock ≈ 33 MHz T = 30 ns		Unit
			Min.	Max.	Min.	Max.	
NF1	NFCLE setup time	tCLS	T–1.0 ns	—	29	—	ns
NF2	NFCLE hold time	tCLH	T–2.0 ns	—	28	—	ns
NF3	$\overline{\text{NFCE}}$ setup time	tCS	2T–5.0 ns	—	55	—	ns
NF4	$\overline{\text{NFCE}}$ hold time	tCH	7T–5.0 ns	—	205	—	ns

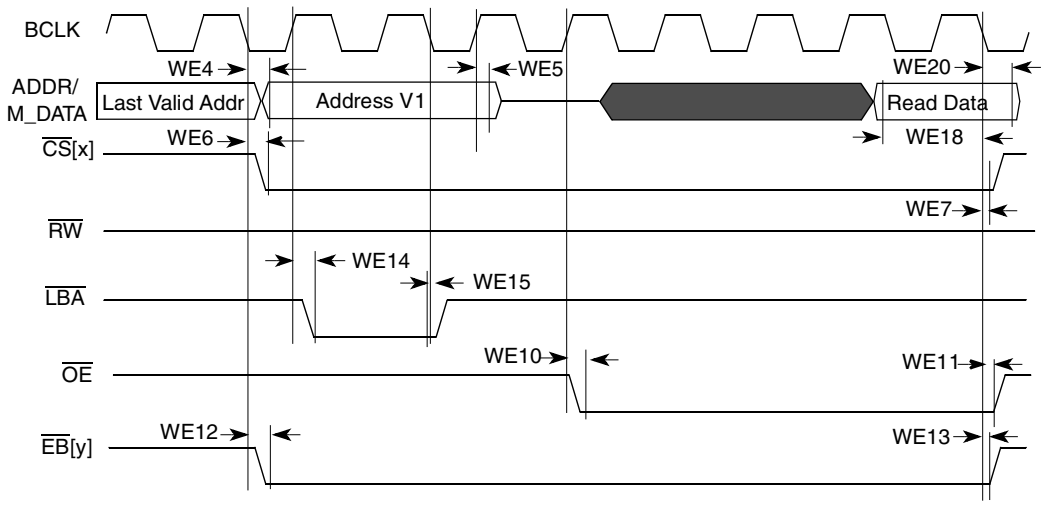


Figure 44. Muxed A/D Mode Timing Diagram for Synchronous Read Access—WSC=7, LBA=1, LBN=1, LAH=1, OEA=7

Figure 45 through Figure 49, and Table 57 help to determine timing parameters relative to chip select (CS) state for asynchronous and DTACK WEIM accesses with corresponding WEIM bit fields and the timing parameters mentioned above.

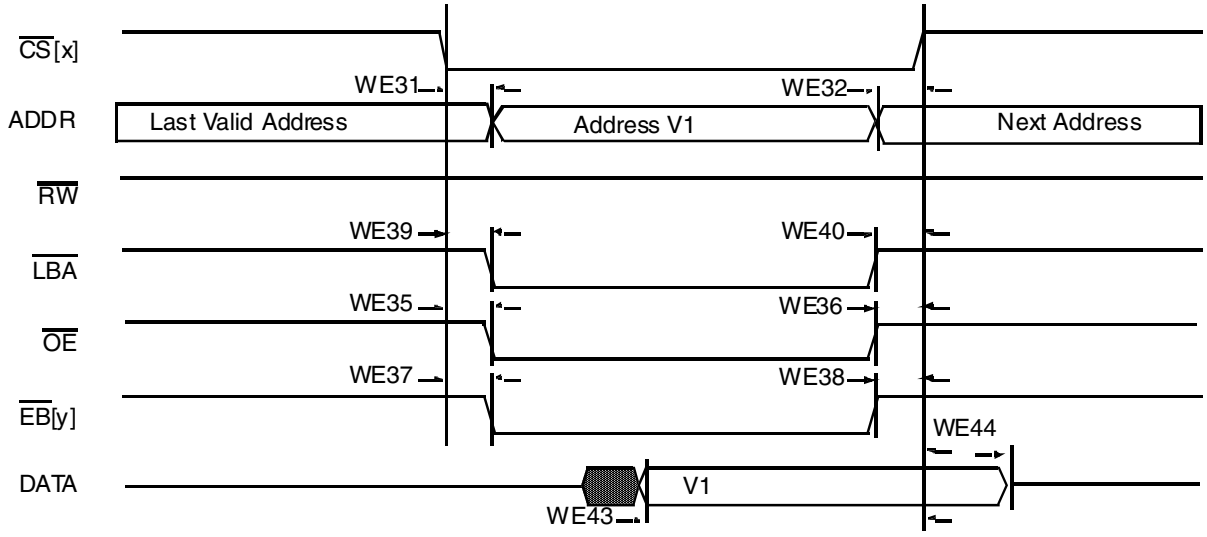


Figure 45. Asynchronous Memory Read Access

3.7.10 Controller Area Network (FlexCAN) Transceiver Parameters and Timing

Table 67 and Table 68 show voltage requirements for the FlexCAN transceiver Tx and Rx pins.

Table 67. Tx Pin Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units
High-level output voltage	V_{OH}	2	—	$Vcc^1 + 0.3$	V
Low-level output voltage	V_{OL}	—	0.8	—	V

1 Vcc = +3.3 V ± 5%

Table 68. Rx Pin Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units
High-level input voltage	V_{IH}	$0.8 \times Vcc^1$	—	Vcc^1	V
Low-level input voltage	V_{IL}	—	0.4	—	V

1 Vcc = +3.3 V ± 5%

Figure 60 through Figure 63 show the FlexCAN timing, including timing of the standby and shutdown signals.

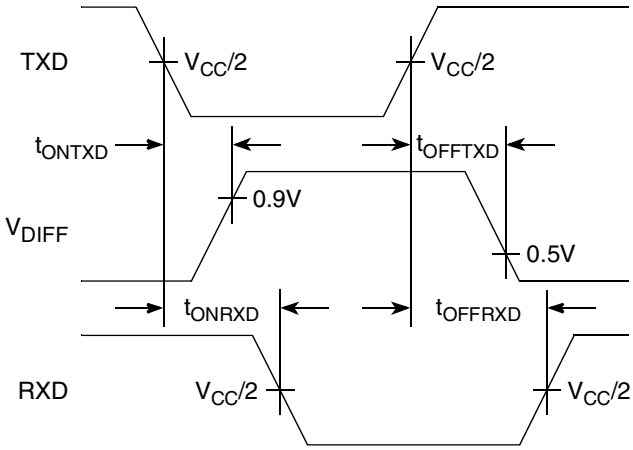


Figure 60. FlexCAN Timing Diagram

[1] A device must internally provide a hold time of at least 300 ns for I2DAT signal in order to bridge the undefined region of the falling edge of I2CLK.

[2] The maximum hold time has only to be met if the device does not stretch the LOW period (ID no IC5) of the I2CLK signal

[3] A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement of Set-up time (ID No IC7) of 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the I2CLK signal.

If such a device does stretch the LOW period of the I2CLK signal, it must output the next data bit to the I2DAT line max_rise_time(ID No IC9) + data_setup_time(ID No IC7) = 1000 + 250 = 1250 ns (according to the Standard-mode I2C-bus specification) before the I2CLK line is released.

[4] C_b = total capacitance of one bus line in pF.

Table 70. I2C Module Timing Parameters: 1.8 V +/– 0.10 V

ID	Parameter	Standard Mode		Unit
		Min.	Max.	
IC1	I2CLK cycle time	10	-	µs
IC2	Hold time (repeated) START condition	4.0	-	µs
IC3	Set-up time for STOP condition	4.0	-	µs
IC4	Data hold time	0[1]	3.45[2]	µs
IC5	HIGH Period of I2CLK Clock	4.0	-	µs
IC6	LOW Period of the I2CLK Clock	4.7	-	µs
IC7	Set-up time for a repeated START condition	4.7	-	µs
IC8	Data set-up time	250	-	ns
IC9	Bus free time between a STOP and START condition	4.7	-	µs
IC10	Rise time of both I2DAT and I2CLK signals	-	1000	ns
IC11	Fall time of both I2DAT and I2CLK signals	-	300	ns
IC12	Capacitive load for each bus line (C_b)	-	400	pF

[1] A device must internally provide a hold time of at least 300 ns for I2DAT signal in order to bridge the undefined region of the falling edge of I2CLK.

[2] The maximum hold time has only to be met if the device does not stretch the LOW period (ID no IC5) of the I2CLK signal

Table 82. SSI Receiver Timing with Internal Clock (continued)

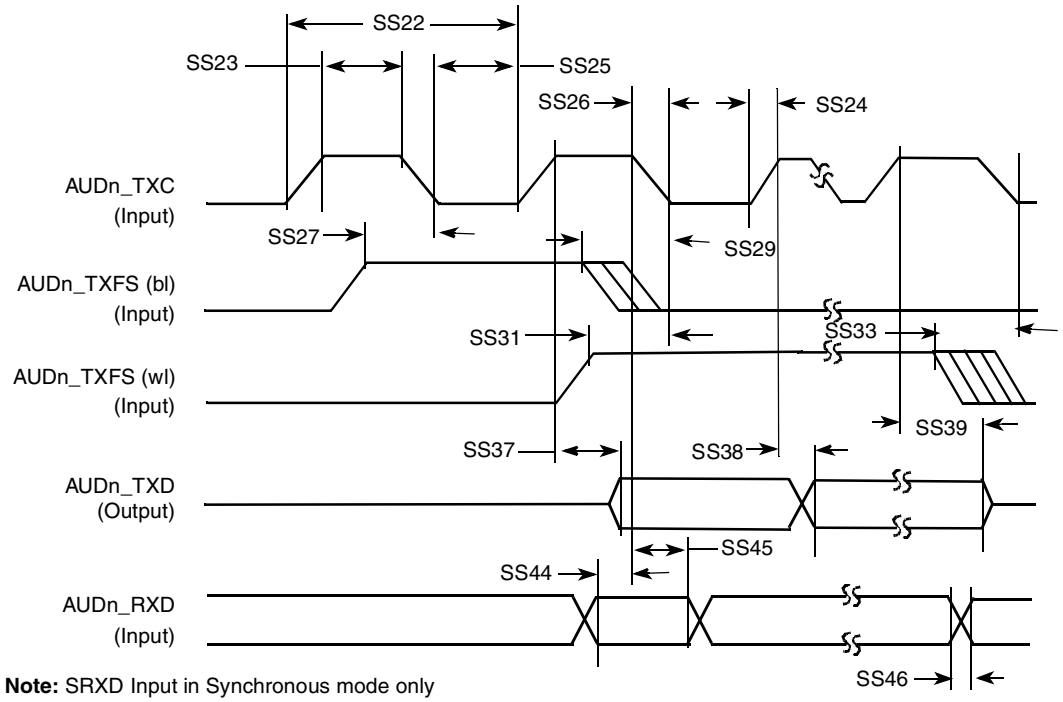
ID	Parameter	Min.	Max.	Unit
SS48	Oversampling clock high period	6.0	—	ns
SS49	Oversampling clock rise time	—	3.0	ns
SS50	Oversampling clock low period	6.0	—	ns
SS51	Oversampling clock fall time	—	3.0	ns

Note:

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on pads when SSI is being used for a data transfer.
- ”Tx” and “Rx” refer to the transmit and receive sections of the SSI.
- For internal frame sync operation using external clock, the FS timing is the same as that of Tx Data (for example, during AC97 mode of operation).

3.7.17.3 SSI Transmitter Timing with External Clock

Figure 80 shows the timing for the SSI transmitter with external clock. Table 83 describes the timing parameters (SS22-SS46) shown in the figure.



Note: SRXD Input in Synchronous mode only

Figure 80. SSI Transmitter with External Clock Timing Diagram

assertion of *soc* is detected. Thus, if the *soc* signal is continuously asserted, the ADC undergoes successive conversion cycles and achieves the maximum sampling rate. If *soc* is negated, no conversion is initiated.

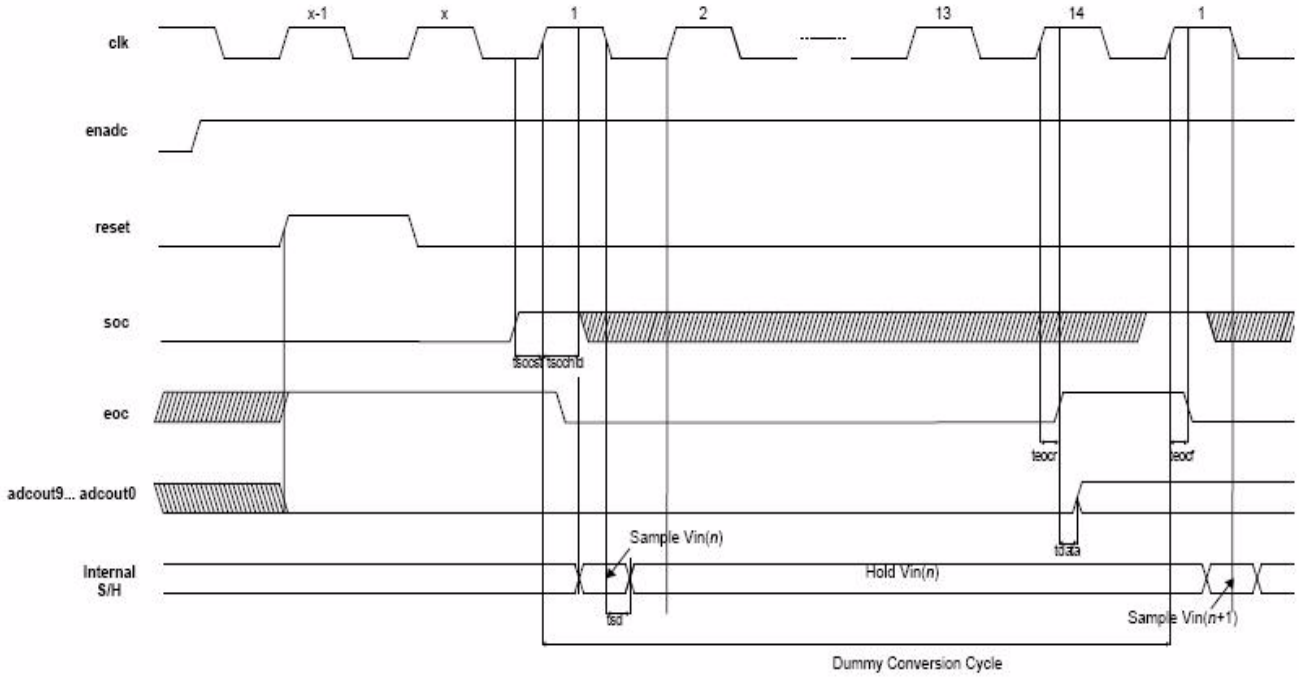


Figure 82. Start-up Sequence

The output data can be read from *adcout11...adcout0*, and is available *tdata* nanoseconds after the rising edge of *eoc*. The *reset* signal and the digital signals controlling the analog switches (*ypsw, xpsw, ynsw, xnsw*) are totally asynchronous.

The following conditions are necessary to guarantee the correct operation of the ADC:

- The input multiplexer selection (*selin11…selin0*) is stable during both the last clock cycle (14^{th}) and the first clock cycle (1^{st}). The best way to guarantee this is to make the input multiplexer selection during clock cycles 2 to 13.
- The references are stable during clock cycle 1 to 13. The best way to guarantee this is to make the reference multiplexer selection (*selrefp* and *selrefn*) before issuing an *soc* pulse and changing it only after an *eoc* pulse has been acquired, during the last clock cycle (14).

Figure 84 represents the usage of the ADC with idle cycles between conversions. This diagram is valid for any value of *N* equal or greater than 1.

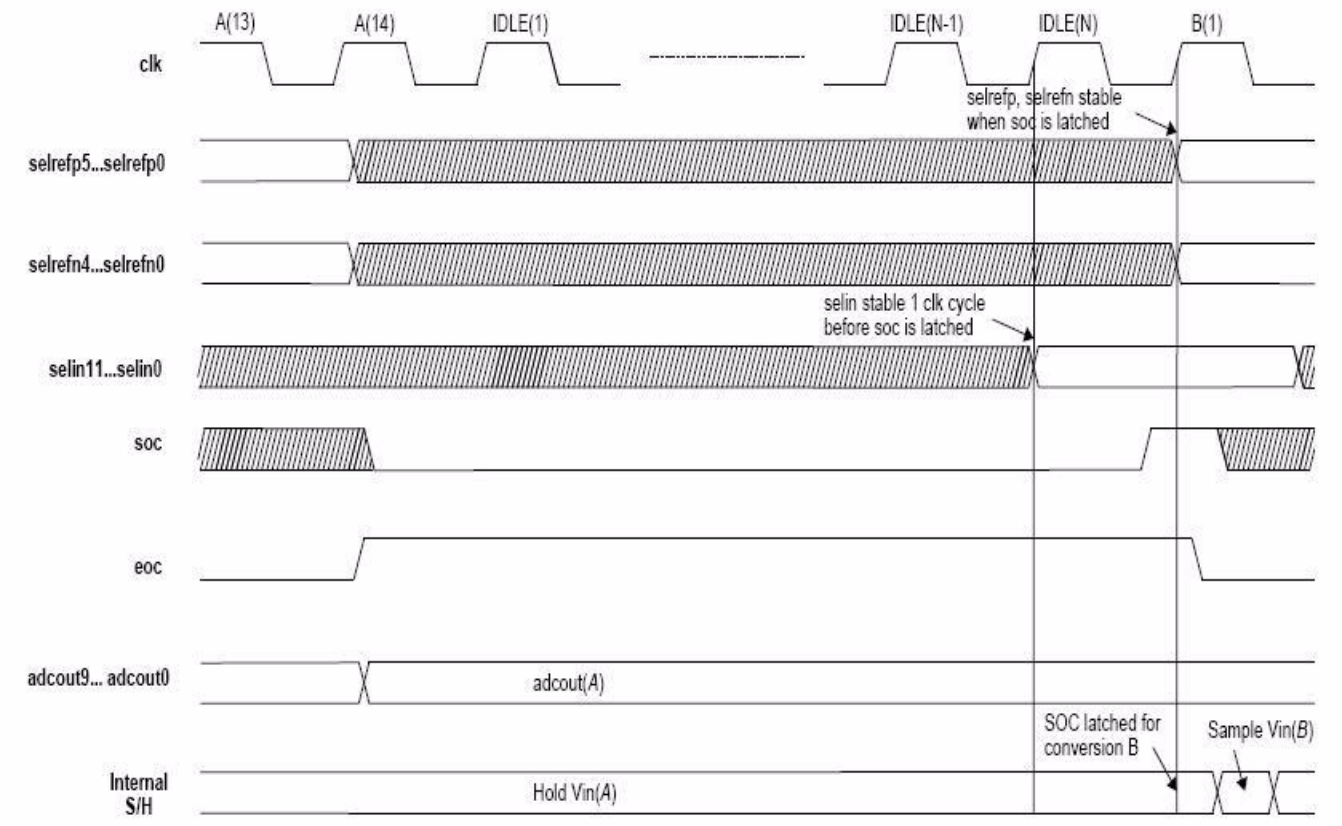


Figure 84. ADC Usage with Idle Cycles Between Conversions

3.7.19 UART Timing

This section describes the timing of the UART module in serial and parallel mode.

3.7.19.2 UART Infrared (IrDA) Mode Timing

The following subsections describe the UART transmit and receive timing in IrDA mode.

3.7.19.2.3 UART IrDA Mode Transmit Timing

Figure 87 depicts the UART transmit timing in IrDA mode, showing only 8 data bits and 1 stop bit. Table 88 describes the timing parameters (UA3–UA4) shown in the figure.

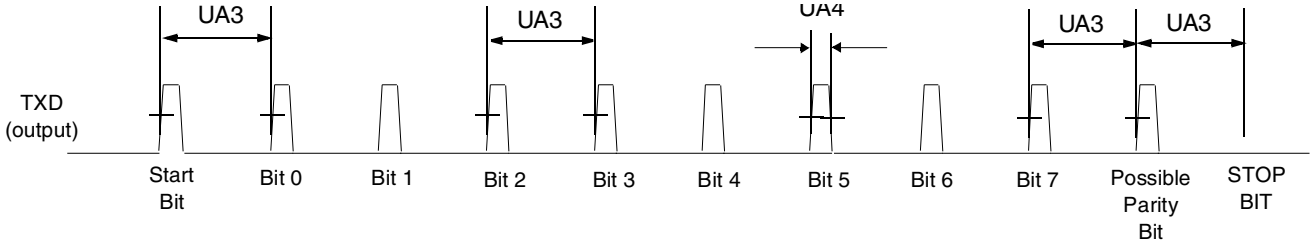


Figure 87. UART IrDA Mode Transmit Timing Diagram

Table 88. UART IrDA Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
UA3	Transmit bit time in IrDA mode	t_{TIRbit}	$1/F_{baud\_rate}$[1] – T_{ref_clk}[2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—
UA4	Transmit IR pulse duration	$t_{TIRpulse}$	$(3/16) \times (1/F_{baud\_rate}) - T_{ref\_clk}$	$(3/16) \times (1/F_{baud\_rate}) + T_{ref\_clk}$	—

1 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

2 T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

3.7.19.2.4 UART IrDA Mode Receive Timing

Figure 88 shows the UART receive timing for IrDA mode, for a format of 8 data bits and 1 stop bit. Table 89 describes the timing parameters (UA5–UA6) shown in the figure.

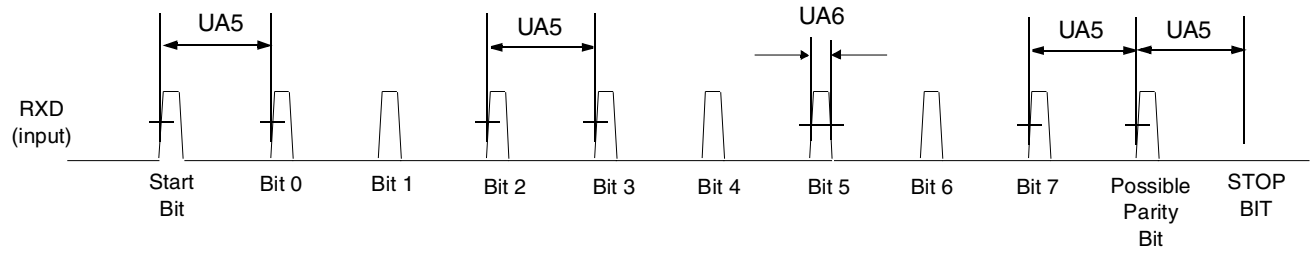


Figure 88. UART IrDA Mode Receive Timing Diagram

Table 89. UART IrDA Mode Receive Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
UA5	Receive bit time[1] in IrDA mode	t_{RIRbit}	$1/F_{baud\_rate}$[2] – $1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$	—
UA6	Receive IR pulse duration	$t_{RIRpulse}$	1.41 µs	$(5/16) \times (1/F_{baud\_rate})$	—

1 The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.

[2] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

3.7.20 USBOTG Timing

This section describes timing for the USB OTG port and host ports. Both serial and parallel interfaces are described.

3.7.20.1 USB Serial Interface Timing

The USB serial transceiver is configurable to four modes supporting four different serial interfaces:

- DAT_SE0 bidirectional, 3-wire mode
- DAT_SE0 unidirectional, 6-wire mode
- VP_VM bidirectional, 4-wire mode
- VP_VM unidirectional, 6-wire mode

The following subsections describe the timings for these four modes.

3.7.20.1.1 DAT_SE0 Bidirectional Mode Timing

Table 90 defines the DAT_SE0 bidirectional mode signals.

Table 90. Signal Definitions—DAT_SE0 Bidirectional Mode

Name	Direction	Signal Description
USB_TXOE_B	Out	Transmit enable, active low
USB_DAT_VP	Out In	Tx data when USB_TXOE_B is low Differential Rx data when USB_TXOE_B is high
USB_SE0_VM	Out In	SE0 drive when USB_TXOE_B is low SE0 Rx indicator when USB_TXOE_B is high

Figure 89 shows the USB transmit waveform in DAT_SE0 bidirectional mode diagram.

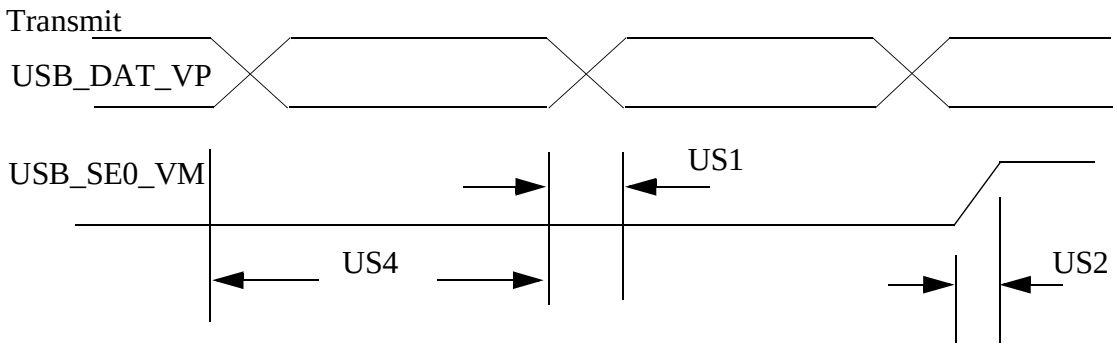


Figure 89. USB Transmit Waveform in DAT_SE0 Bidirectional Mode

3.7.20.1.3 VP_VM Bidirectional Mode Timing

Table 94 defines the VP_VM bidirectional mode signals.

Table 94. Signal Definitions—VP_VM Bidirectional Mode

Name	Direction	Signal Description
USB_TXOE_B	Out	• Transmit enable, active low
USB_DAT_VP	Out (Tx) In (Rx)	• Tx VP data when USB_TXOE_B is low • Rx VP data when USB_TXOE_B is high
USB_SE0_VM	Out (Tx) In (Rx)	• Tx VM data when USB_TXOE_B low • Rx VM data when USB_TXOE_B high
USB_RCV	In	• Differential Rx data

Figure 93 shows the USB transmit waveform in VP_VM bidirectional mode diagram.

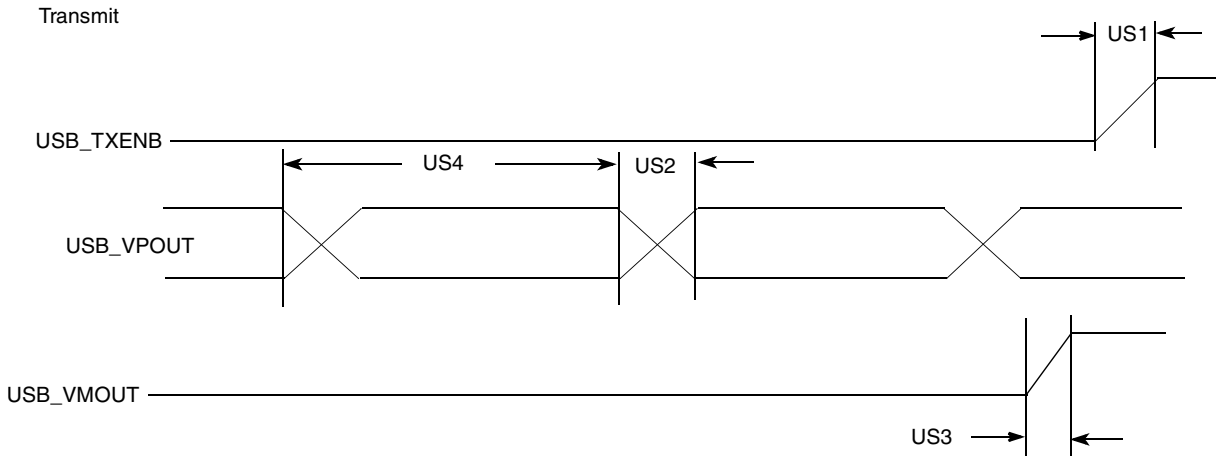


Figure 93. USB Transmit Waveform in VP_VM Bidirectional Mode

Figure 94 shows the USB receive waveform in VP_VM bidirectional mode diagram.

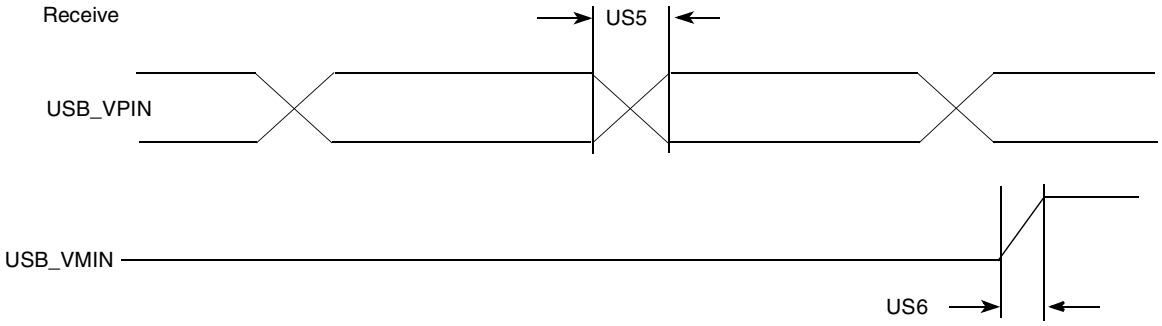


Figure 94. USB Receive Waveform in VP_VM Bidirectional Mode

Table 97 shows the timing specifications for USB in VP_VM unidirectional mode.

Table 97. USB Timing Specifications in VP_VM Unidirectional Mode

No.	Parameter	Signal	Direction	Min.	Max.	Unit	Conditions/ Reference Signal
US30	Tx rise/fall time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US31	Tx rise/fall time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US32	Tx rise/fall time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US33	Tx duty cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US34	Tx high overlap	USB_SE0_VM	Out	0.0	—	ns	USB_DAT_VP
US35	Tx low overlap	USB_SE0_VM	Out	—	0.0	ns	USB_DAT_VP
US36	Enable delay	USB_DAT_VP USB_SE0_VM	In	—	8.0	ns	USB_TXOE_B
US37	Disable delay	USB_DAT_VP USB_SE0_VM	In	—	10.0	ns	USB_TXOE_B
US38	Rx rise/fall time	USB_VP1	In	—	3.0	ns	35 pF
US39	Rx rise/fall time	USB_VM1	In	—	3.0	ns	35 pF
US40	Rx skew	USB_VP1	Out	–4.0	+4.0	ns	USB_SE0_VM
US41	Rx skew	USB_RCV	Out	–6.0	+2.0	ns	USB_DAT_VP

3.7.20.2 USB Parallel Interface Timing

Table 98 defines the USB parallel interface signals.

Table 98. Signal Definitions for USB Parallel Interface

Name	Direction	Signal Description
USB_Clk	In	Interface clock—All interface signals are synchronous to USB_Clk
USB_Data[7:0]	I/O	Bidirectional data bus, driven low by the link during idle—Bus ownership is determined by the direction
USB_Dir	In	Direction—Control the direction of the data bus
USB_Stp	Out	Stop—The link asserts this signal for one clock cycle to stop the data stream currently on the bus
USB_Nxt	In	Next—The PHY asserts this signal to throttle the data

Table 101. 17×17 mm Package i.MX25 Signal Contact Assignment (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuration after Reset[1]
LD2[2]	W7	LCDC	GPIO	OUTPUT	Low
LD3[2]	U8	LCDC	GPIO	OUTPUT	Low
LD4[2]	Y6	LCDC	GPIO	OUTPUT	Low
LD5[2]	V7	LCDC	GPIO	OUTPUT	Low
LD6[2]	W6	LCDC	GPIO	OUTPUT	Low
LD7[2]	Y5	LCDC	GPIO	OUTPUT	Low
LD8[2]	V6	LCDC	GPIO	OUTPUT	Low
LD9[2]	W5	LCDC	GPIO	OUTPUT	Low
LD10[2]	Y4	LCDC	GPIO	OUTPUT	Low
LD11[2]	Y3	LCDC	GPIO	OUTPUT	Low
LD12[2]	V5	LCDC	GPIO	OUTPUT	Low
LD13[2]	W4	LCDC	GPIO	OUTPUT	Low
LD14[2]	V4	LCDC	GPIO	OUTPUT	Low
LD15[2]	W3	LCDC	GPIO	OUTPUT	Low
HSYNC[2]	U7	LCDC	GPIO	OUTPUT	Low
VSYNC[2]	U6	LCDC	GPIO	OUTPUT	Low
LSCLK[2]	U5	LCDC	GPIO	OUTPUT	Low
OE_ACD[2]	V3	LCDC	GPIO	OUTPUT	Low
CONTRAST	U4	LCDC	GPIO	OUTPUT	Low
PWM[2]	W2	LCDC	GPIO	INPUT	100 KΩ Pull-Down
CSI_D2	F18	CSI	GPIO	INPUT	Keeper
CSI_D3	E19	CSI	GPIO	INPUT	Keeper
CSI_D4	F19	CSI	GPIO	INPUT	Keeper
CSI_D5	G18	CSI	GPIO	INPUT	Keeper
CSI_D6	E20	CSI	GPIO	INPUT	Keeper
CSI_D7	E18	CSI	GPIO	INPUT	Keeper
CSI_D8	G19	CSI	GPIO	INPUT	Keeper
CSI_D9	F20	CSI	GPIO	INPUT	Keeper
CSI_MCLK[2]	H18	CSI	GPIO	OUTPUT	Low
CSI_VSYNC[2]	G20	CSI	GPIO	INPUT	Keeper
CSI_HSYNC[2]	H19	CSI	GPIO	INPUT	Keeper
CSI_PIXCLK[2]	H20	CSI	GPIO	INPUT	Keeper

Table 101. 17×17 mm Package i.MX25 Signal Contact Assignment (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuration after Reset[1]
I2C1_CLK	F17	CSI	GPIO	INPUT	100 KΩ Pull-Up
I2C1_DAT	G17	CSI	GPIO	INPUT	100 KΩ Pull-Up
CSPI1_MOSI	T4	MISC	GPIO	INPUT	100 KΩ Pull-Up
CSPI1_MISO	W1	MISC	GPIO	OUTPUT	Low
CSPI1_SS0	R4	MISC	GPIO	INPUT	100 KΩ Pull-Up
CSPI1_SS1	V2	MISC	GPIO	INPUT	100 KΩ Pull-Up
CSPI1_SCLK	U3	MISC	GPIO	INPUT	100 KΩ Pull-Up
CSPI1_RDY	V1	MISC	GPIO	INPUT	100 KΩ Pull-Up
UART1_RXD	U2	MISC	GPIO	INPUT	100 KΩ Pull-Up
UART1_TXD	U1	MISC	GPIO	OUTPUT	High
UART1_RTS	T3	MISC	GPIO	INPUT	100 KΩ Pull-Up
UART1_CTS	T2	MISC	GPIO	OUTPUT	High
UART2_RXD	P4	MISC	GPIO	INPUT	100 KΩ Pull-Up
UART2_TXD	T1	MISC	GPIO	OUTPUT	High
UART2_RTS	R3	MISC	GPIO	INPUT	100 KΩ Pull-Up
UART2_CTS	R2	MISC	GPIO	INPUT	-
SD1_CMD	K20	SDIO	GPIO	INPUT	47 KΩ Pull-Up
SD1_CLK	M20	SDIO	GPIO	OUTPUT	High
SD1_DATA0	L20	SDIO	GPIO	INPUT	47 KΩ Pull-Up
SD1_DATA1	N20	SDIO	GPIO	INPUT	47 KΩ Pull-Up
SD1_DATA2	M19	SDIO	GPIO	INPUT	47 KΩ Pull-Up
SD1_DATA3	J20	SDIO	GPIO	INPUT	47 KΩ Pull-Up
KPP_ROW0	N4	MISC	GPIO	INPUT	100 KΩ Pull-Up
KPP_ROW1	R1	MISC	GPIO	INPUT	100 KΩ Pull-Up
KPP_ROW2	P3	MISC	GPIO	INPUT	100 KΩ Pull-Up
KPP_ROW3	P2	MISC	GPIO	INPUT	100 KΩ Pull-Up
KPP_COL0	P1	MISC	GPIO	INPUT	100 KΩ Pull-Up
KPP_COL1	N3	MISC	GPIO	INPUT	100 KΩ Pull-Up
KPP_COL2	N2	MISC	GPIO	INPUT	100 KΩ Pull-Up
KPP_COL3	N1	MISC	GPIO	INPUT	100 KΩ Pull-Up
FEC_MDC	L1	MISC	GPIO	OUTPUT	Low
FEC_MDIO	L2	MISC	GPIO	INPUT	22 KΩ Pull-Up

Table 102 lists the 17×17 mm package i.MX25 no connect contact assignments.

Table 102. 17×17 mm Package i.MX25 No Connect Contact Assignments

Signal Name	Contact Assignment
NC_BGA_B20	B20
NC_BGA_E17	E17
NC_BGA_H17	H17
NC_BGA_J19	J19
NC_BGA_M18	M18
NC_BGA_P20	P20
NC_BGA_U15	U15
NC_BGA_U16	U16
NC_BGA_V15	V15
NC_BGA_V16	V16
NC_BGA_V17	V17
NC_BGA_W14	W14
NC_BGA_Y2	Y2
NC_BGA_Y14	Y14
NC_BGA_Y17	Y17