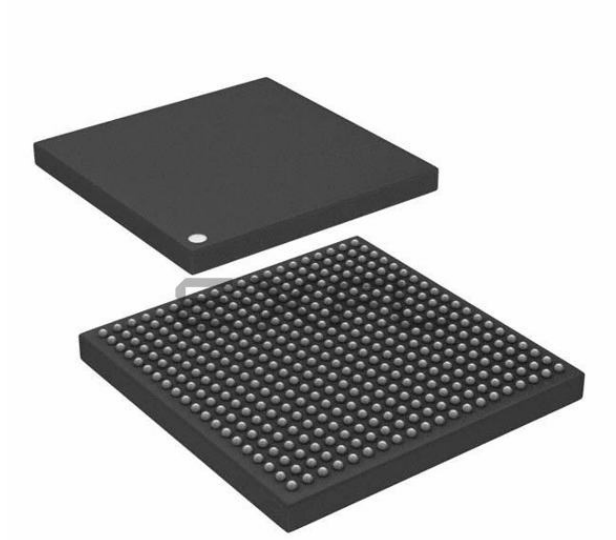

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM926EJ-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	LPDDR, DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	Keypad
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	2.0V, 2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	Boot Security, Cryptography, Secure Fusebox, Secure JTAG, Secure Memory, Tamper Detection
Package / Case	400-LFBGA
Supplier Device Package	400-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx251ajm4ar2

Table 3. i.MX25 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
EPIT(2)	Enhanced periodic interrupt timer	Timer peripherals	Each Enhanced Periodic Interrupt Timer (EPIT) is a 32-bit set-and-forget timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler to adjust the input clock frequency to the required time setting for the interrupts, and the counter value can be programmed on the fly.
ESAI	Enhanced serial audio interface	Connectivity peripherals	ESAI provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other DSPs. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator.
eSDHC(2)	Enhanced multimedia card/ secure digital host controller	Connectivity peripherals	The features of the eSDHC module, when serving as host, include the following: • Conforms to the SD host controller standard specification version 2.0 • Compatible with the JEDEC MMC system specification version 4.2 • Compatible with the SD memory card specification version 2.0 • Compatible with the SDIO specification version 1.2 • Designed to work with SD memory, miniSD memory, SDIO, miniSDIO, SD combo, MMC and MMC RS cards • Configurable to work in one of the following modes: —SD/SDIO 1-bit, 4-bit —MMC 1-bit, 4-bit, 8-bit • Full-/high-speed mode • Host clock frequency variable between 32 kHz and 52 MHz • Up to 200-Mbps data transfer for SD/SDIO cards using four parallel data lines • Up to 416-Mbps data transfer for MMC cards using eight parallel data lines
FEC	Fast ethernet controller	Connectivity peripherals	The Ethernet Media Access Controller (MAC) is designed to support both 10- and 100-Mbps Ethernet networks compliant with IEEE 802.3® standard. An external transceiver interface and transceiver function are required to complete the interface to the media
FlexCAN(2)	Controller area network module	Connectivity peripherals	The Controller Area Network (CAN) protocol is primarily designed to be used as a vehicle serial data bus running at 1 MBps.
GPIO(4)	General purpose I/O modules	System control peripherals	Used for general purpose input/output to external ICs. Each GPIO module supports 32 bits of I/O.
GPT(4)	General purpose timers	Timer peripherals	Each GPT is a 32-bit free-running or set-and-forget mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in set-and-forget mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.

Table 20. GPIO DC Electrical Characteristics (continued)

DC Electrical Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Input hysteresis	VHYS	OVDD = 3.3 V OVDD = 1.8V	370 290	—	420 320	mV
Schmitt trigger VT+[1]	VT+	—	0.5 × OVDD	—	—	V
Schmitt trigger VT–[1]	VT–	—	—	—	0.5 × OVDD	V
Pull-up resistor (22 kΩ PU)	Rpu	Vi=0	18.5	22	25.6	kΩ
Pull-up resistor (47 kΩ PU)	Rpu	Vi=0	41	47	55	kΩ
Pull-up resistor (100 kΩ PU)	Rpu	Vi=0	85	100	120	kΩ
Pull-down resistor (100 kΩ PD)	Rpd	VI = OVDD	85	100	120	kΩ
Input current (no pull-up/down)	IIN	VI = 0, OVDD = 3.3 V VI = OVDD = 3.3 V VI = 0, OVDD = 1.8 V VI = OVDD = 1.8 V	—	—	100 60 77 50	nA
Input current (22 kΩ PU)	IIN	VI = 0, OVDD = 3.3 V VI = OVDD = 3.3 V VI = 0, OVDD = 1.8 V VI = OVDD = 1.8 V	117 0.0001 64 0.0001	—	184 0.0001 104 0.0001	µA
Input current (47 kΩ PU)	IIN	VI = 0, OVDD = 3.3 V VI = OVDD = 3.3 V VI = 0, OVDD = 1.8 V VI = OVDD = 1.8 V	54 0.0001 30 0.0001	—	88 0.0001 49 0.0001	µA
Input current (100 kΩ PU)	IIN	VI = 0, OVDD = 3.3 V VI = OVDD = 3.3 V VI = 0, OVDD = 1.8 V VI = OVDD = 1.8 V	25 0.0001 14 0.0001	—	42 0.0001 23 0.0001	µA
Input current (100 kΩ PD)	IIN	VI = 0, OVDD = 3.3 V VI = OVDD = 3.3 V VI = 0, OVDD = 1.8 V VI = OVDD = 1.8 V	25 0.0001 14 0.0001	—	42 0.001 23 0.0001	µA
High-impedance I/O supply current	Icc–ovdd	VI = 0, OVDD = 3.3 V VI = OVDD = 3.3 V VI = 0, OVDD = 1.8 V VI = OVDD = 1.8 V	—	—	688 688 560 560	nA
High-impedance core supply current	Icc–vddi	VI = 0, OVDD = 3.3 V VI = OVDD = 3.3 V VI = 0, OVDD = 1.8 V VI = OVDD = 1.8 V	—	—	490 490 410 410	nA

[1] Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.

3.6 AC Electrical Characteristics

This section provides the AC parameters for slow and fast I/O.

Table 24. AC Parameters for Mobile DDR I/O (continued)

Parameter	Symbol	Load Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Output pad propagation delay[1] (high drive), 40%–60%	tpo	15 pF 35 pF	1.04/1.09 1.63/1.56	1.73/1.83 2.43/2.52	2.69/2.62 3.79/3.62	ns
Output pad propagation delay[1] (standard drive), 40%–60%	tpo	15 pF 35 pF	1.50/1.74 2.73/2.42	2.36/2.41 3.77/3.78	3.67/3.46 5.86/5.37	ns
Output enable to output valid delay[1] (max. drive), 50%–50%	tpv	15 pF 35 pF	1.17/1.01 1.43/1.30	1.93/1.61 2.33/2.00	3.06/2.55 3.69/3.13	ns
Output enable to output valid delay[1] (high drive), 50%–50%	tpv	15 pF 35 pF	1.38/1.28 1.97/1.92	2.25/1.99 3.16/2.86	3.58/3.10 5.01/4.39	ns
Output enable to output valid delay[1] (standard drive), 50%–50%	tpv	15 pF 35 pF	1.92/1.57 3.12/3.16	3.11/2.79 4.97/4.59	4.98/4.13 7.97/6.98	ns
Output enable to output valid delay[1] (max. drive), 40%–60%	tpv	15 pF 35 pF	1.28/1.12 1.49/1.36	2.01/1.70 2.33/2.01	3.09/2.60 3.60/3.06	ns
Output enable to output valid delay[1] (high drive), 40%–60%	tpv	15 pF 35 pF	1.43/1.33 1.90/1.84	2.24/1.99 2.96/2.68	3.47/3.02 4.59/4.03	ns
Output enable to output valid delay[1] (standard drive), 40%–60%	tpv	15 pF 35 pF	1.85/1.78 2.80/2.81	2.91/2.62 4.37/4.53	4.54/3.96 6.88/6.05	ns
Output pad slew rate[2] (max. drive)	tps	25 pF 50 pF	0.80/0.92 0.43/0.50	1.35/1.50 0.72/0.81	2.23/2.27 1.66/1.68	V/ns
Output pad slew rate[2] (high drive)	tps	25 pF 50 pF	0.37/0.43 0.19/0.23	0.62/0.70 0.33/0.37	1.03/1.05 0.75/0.77	V/ns
Output pad slew rate[2] (standard drive)	tps	25 pF 50 pF	0.18/0.22 0.10/0.12	0.31/0.35 0.16/0.18	0.51/0.53 0.38/0.39	V/ns
Output pad dI/dt[3] (max. drive)	tdit	25 pF 50 pF	64 69	171 183	407 432	mA/ns
Output pad dI/dt[3] (high drive)	tdit	25 pF 50 pF	37 39	100 106	232 246	mA/ns
Output pad di/dt[3] (standard drive)	tdit	25 pF 50 pF	18 20	50 52	116 123	mA/ns
Input pad transition times[4]	trfi	1.0 pF	0.07/0.08	0.11/0.13	0.16/0.20	ns
Input pad propagation delay, 50%–50%[4]	tpi	1.0 pF	0.77/1.00	1.22/1.45	1.89/2.21	ns
Input pad propagation delay, 40%–60%[4]	tpi	1.0 pF	1.59/1.82	2.04/2.27	2.69/3.01	ns

1 Maximum condition for tpr, tpo, tpi, and tpv: wcs model, 1.1 V, I/O 1.65 V, and 105 °C. Minimum condition for tpr, tpo, and tpv: bcs model, 1.3 V, I/O 1.95 V and –40 °C. Input transition time from core is 1 ns (20%–80%).

2 Minimum condition for tps: wcs model, 1.1 V, I/O 1.65 V, and 105 °C. tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.

3 Maximum condition for tdit: bcs model, 1.3 V, I/O 1.95 V, and –40 °C.

4 Maximum condition for tpi and trfi: wcs model, 1.1 V, I/O 1.65 V and 105 °C. Minimum condition for tpi and trfi: bcs model, 1.3 V, I/O 1.95 V and –40 °C. Input transition time from pad is 5 ns (20%–80%).

3.7.2.1 PIO Mode Timing Parameters

Figure 11 shows a timing diagram for PIO read mode.

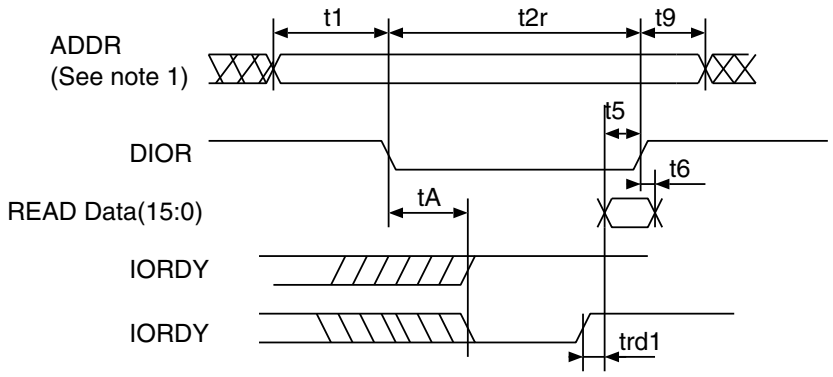

Figure 11. PIO Read Mode Timing

To meet PIO read mode timing requirements, a number of timing parameters must be controlled. Table 36 shows timing parameters and their determining relations, and indicates parameters that can be adjusted to meet required conditions.

Table 36. Timing Parameters for PIO Read Mode

ATA Parameter	PIO Read Mode Timing Parameter[1]	Relation	Adjustable Parameter
t1	t1	t1(min.) = time_1 × T – (tskew1 + tskew2 + tskew5)	time_1
t2	t2r	t2(min.) = time_2r × T – (tskew1 + tskew2 + tskew5)	time_2r
t9	t9	t9(min.) = time_9 × T – (tskew1 + tskew2 + tskew6)	time_9
t5	t5	t5(min.) = tco + tsu + tbuf + tbuf + tcable1 + tcable2	If not met, increase time_2
t6	t6	0	—
tA	tA	tA(min.) = (1.5 + time_ax) × T – (tco + tsui + tcable2 + tcable2 + 2 × tbuf)	time_ax
trd	trd1	trd1(max.) = (–trd) + (tskew3 + tskew4) trd1(min.) = (time_pio_rdx – 0.5) × T – (tsu + thi) (time_pio_rdx – 0.5) × T > tsu + thi + tskew3 + tskew4	time_pio_rdx
t0	—	t0(min.) = (time_1 + time_2 + time_9) × T	time_1, time_2r, time_9

[1] See Figure 11.

Figure 17 shows timing for device-terminated UDMA in-transfer.

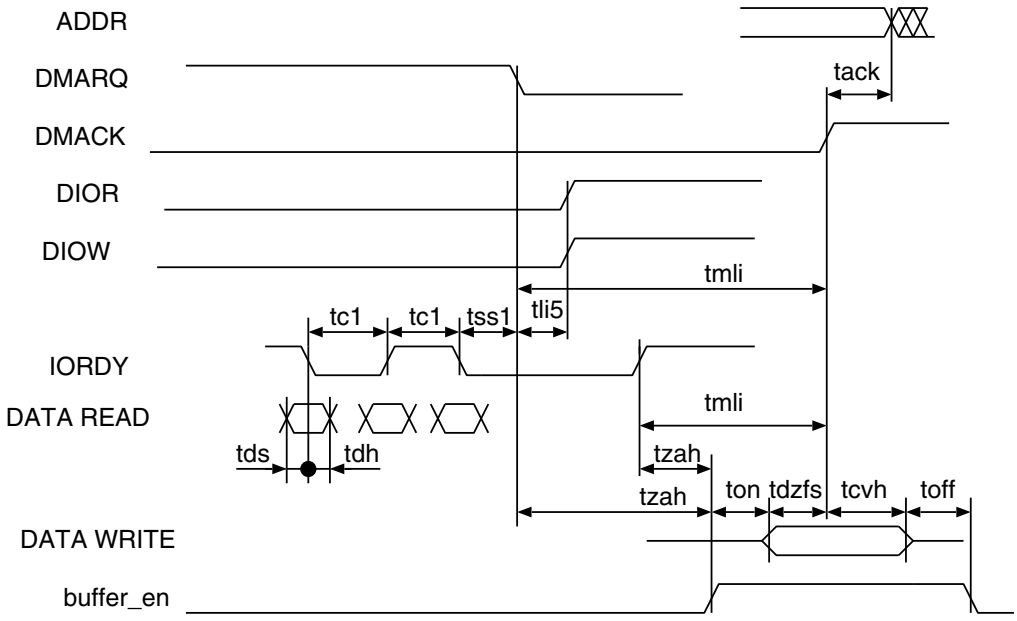

Figure 17. Timing for Device-Terminated UDMA Transfer

Timing parameters for UDMA in-burst are listed in Table 39.

Table 39. Timing Parameters for UDMA In-Burst

ATA Parameter	Spec. Parameter	Value	Required Conditions
tack	tack	tack(min.) = (time_ack × T) – (tskew1 + tskew2)	time_ack
tenv	tenv	tenv(min.) = (time_env × T) – (tskew1 + tskew2) tenv(max.) = (time_env × T) + (tskew1 + tskew2)	time_env
tds	tds1	tds – (tskew3) – ti_ds > 0	tskew3, ti_ds, ti_dh should be low enough
tdh	tdh1	tdh – (tskew3) –ti_dh > 0	
tcyc	tc1	(tcyc – tskew) > T	T big enough
trp	trp	trp(min.) = time_rp × T – (tskew1 + tskew2 + tskew6)	time_rp
—	tx1[1]	(time_rp × T) – (tco + tsu + 3T + 2 × tbuf + 2 × tcable2) > trfs (drive)	time_rp
tmli	tmli1	tmli1(min.) = (time_mlix + 0.4) × T	time_mlix
tzah	tzah	tzah(min.) = (time_zah + 0.4) × T	time_zah
tdzfs	tdzfs	tdzfs = (time_dzfs × T) – (tskew1 + tskew2)	time_dzfs
tcvh	tcvh	tcvh = (time_cvh × T) – (tskew1 + tskew2)	time_cvh
—	ton toff	ton = time_on × T – tskew1 toff = time_off × T – tskew1	—

[1] There is a special timing requirement in the ATA host that requires the internal DIOW to go only high three clocks after the last active edge on the DSTROBE signal. The equation given on this line tries to capture this constraint.

Make t_{on} and t_{off} big enough to avoid bus contention.

3.7.5 Configurable Serial Peripheral Interface (CSPI) Timing

Figure 23 and Figure 24 provide CSPI master and slave mode timing diagrams, respectively. Table 43 describes the timing parameters (t1–t14) that are shown in the figures. The values shown in timing diagrams were tested using a worst-case core voltage of 1.1 V, slow pad voltage of 2.68 V, and fast pad voltage of 1.65 V.

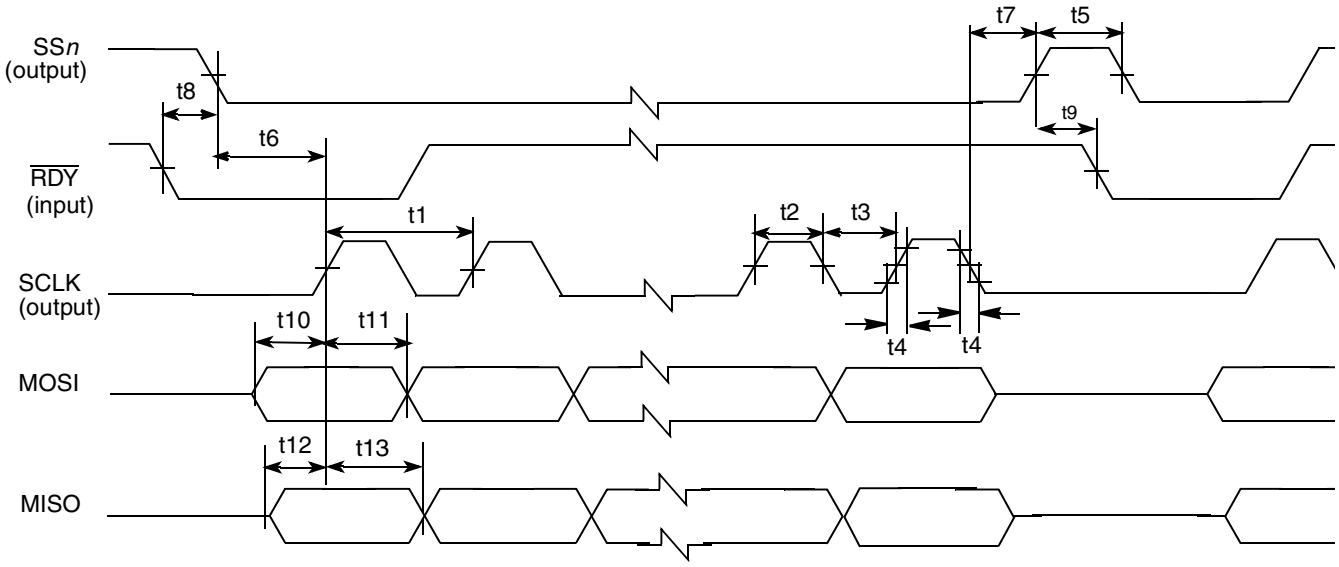

Figure 23. CSPI Master Mode Timing Diagram

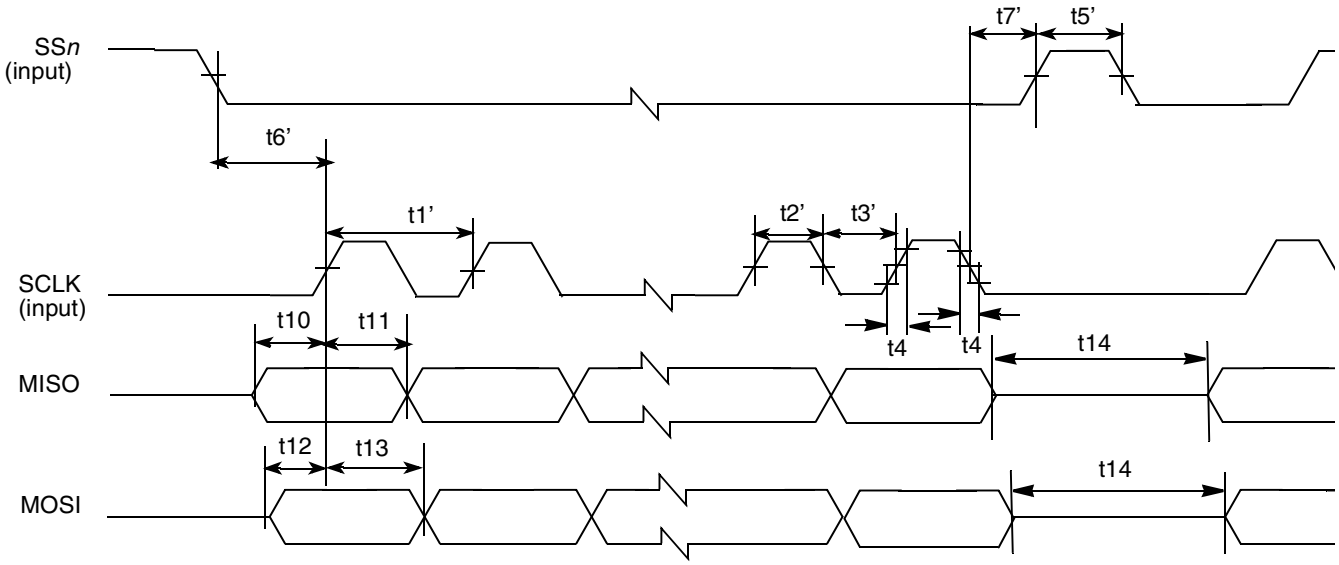

Figure 24. CSPI Slave Mode Timing Diagram

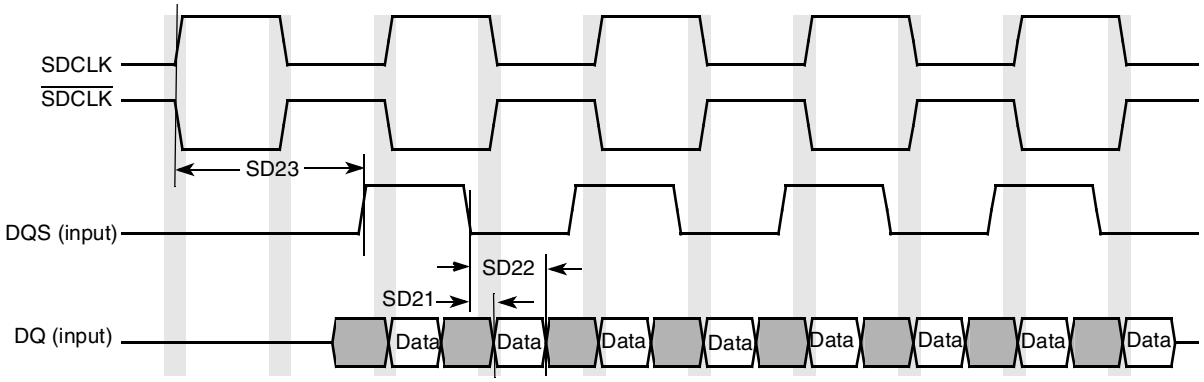

Figure 30. Mobile DDR SDRAM DQ versus DQS and SDCLK Read Cycle Timing Diagram

Table 49. Mobile DDR SDRAM Read Cycle Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
SD21	DQS – DQ Skew (defines the data valid window in read cycles related to DQS)	tDQSQ	—	0.85	ns
SD22	DQS DQ HOLD time from DQS	tQH	2.3	—	ns
SD23	DQS output access time from SDCLK posedge	tDQSCK	—	6.7	ns

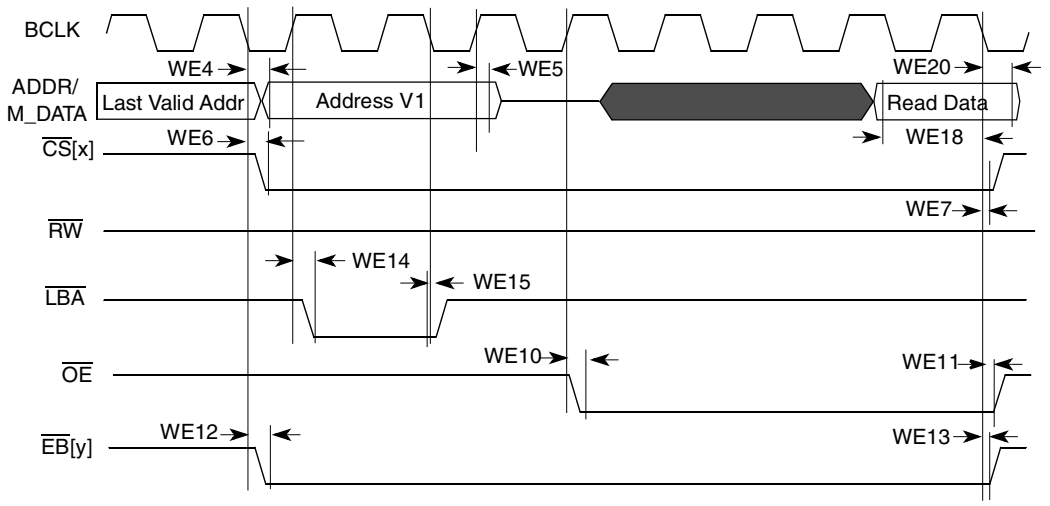

Figure 44. Muxed A/D Mode Timing Diagram for Synchronous Read Access—WSC=7, LBA=1, LBN=1, LAH=1, OEA=7

Figure 45 through Figure 49, and Table 57 help to determine timing parameters relative to chip select (CS) state for asynchronous and DTACK WEIM accesses with corresponding WEIM bit fields and the timing parameters mentioned above.

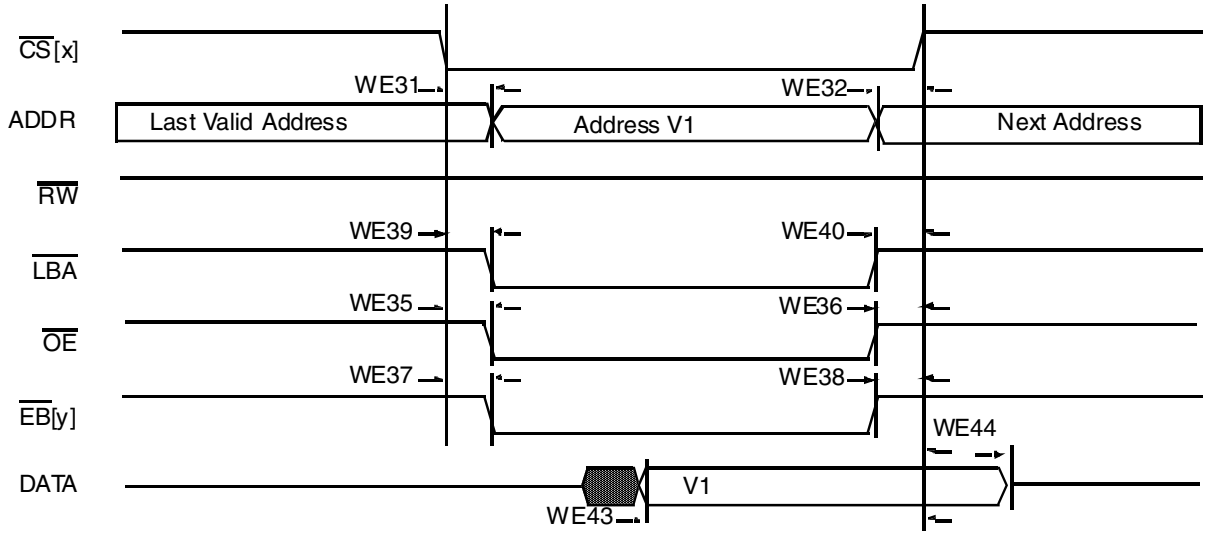

Figure 45. Asynchronous Memory Read Access

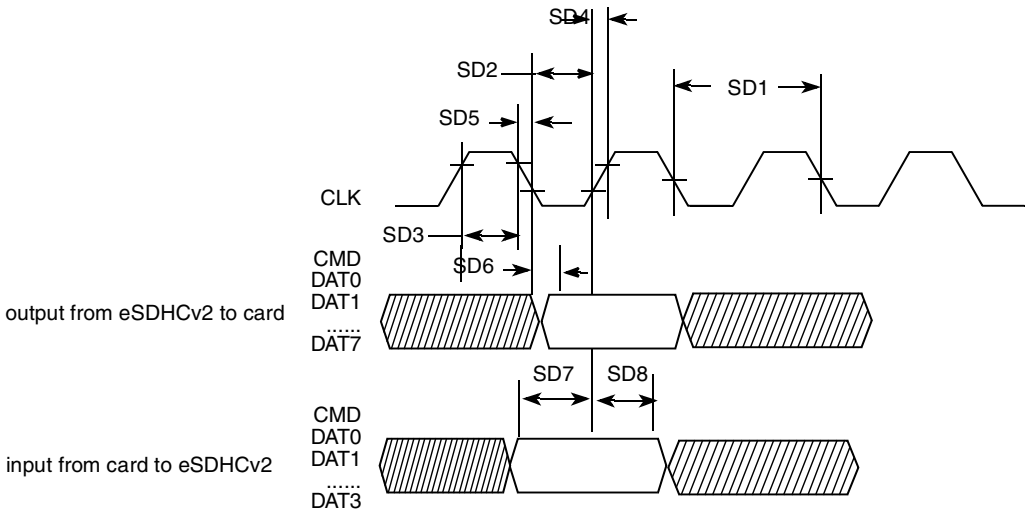

Figure 54. eSDHCv2 Timing

Table 61. eSDHCv2 Interface Timing Specification

ID	Parameter	Symbols	Min.	Max.	Unit
Card Input Clock					
SD1	Clock frequency (low speed)	f_{PP}[1]	0	400	kHz
	Clock frequency (SD/SDIO full speed/high speed)	f_{PP}[2]	0	25/50	MHz
	Clock frequency (MMC full speed/high speed)	f_{PP}[3]	0	20/52	MHz
	Clock frequency (identification mode)	f_{OD}	100	400	kHz
SD2	Clock low time	t_{WL}	6.5	—	ns
SD3	Clock high time	t_{WH}	6.5	—	ns
SD4	Clock rise time	t_{TLH}	—	3	ns
SD5	Clock fall time	t_{THL}	—	3	ns
eSDHC Output / Card Inputs CMD, DAT (Reference to CLK)					
SD6	eSDHC output delay	t_{OD}	–3	3	ns
eSDHC Input / Card Outputs CMD, DAT (Reference to CLK)					
SD7	eSDHC input setup time	t_{ISU}	2.5	—	ns
SD8	eSDHC input hold time	t_{IH}[4]	2.5	—	ns

1 In low-speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2 In normal-speed mode for SD/SDIO card, clock frequency can be any value between 0 ~ 25 MHz. In high speed mode, clock frequency can be any value between 0 ~ 50 MHz.

3 In normal-speed mode for MMC card, clock frequency can be any value between 0 ~ 20 MHz. In high speed mode, clock frequency can be any value between 0 ~ 52 MHz.

4 To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

3.7.9 Fast Ethernet Controller (FEC) Timing

The FEC is designed to support both 10- and 100-Mbps Ethernet networks compliant with the IEEE 802.3 standard. An external transceiver interface and transceiver function are required to complete the interface to the media. The FEC supports 10/100 Mbps MII (18 pins altogether), 10/100 Mbps RMII (ten pins, including serial management interface) and the 10-Mbps-only 7-Wire interface (which uses seven of the MII pins), for connection to an external Ethernet transceiver. All signals are compatible with transceivers operating at a voltage of 3.3 V.

The following subsections describe the timing for MII and RMII modes.

3.7.9.1 FEC MII Mode Timing

The following subsections describe MII receive, transmit, asynchronous inputs, and serial management signal timings.

3.7.9.1.4 MII Receive Signal Timing (FEC_RXD[3:0], FEC_RX_DV, FEC_RX_ER, and FEC_RX_CLK)

The receiver functions correctly up to an FEC_RX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the FEC_RX_CLK frequency.

Figure 55 shows MII receive signal timings. Table 62 describes the timing parameters (M1–M4) shown in the figure.

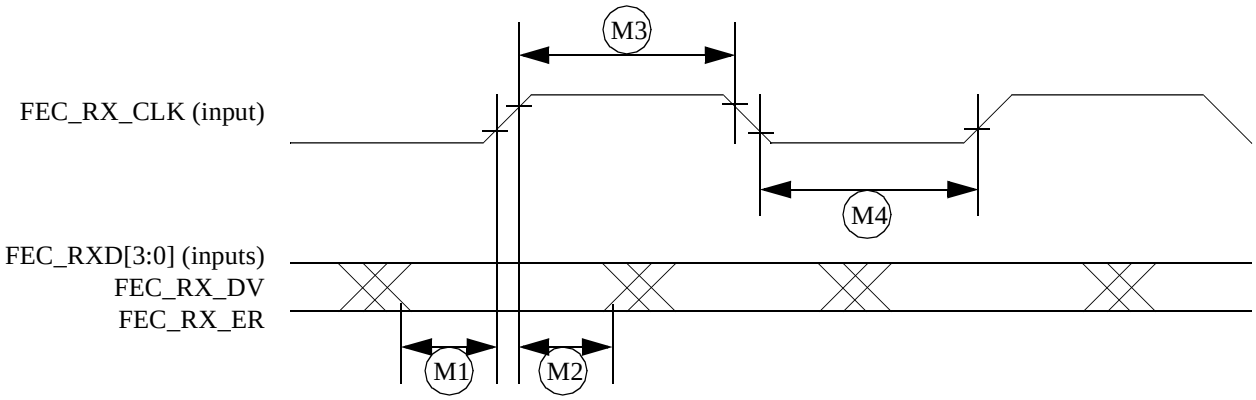

Figure 55. MII Receive Signal Timing Diagram

Table 62. MII Receive Signal Timing

ID	Characteristic[1]	Min.	Max.	Unit
M1	FEC_RXD[3:0], FEC_RX_DV, FEC_RX_ER to FEC_RX_CLK setup	5	—	ns
M2	FEC_RX_CLK to FEC_RXD[3:0], FEC_RX_DV, FEC_RX_ER hold	5	—	ns
M3	FEC_RX_CLK pulse width high	35%	65%	FEC_RX_CLK period
M4	FEC_RX_CLK pulse width low	35%	65%	FEC_RX_CLK period

[1] FEC_RX_DV, FEC_RX_CLK, and FEC_RXD0 have the same timing in 10 Mbps 7-wire interface mode.

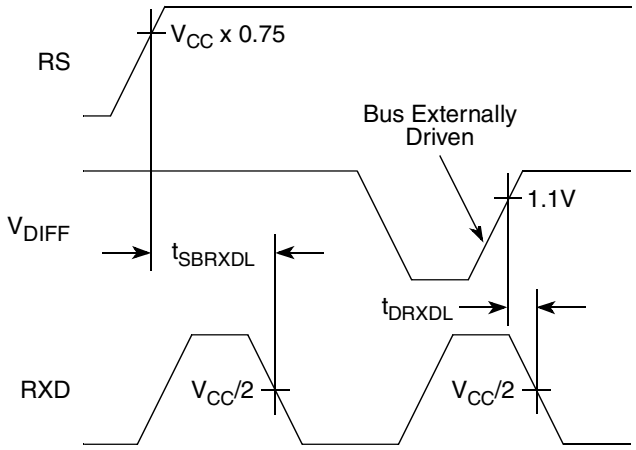

Figure 61. Timing Diagram for FlexCAN Standby Signal

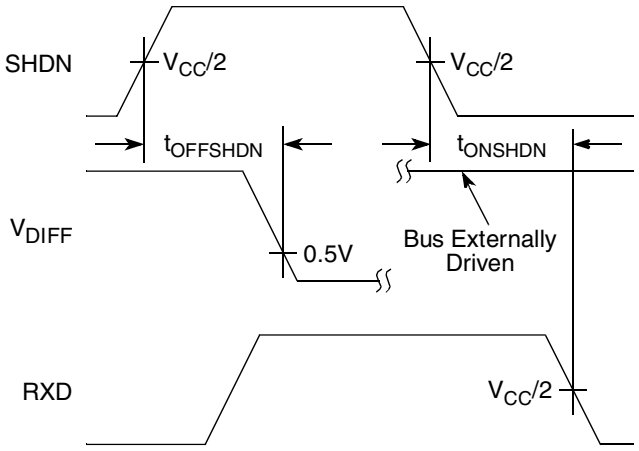

Figure 62. Timing Diagram for FlexCAN Shutdown Signal

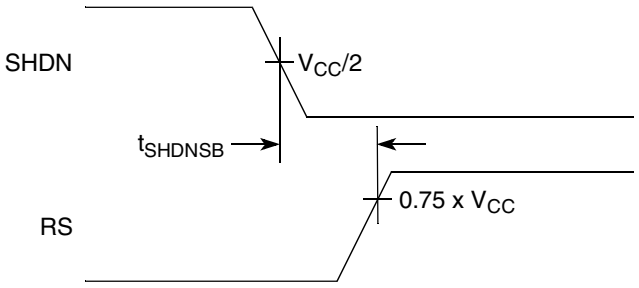

Figure 63. Timing Diagram for FlexCAN Shutdown-to-Standby Signal

Because integer multiples are not possible, taking into account the range of frequencies at which the SoC has to operate, DPLLs work in FOL mode only.

[1] A device must internally provide a hold time of at least 300 ns for I2DAT signal in order to bridge the undefined region of the falling edge of I2CLK.

[2] The maximum hold time has only to be met if the device does not stretch the LOW period (ID no IC5) of the I2CLK signal

[3] A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement of Set-up time (ID No IC7) of 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the I2CLK signal.

If such a device does stretch the LOW period of the I2CLK signal, it must output the next data bit to the I2DAT line max_rise_time(ID No IC9) + data_setup_time(ID No IC7) = 1000 + 250 = 1250 ns (according to the Standard-mode I2C-bus specification) before the I2CLK line is released.

[4] C_b = total capacitance of one bus line in pF.

Table 70. I2C Module Timing Parameters: 1.8 V +/– 0.10 V

ID	Parameter	Standard Mode		Unit
		Min.	Max.	
IC1	I2CLK cycle time	10	-	µs
IC2	Hold time (repeated) START condition	4.0	-	µs
IC3	Set-up time for STOP condition	4.0	-	µs
IC4	Data hold time	0[1]	3.45[2]	µs
IC5	HIGH Period of I2CLK Clock	4.0	-	µs
IC6	LOW Period of the I2CLK Clock	4.7	-	µs
IC7	Set-up time for a repeated START condition	4.7	-	µs
IC8	Data set-up time	250	-	ns
IC9	Bus free time between a STOP and START condition	4.7	-	µs
IC10	Rise time of both I2DAT and I2CLK signals	-	1000	ns
IC11	Fall time of both I2DAT and I2CLK signals	-	300	ns
IC12	Capacitive load for each bus line (C_b)	-	400	pF

[1] A device must internally provide a hold time of at least 300 ns for I2DAT signal in order to bridge the undefined region of the falling edge of I2CLK.

[2] The maximum hold time has only to be met if the device does not stretch the LOW period (ID no IC5) of the I2CLK signal

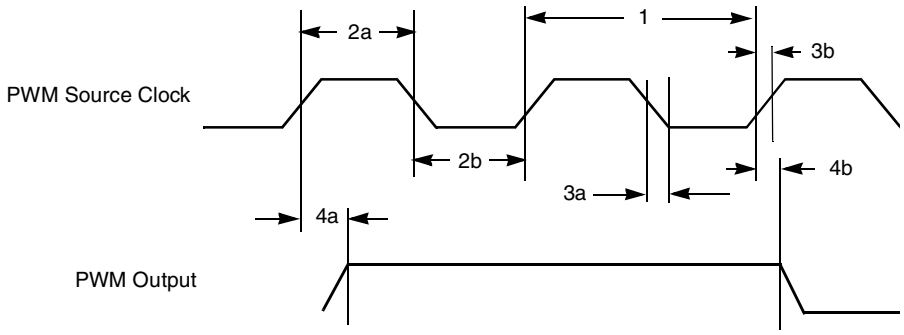

Figure 67. PWM Timing

Table 73. PWM Output Timing Parameter

Ref No.	Parameter	Minimum	Maximum	Unit
1	System CLK frequency[1]	0	ipg_clk	MHz
2a	Clock high time	12.29	—	ns
2b	Clock low time	9.91	—	ns
3a	Clock fall time	—	0.5	ns
3b	Clock rise time	—	0.5	ns
4a	Output delay time	—	9.37	ns
4b	Output setup time	8.71	—	ns

[1] CL of PWMO = 30 pF

3.7.14 Subscriber Identity Module (SIM) Timing

Each SIM module interface consists of a total of 12 pins (two separate ports, each containing six signals). Typically a port uses five signals.

The interface is designed to be used with synchronous SIM cards, meaning the SIM module provides the clock used by the SIM card. The clock frequency is typically 372 times the Tx/Rx data rate; however, the SIM module can also work with CLK frequencies of 16 times the Tx/Rx data rate.

There is no timing relationship between the clock and the data. The clock that the SIM module provides to the SIM card is used by the SIM card to recover the clock from the data in the same manner as standard UART data exchanges. All six signals (five for bidirectional Tx/Rx) of the SIM module are asynchronous with each other.

There are no required timing relationships between signals in normal mode. The SIM card is initiated by the interface device; the SIM card responds with Answer to Reset. Although the SIM interface has no defined requirements, the ISO/IEC 7816 defines reset and power-down sequences (for detailed information see ISO/IEC 7816).

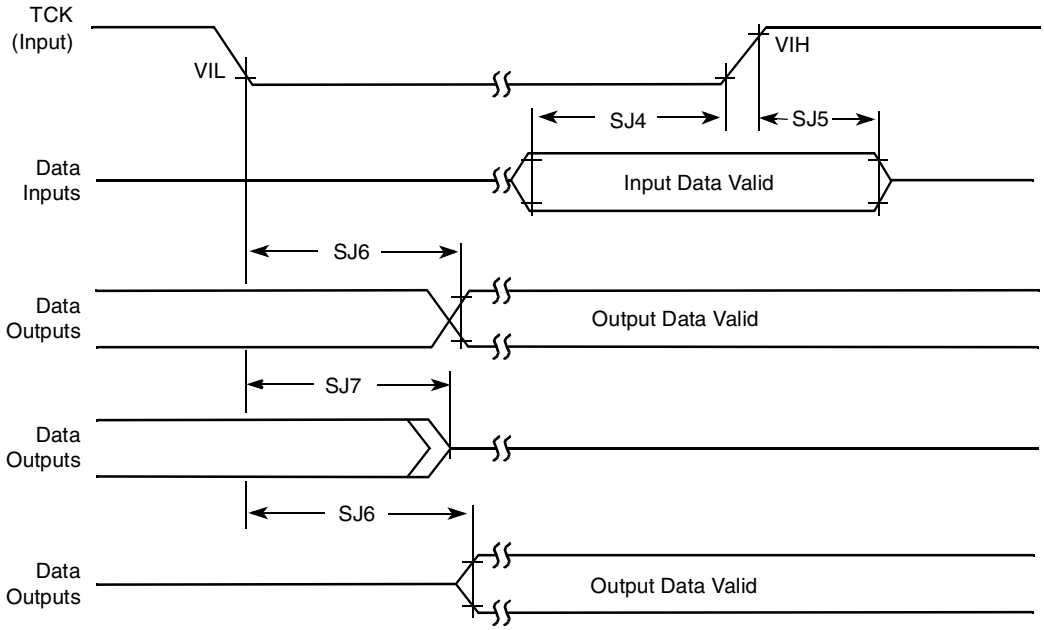

Figure 73. Boundary Scan (JTAG) Timing Diagram

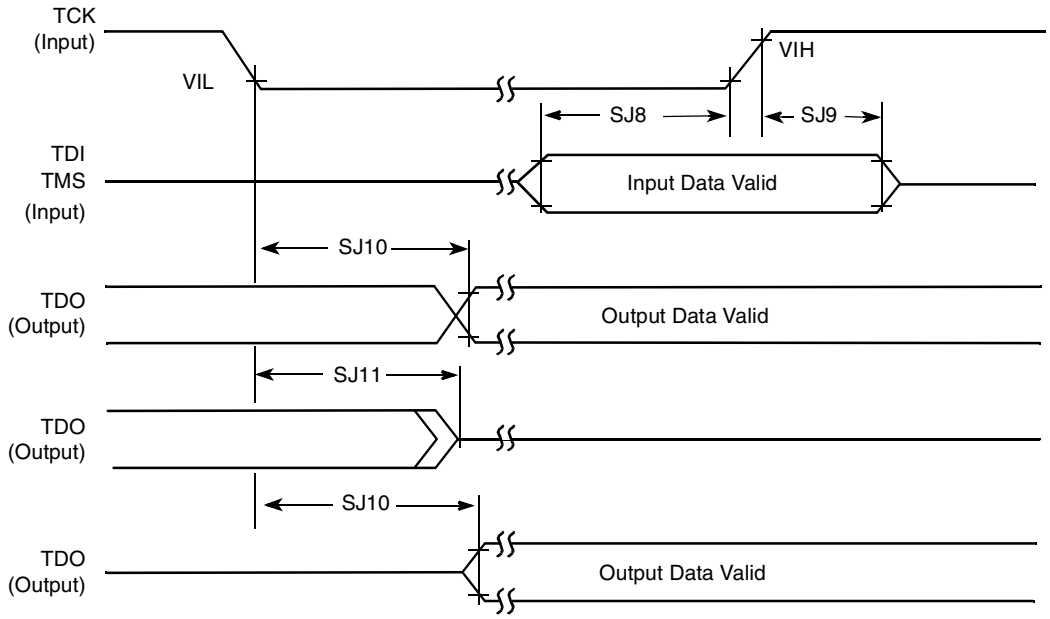

Figure 74. Test Access Port Timing Diagram

Table 83. SSI Transmitter Timing with External Clock

ID	Parameter	Min.	Max.	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36.0	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns
SS25	(Tx/Rx) CK clock low period	36.0	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS27	FS (bl) low/ high setup before (Tx) CK falling	–10.0	15.0	ns
SS29	FS (bl) low/ high setup before (Tx) CK falling	10.0	—	ns
SS31	FS (wl) low/ high setup before (Tx) CK falling	–10.0	15.0	ns
SS33	FS (wl) low/ high setup before (Tx) CK falling	10.0	—	ns
SS37	(Tx) CK high to STXD valid from high impedance	—	15.0	ns
SS38	(Tx) CK high to STXD high/low	—	15.0	ns
SS39	(Tx) CK high to STXD high impedance	—	15.0	ns
Synchronous External Clock Operation				
SS44	SRXD setup before (Tx) CK falling	10.0	—	ns
SS45	SRXD hold after (Tx) CK falling	2.0	—	ns
SS46	SRXD rise/fall time	—	6.0	ns

Note:

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables figures.
- All timings are on pads when SSI is being used for data transfer.
- ”Tx” and “Rx” refer, respectively, to the transmit and receive sections of the SSI.
- For internal frame sync operation using external clock, the FS timing is the same as that of Tx data (for example, during AC97 mode of operation).

assertion of *soc* is detected. Thus, if the *soc* signal is continuously asserted, the ADC undergoes successive conversion cycles and achieves the maximum sampling rate. If *soc* is negated, no conversion is initiated.

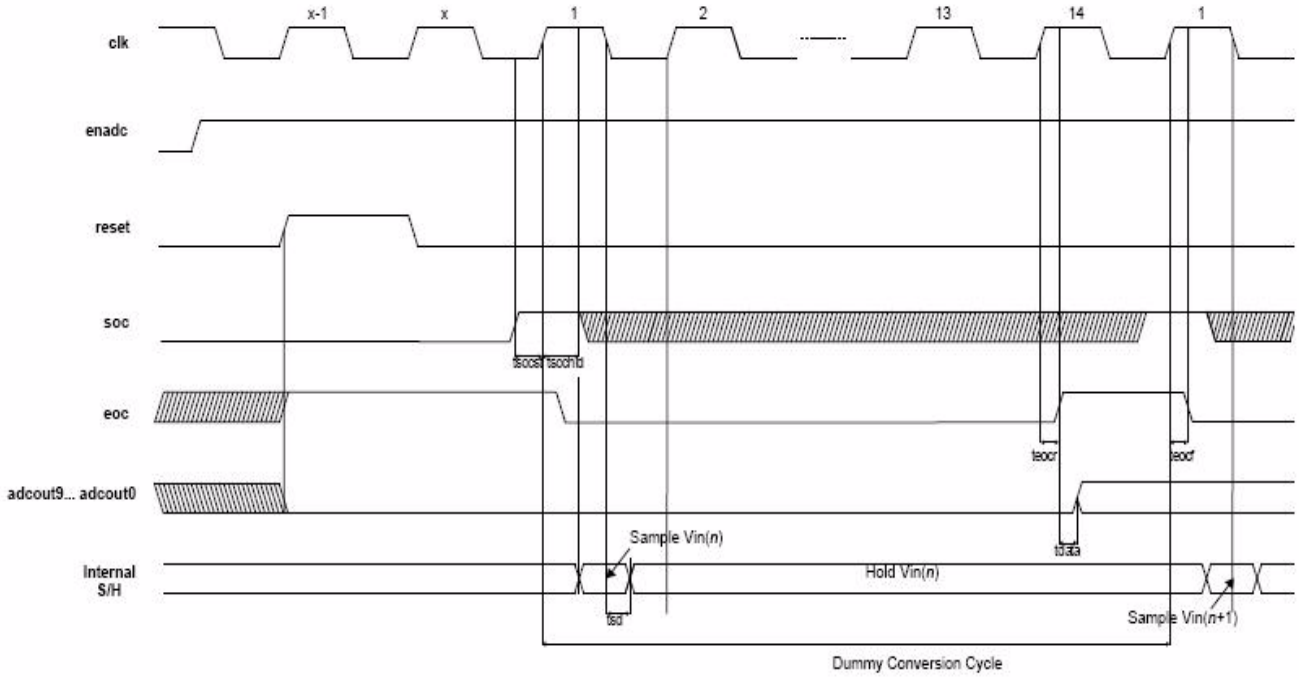

Figure 82. Start-up Sequence

The output data can be read from *adcout11...adcout0*, and is available *tdata* nanoseconds after the rising edge of *eoc*. The *reset* signal and the digital signals controlling the analog switches (*ypsw, xpsw, ynsw, xnsw*) are totally asynchronous.

The following conditions are necessary to guarantee the correct operation of the ADC:

- The input multiplexer selection (*selin11…selin0*) is stable during both the last clock cycle (14^{th}) and the first clock cycle (1^{st}). The best way to guarantee this is to make the input multiplexer selection during clock cycles 2 to 13.
- The references are stable during clock cycle 1 to 13. The best way to guarantee this is to make the reference multiplexer selection (*selrefp* and *selrefn*) before issuing an *soc* pulse and changing it only after an *eoc* pulse has been acquired, during the last clock cycle (14).

3.7.20.1.3 VP_VM Bidirectional Mode Timing

Table 94 defines the VP_VM bidirectional mode signals.

Table 94. Signal Definitions—VP_VM Bidirectional Mode

Name	Direction	Signal Description
USB_TXOE_B	Out	• Transmit enable, active low
USB_DAT_VP	Out (Tx) In (Rx)	• Tx VP data when USB_TXOE_B is low • Rx VP data when USB_TXOE_B is high
USB_SE0_VM	Out (Tx) In (Rx)	• Tx VM data when USB_TXOE_B low • Rx VM data when USB_TXOE_B high
USB_RCV	In	• Differential Rx data

Figure 93 shows the USB transmit waveform in VP_VM bidirectional mode diagram.

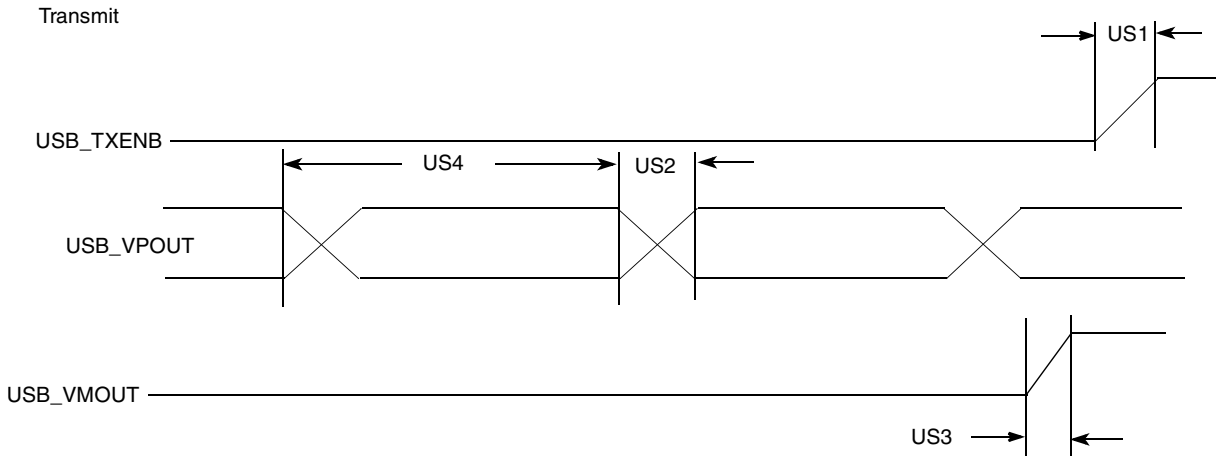

Figure 93. USB Transmit Waveform in VP_VM Bidirectional Mode

Figure 94 shows the USB receive waveform in VP_VM bidirectional mode diagram.

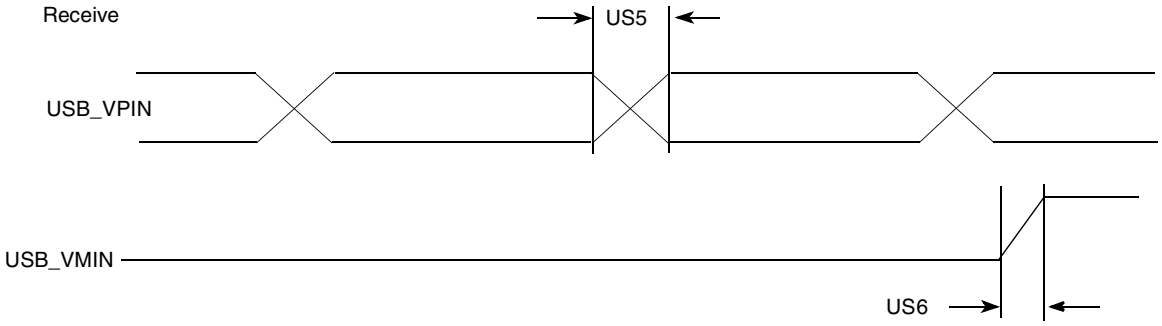

Figure 94. USB Receive Waveform in VP_VM Bidirectional Mode

Table 100. 17×17 mm Package Ground, Power Sense, and Reference Contact Assignments (continued)

Contact Name	Contact Assignment
NVCC_DRYICE[1]	W11
NVCC_EMI1	G6, G7, G8, G9, H6, H7, H8, J6, J7
NVCC_EMI2	G12, G13, G14, G15, H12, H13, H14
NVCC_JTAG	U10
NVCC_LCDC	P6, P7, R6, R7
NVCC_MISC	N5, N6, N7
NVCC_NFC	L6, L7, L8
NVCC_SDIO	R17
OSC24M_GND	W15
OSC24M_VDD	W16
QGND	A1, A11, A20, B11, C11, D11, E5, E6, E7, E8, E9, E10, E11, E12, E13, E14, E15, E16, F5, F6, F7, F8, F9, F10, F11, F12, F13, F14, F15, F16, G5, G10, G16, H5, H9, H10, H11, H15, H16, J5, J9, J10, J11, J15, J16, K1, K2, K3, K4, K5, K8, K9, K10, K11, K13, K14, K15, L5, L9, L10, L11, L12, L13, L14, L15, M8, M9, M10, M11, M12, M13, M14, M15, N9, N12, N13, N15, N16, P5, P13, P14, P15, P16, R5, R8, R9, R10, R11, R12, R13, R14, R15, R16, T5, T6, T7, T8, T9, T10, T11, T12, T13, T14, T15, T16, Y1, Y20
QVDD	G11, J8, J12, K6, K7, K12, M5, M6, M7, N8, P8, P9
REF	V11
UPLL_GND	M16
UPLL_VDD	L16
USBPHY1_UPLLVDD	M17
USBPHY1_UPLLVSS	N17
USBPHY1_VDDA	K16
USBPHY1_VDDA_BIAS	K19
USBPHY1_VSSA	L19
USBPHY1_VSSA_BIAS	J17
USBPHY2_VDD	W18
USBPHY2_VSS	W17

[1] NVCC_DRYICE is a supply output. An external capacitor no less than 4 µF must be connected to it. A 4.7 µF capacitor is recommended.

4.3 Signal Contact Assignments—17 x 17 mm, 0.8 mm Pitch

Table 101 lists the 17×17 mm package i.MX25 signal contact assignments.

Table 101. 17×17 mm Package i.MX25 Signal Contact Assignment

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuration after Reset[1]
A0	A18	EMI2	DDR	OUTPUT	Low
A1	B17	EMI2	DDR	OUTPUT	Low
A2	C17	EMI2	DDR	OUTPUT	Low
A3	B18	EMI2	DDR	OUTPUT	Low
A4	C20	EMI2	DDR	OUTPUT	Low
A5	A19	EMI2	DDR	OUTPUT	Low
A6	C19	EMI2	DDR	OUTPUT	Low
A7	B19	EMI2	DDR	OUTPUT	Low
A8	D18	EMI2	DDR	OUTPUT	Low
A9	C18	EMI2	DDR	OUTPUT	Low
A10	A2	EMI1	DDR	OUTPUT	Low
MA10	D16	EMI2	DDR	OUTPUT	Low
A11	D20	EMI2	DDR	OUTPUT	Low
A12	D17	EMI2	DDR	OUTPUT	Low
A13	D19	EMI2	DDR	OUTPUT	Low
A14	A3	EMI1	DDR	OUTPUT	Low
A15	B4	EMI1	DDR	OUTPUT	Low
A16	C6	EMI1	DDR	OUTPUT	Low
A17	B5	EMI1	DDR	OUTPUT	Low
A18	D7	EMI1	DDR	OUTPUT	Low
A19	A4	EMI1	DDR	OUTPUT	Low
A20	B6	EMI1	DDR	OUTPUT	Low
A21	C7	EMI1	DDR	OUTPUT	Low
A22	A5	EMI1	DDR	OUTPUT	Low
A23	A6	EMI1	DDR	OUTPUT	Low
A24	B7	EMI1	DDR	OUTPUT	Low
A25	A7	EMI1	DDR	OUTPUT	Low
SD0	A12	EMI1	DDR	INPUT	Keeper
SD1	C13	EMI1	DDR	INPUT	Keeper
SD2	B13	EMI1	DDR	INPUT	Keeper

Table 104. Revision History (continued)

Rev. Number	Date	Substantive Change(s)
Rev. 6	—	This revision number was skipped so the Consumer/Industrial and Automotive revision numbers can be in sync.
Rev. 5	09/2010	• Added Section 3.2.3, “SRTC DryIce Power-Up/Down Sequence.”
Rev. 4	08/2010	• Updated Table 56, "WEIM Bus Timing Parameters," on page 69 to include new row for WE19. • Updated Table 6, "DC Operating Conditions," on page 11 to include Min and Max values of FUSE_VDD.
Rev. 3	06/2010	• Updated Table 1, “Ordering Information,” to include new part numbers.
Rev. 2	03/2010	• Updated Table 1, “Ordering Information,” to include new part numbers. • Added Table 2, “i.MX25 Parts Functional Differences.” • Added Section 3.3, “Power Characteristics.”
Rev. 1	10/2009	• Updated Table 1, “Ordering Information,” to include new part numbers. • Updated DRYICE description in Table 3, “i.MX25 Digital and Analog Modules.” • Updated REF signal description in Table 4, “Signal Considerations.” • Updated ESD damage immunity values in Table 5, “DC Absolute Maximum Ratings.” • Updated values in Table 13, “i.MX25 Power Mode Current Consumption.” • Added a note on timing in Section 3.2.1, “Power-Up Sequence.” • Added Table 14, “iMX25 Reduced Power Mode Current Consumption.” • Updated Table 55, “NFC Timing Parameters.” • Updated values in Table 56, “WEIM Bus Timing Parameters. • Updated Table 85, “Touchscreen ADC Electrical Specifications.”
Rev. 0	6/2009	Initial release.