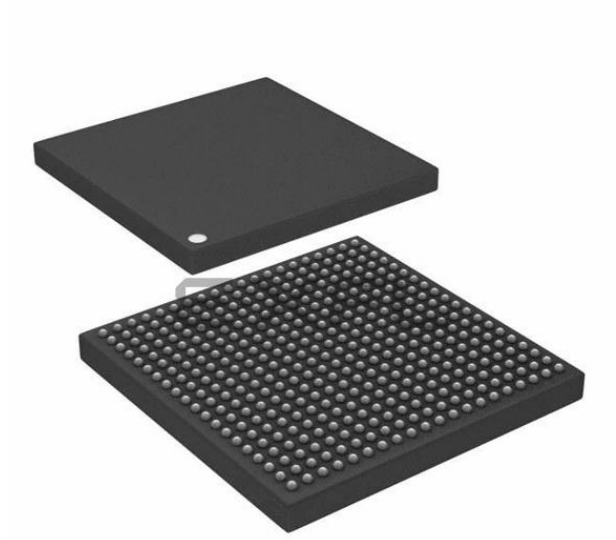

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM926EJ-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	LPDDR, DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD, Touchscreen
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	2.0V, 2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	Boot Security, Cryptography, Secure Fusebox, Secure JTAG, Secure Memory, Tamper Detection
Package / Case	400-LFBGA
Supplier Device Package	400-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx255avm4

1.2 Block Diagram

Figure 1 shows the simplified interface block diagram.

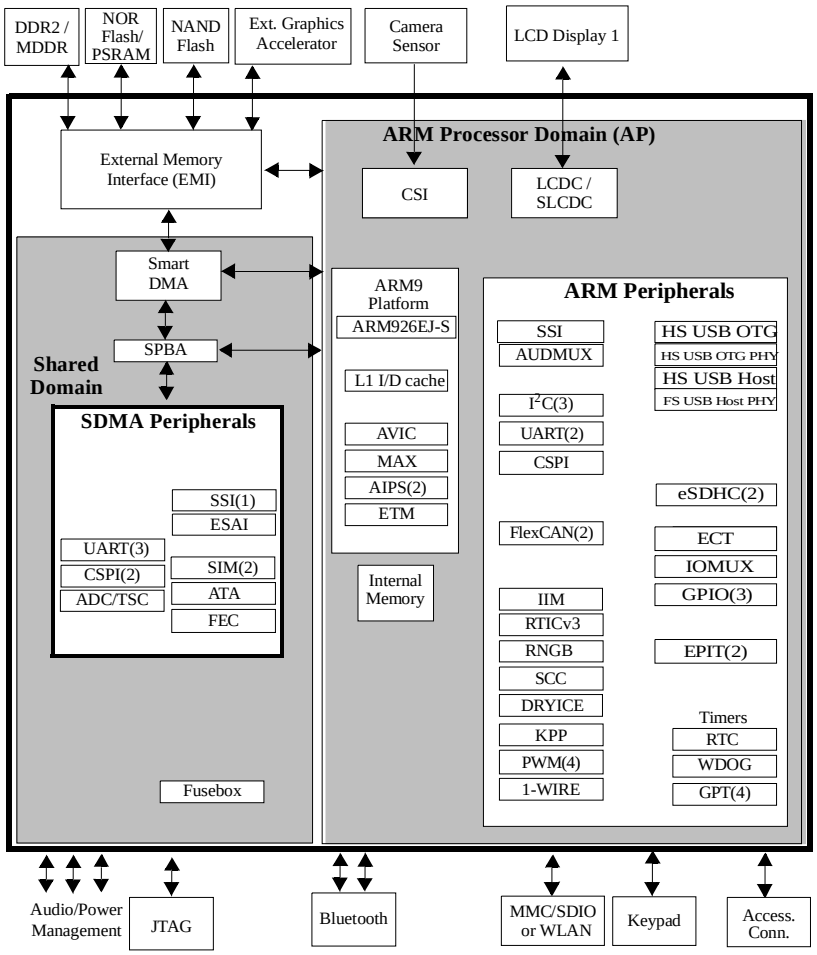


Figure 1. i.MX25 Simplified Interface Block Diagram

NOTE

The term ‘OVDD’ in this section refers to the associated supply rail of an input or output. The association is shown in the “Signal Multiplexing” chapter of the reference manual.

3.5.1 DDR I/O DC Parameters

The DDR pad type is configured by the IOMUXC_SW_PAD_CTL_GRP_DDRTYPE register (see the External Signals and Pin Multiplexing chapter of the *i.MX25 Reference Manual* for details).

3.5.1.1 DDR_TYPE = 00 Standard Setting DDR I/O DC Parameters

Table 17 shows the I/O parameters for mobile DDR. These settings are suitable for mDDR and DDR2 1.8V (± 5%) applications.

Table 17. Mobile DDR I/O DC Electrical Characteristics

DC Electrical Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
High-level output voltage	Voh	I_{OH} = –1mA I_{OH} = Specified Drive	OVDD – 0.08 0.8 × OVDD	—	—	V
Low-level output voltage	Vol	I_{OL} = 1mA I_{OL} = Specified Drive	—	—	0.08 0.2 × OVDD	V
High-level output current	I Ioh	Voh = 0.8 × OVDDV Standard Drive High Drive Max. Drive	 –3.6 –7.2 –10.8	—	—	 mA
Low-level output current	I Iol	Vol = 0.2 × OVDDV Standard Drive High Drive Max. Drive	 3.6 7.2 10.8	—	—	 mA
High-level DC CMOS input voltage	VIH	—	0.7 × OVDD	OVDD	OVDD+0.3	V
Low-level DC CMOS input voltage	VIL	—	–0.3	0	0.3 × OVDD	V
Differential receiver VTH+	VTH+	—		—	100	mV
Differential receiver VTH-	VTH-		–100	—	—	mV
Input current (no pull-up/down)	IIN	VI = 0 VI = OVDD	—	—	110 60	nA
High-impedance I/O supply current	Icc-ovdd	VI = OVDD or 0	—	—	990	nA
High-impedance core supply current	Icc-vddi	VI = VDD or 0	—	—	1220	nA

Table 21. Slow I/O AC Parameters (continued)

Parameter	Symbol	Test Voltage	Test Capacitance	Min. Rise/Fall	Typ. Rise/Fall	Max. Rise/Fall	Units
Output enable to output valid delay[1] (max. drive), 50%–50%	tpv	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	2.13/2.01 2.65/2.46 2.31/2.45 2.95/3.01	3.3/3.045 4.038/3.639 3.76/4.00 4.81/4.82	5.072/4.609 6.142/5.423 6.11/6.47 7.81/7.73	ns
Output enable to output valid delay[1] (high drive), 50%–50%	tpv	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	2.56/2.43 3.55/3.21 2.85/2.90 3.87/3.78	3.91/3.604 5.21/4.598 4.65/4.64 6.31/5.95	5.937/5.36 7.776/6.694 7.58/7.44 10.3/9.43	
Output enable to output valid delay[1] (standard drive), 50%–50%	tpv	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	3.60/3.28 5.50/4.81 4.04/3.94 5.85/5.56	5.35/4.70 7.93/6.603 6.65/6.21 9.47/8.49	7.97/6.836 11.58/9.338 10.9/9.22 15.5/13.3	
Output enable to output valid delay[1] (max. drive), 40%–60%	tpv	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	2.152/1.7 2.6/2.07 2.28/2.46 2.83/2.93	3.25/2.68 3.88/3.17 3.62/3.92 4.50/4.62	4.93/4.162 5.842/4.846 5.77/6.24 7.20/7.32	ns
Output enable to output valid delay[1] (high drive), 40%–60%	tpv	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	2.497/2.036 3.254/2.647 2.71/2.81 3.59/3.56	3.75/3.135 4.8/3.9 4.31/4.23 5.75/5.54	5.633/4.782 7.117/5.84 6.89/7.01 9.23/8.71	
Output enable to output valid delay[1] (standard drive), 40%–60%	tpv	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	3.326/2.7 4.81/3.85 3.73/3.69 5.16/4.99	4.9/3.9 6.9/5.4 6.04/5.77 8.28/7.61	7.269/5.95 10.12/7.86 9.81/9.11 13.4/11.8	
Output pad slew rate[2] (max. drive)	tps	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	0.79/1.12 0.49/0.73 0.30/0.42 0.20/0.29	1.30/1.77 0.84/1.23 0.54/0.73 0.35/0.50	2.02/2.58 1.19/1.58 0.91/1.20 0.60/0.80	V/ns
Output pad slew rate[2] (high drive)	tps	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	0.48/0.72 0.27/0.42 0.19/0.28 0.12/0.18	0.76/1.10 0.41/0.62 0.34/0.49 0.34/0.49	1.17/1.56 0.63/0.86 0.58/0/79 0.36/0.49	
Output pad slew rate[2] (standard drive)	tps	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	0.25/0.40 0.14/0.21 0.12/0.18 0.07/0.11	0.40/0.59 0.21/0.32 0.20/0.30 0.11/0.17	0.60/0.83 0.32/0.44 0.34/0.47 0.20/0.27	

Table 21. Slow I/O AC Parameters (continued)

Parameter	Symbol	Test Voltage	Test Capacitance	Min. Rise/Fall	Typ. Rise/Fall	Max. Rise/Fall	Units
Output pad dI/dt[3] (max. drive)	tdit	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	15 16 7 7	36 38 21 22	76 80 56 58	mA /ns
Output pad dI/dt[3] (high drive)	tdit	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	8 9 5 5	20 21 14 15	45 47 38 40	
Output pad dI/dt[3] (standard drive)	tdit	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	4 4 2 2	10 10 7 7	22 23 18 19	
Input pad propagation delay without hysteresis, 50%–50%[4]	tpi	—	1.6 pF	0.82/0.47 0.74/1	1.1/0.76 1.1/1.5	1.6/1.04 1.75/2.16	ns
Input pad propagation delay with hysteresis, 50%–50%[4]	tpi	—	1.6 pF	1.1/1.3 1.75/1.63	1.43/1.6 2.67/2.22	2/2 2.92/3	
Input pad propagation delay without hysteresis, 40%–60%[4]	tpi	—	1.6 pF	1.62/1.28 1.82/1.55	1.9/1.56 2.28/1.87	2.38/1.82 2.95/2.54	
Input pad propagation delay with hysteresis, 40%–60%[4]	tpi	—	1.6 pF	1.88/2.1 2.4/2.6	2.2/2.4 3/3.07	2.7/2.75 3.77/3.71	
Input pad transition times without hysteresis[4]	trfi	—	1.6 pF	0.16/0.12	0.23/0.18	0.33/0.29	
Input pad transition times with hysteresis[4]	trfi		1.6 pF	0.16/0.13	0.22/0.18	0.33/0.29	
Maximum input transition times[5]	trm	—	—	—	—	25	ns

1 Maximum condition for tpr, tpo, and tpv: wcs model, 1.1 V, I/O 3.0 V (3.0–3.6 V range) or 1.65 V (1.65–1.95 V range), and 105 °C. Minimum condition for tpr, tpo, and tpv: bcs model, 1.3 V, I/O 3.6 V (3.0–3.6 V range) or 1.95 V (1.65–1.95 V range), and –40 °C. Input transition time from core is 1 ns (20%–80%).

2 Minimum condition for tps: wcs model, 1.1 V, I/O 3.0 V (3.0–3.6 V range) or 1.65 V (1.65–1.95 V range), and 105 °C. tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.

3 Maximum condition for tdit: bcs model, 1.3 V, I/O 3.6 V (3.0–3.6 V range) or 1.95 V (1.65–1.95 V range), and –40 °C.

4 Maximum condition for tpi and trfi: wcs model, 1.1 V, I/O 3.0 V (3.0–3.6 V range) or 1.65 V (1.65–1.95 V range), and 105 °C. Minimum condition for tpi and trfi: bcs model, 1.3 V, I/O 3.6 V or 1.95 V (1.65–1.95 V range), and –40 °C. Input transition time from pad is 5 ns (20%–80%).

5 Hysteresis mode is recommended for input with transition time greater than 25 ns.

3.6.2 Fast I/O AC Parameters

Table 22 shows the fast I/O AC parameters for OVDD = 1.65–1.95 V.

Table 22. Fast I/O AC Parameters for OVDD = 1.65–1.95 V

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	—	60	%
Output pad transition times[1] (max. drive)	tpr	25 pF 50 pF	0.88/0.77 1.45/1.24	1.36/1.10 2.20/1.80	2.10/1.70 3.50/2.70	ns
Output pad transition times[1] (high drive)	tpr	25 pF 50 pF	1.10/0.92 1.84/1.54	1.65/1.33 2.80/2.20	2.64/2.10 4.40/3.30	ns
Output pad transition times[1] (standard drive)	tpr	25 pF 50 pF	1.60/1.35 2.74/2.26	2.47/1.95 4.20/3.20	3.99/3.10 6.56/4.86	ns
Output pad propagation delay[1] (max. drive), 50%–50%	tpo	25 pF 50 pF	1.64/1.53 2.15/2.01	2.68/2.41 3.47/3.08	4.25/3.74 5.50/4.77	ns
Output pad propagation delay[1] (high drive), 50%–50%	tpo	25 pF 50 pF	1.82/1.71 2.46/2.29	2.98/2.66 3.96/3.49	4.74/4.13 6.27/5.37	ns
Output pad propagation delay[1] (standard drive), 50%–50%	tpo	25 pF 50 pF	2.24/2.06 3.17/2.92	3.63/3.15 5.09/4.41	5.73/4.84 8.06/6.75	ns
Output pad propagation delay[1] (max. drive), 40%–60%	tpo	25 pF 50 pF	1.67/1.58 2.09/1.98	2.63/2.38 3.30/2.97	4.06/3.63 5.14/4.51	ns
Output pad propagation delay[1] (high drive), 40%–60%	tpo	25 pF 50 pF	1.94/1.73 2.34/2.22	2.89/2.61 3.69/3.30	4.49/3.97 5.76/5.01	ns
Output pad propagation delay[1] (standard drive), 40%–60%	tpo	25 pF 50 pF	2.15/1.99 2.94/2.74	3.39/2.99 4.65/4.07	5.28/4.53 7.28/6.13	ns
Output enable to output valid delay[1] (max. drive), 50%–50%	tpv	25 pF 50 pF	1.87/1.70 2.36/2.16	3.06/2.71 3.83/3.37	4.97/4.30 6.18/5.30	ns
Output enable to output valid delay[1] (high drive), 50%–50%	tpv	25 pF 50 pF	2.05/1.88 2.68/2.45	3.67/2.98 4.32/3.78	5.46/4.72 6.98/5.92	ns
Output enable to output valid delay[1] (standard drive), 50%–50%	tpv	25 pF 50 pF	2.49/2.25 3.40/3.08	4.06/3.50 5.50/4.73	6.57/5.49 8.88/7.37	ns
Output enable to output valid delay[1] (max. drive), 40%–60%	tpv	25 pF 50 pF	1.90/1.74 2.30/2.13	3.00/2.69 3.65/3.24	4.76/4.18 5.79/5.02	ns
Output enable to output valid delay[1] (high drive), 40%–60%	tpv	25 pF 50 pF	2.06/1.90 2.56/2.37	3.28/2.33 4.04/3.59	5.21/4.54 6.43/5.54	ns
Output enable to output valid delay[1] (standard drive), 40%–60%	tpv	25 pF 50 pF	2.39/2.18 3.16/2.89	3.80/3.18 5.03/4.37	6.05/5.14 8.02/6.72	ns
Output pad slew rate[2] (max. drive)	tps	25 pF 50 pF	0.40/0.57 0.25/0.36	0.72/0.97 0.43/0.61	1.2/1.5 0.72/0.95	V/ns
Output pad slew rate[2] (high drive)	tps	25 pF 50 pF	0.38/0.48 0.20/0.30	0.59/0.81 0.34/0.50	0.98/1.27 0.56/0.72	V/ns
Output pad slew rate[2] (standard drive)	tps	25 pF 50 pF	0.23/0.32 0.13/0.20	0.40/0.55 0.23/0.34	0.66/0.87 0.38/0.52	V/ns

3.6.3.2 DDR_TYPE = 01 SDRAM I/O AC Parameters and Requirements

Table 27 shows AC parameters for SDRAM I/O.

Table 27. AC Parameters for SDRAM I/O

Parameter	Symbol	Load Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	50	60	%
Clock frequency[1]	f	—	—	—	133	MHz
Output pad transition times[1] (max. drive)	tpr	25 pF 50 pF	0.82/0.87 1.56/1.67	1.14/1.13 2.13/2.09	1.62/1.50 3.015/2.77	ns
Output pad transition times[1] (high drive)	tpr	25 pF 50 pF	1.23/1.31 2.31/2.47	1.71/1.68 3.22/3.12	2.39/2.22 4.53/4.16	ns
Output pad transition times[1] (standard drive)	tpr	25 pF 50 pF	2.44/2.60 4.65/4.99	3.38/3.27 6.38/6.23	4.73/4.38 9.05/8.23	ns
Output pad propagation delay[1] (max. drive), 50%–50%	tpo	15 pF 35 pF	0.97/1.19 2.85/3.21	1.69/0.75 2.02/2.30	2.17/2.46 2.93/3.27	ns
Output pad propagation delay[1] (high drive), 50%–50%	tpo	15 pF 35 pF	1.15/1.39 3.57/3.91	1.72/1.93 2.54/2.85	2.51/2.77 3.66/3.97	ns
Output pad propagation delay[1] (standard drive), 50%–50%	tpo	15 pF 35 pF	2.01/1.57 5.73/6.05	2.45/2.69 4.10/4.51	3.54/3.77 5.84/6.13	ns
Output pad propagation delay[1] (max. drive), 40%–60%	tpo	15 pF 35 pF	1.06/1.26 1.38/1.38	1.53/1.73 1.96/2.23	2.18/2.47 2.78/3.12	ns
Output pad propagation delay[1] (high drive), 40%–60%	tpo	15 pF 35 pF	1.15/1.20 1.75/1.67	1.72/1.93 2.37/2.66	2.45/2.71 3.35/3.67	ns
Output pad propagation delay[1] (standard drive), 40%–60%	tpo	15 pF 35 pF	1.91/2.01 2.88/2.56	2.30/2.52 3.59/3.97	3.26/3.50 5.06/5.36	ns
Output enable to output valid delay[1] (max. drive), 50%–50%	tpv	15 pF 35 pF	0.90/1.27 1.07/1.77	1.44/1.89 1.66/2.51	2.19/2.87 2.51/3.69	ns
Output enable to output valid delay[1] (high drive), 50%–50%	tpv	15 pF 35 pF	1.01/1.48 1.37/2.33	1.58/2.16 2.06/3.09	2.38/3.23 3.06/4.46	ns
Output enable to output valid delay[1] (standard drive), 50%–50%	tpv	15 pF 35 pF	1.32/2.14 2.04/3.67	2.02/3.00 3.00/4.91	3.01/4.36 4.40/6.90	ns
Output enable to output valid delay[1] (max. drive), 40%–60%	tpv	15 pF 35 pF	1.03/1.34 1.16/1.74	1.54/1.94 1.74/2.44	2.26/2.88 2.55/3.54	ns
Output enable to output valid delay[1] (high drive), 40%–60%	tpv	15 pF 35 pF	1.11/1.51 1.39/2.10	1.65/2.15 2.03/2.89	2.43/3.16 2.95/4.13	ns
Output enable to output valid delay[1] (standard drive), 40%–60%	tpv	15 pF 35 pF	1.35/2.03 1.91/3.23	1.99/2.83 2.76/4.30	2.89/4.03 3.98/6.01	ns
Output pad slew rate[2] (max. drive)	tps	25 pF 50 pF	1.11/1.20 0.97/0.65	1.74/1.75 0.92/0.94	2.42/2.46 1.39/1.30	V/ns
Output pad slew rate[2] (high drive)	tps	25 pF 50 pF	0.76/0.80 0.40/0.43	1.16/1.19 0.61/0.63	1.76/1.66 0.93/0.87	V/ns

3.7.2.4 UDMA Out-Transfer Timing

Figure 18 shows the timing for start of UDMA out-transfer.

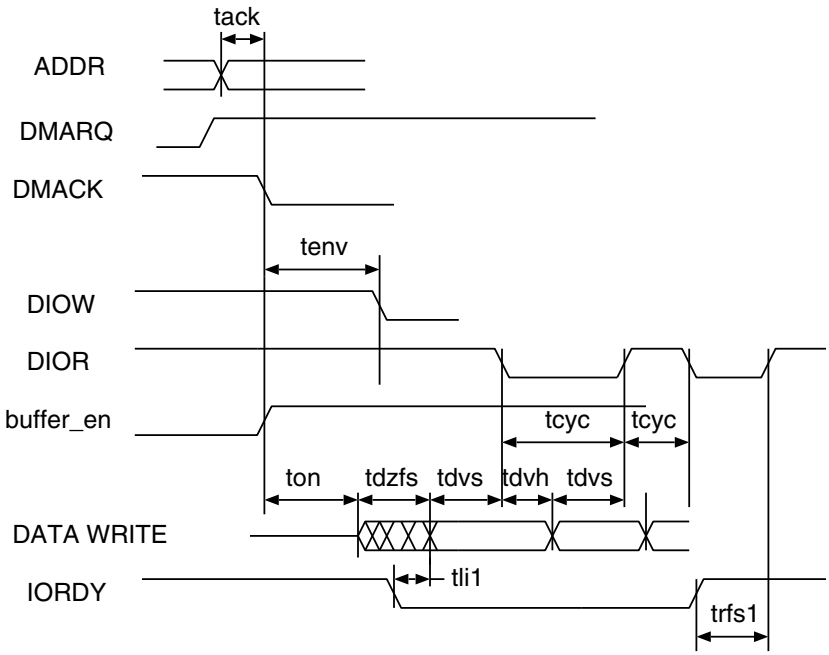


Figure 18. Timing for UDMA Out-Transfer Start

Figure 19 shows timing for host-terminated UDMA out-transfer.

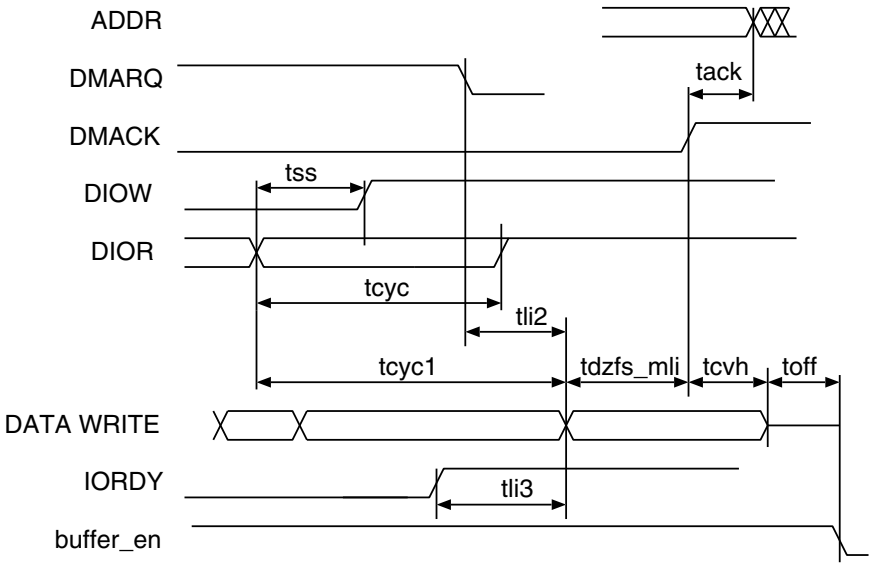


Figure 19. Timing for Host-Terminated UDMA Out-Transfer

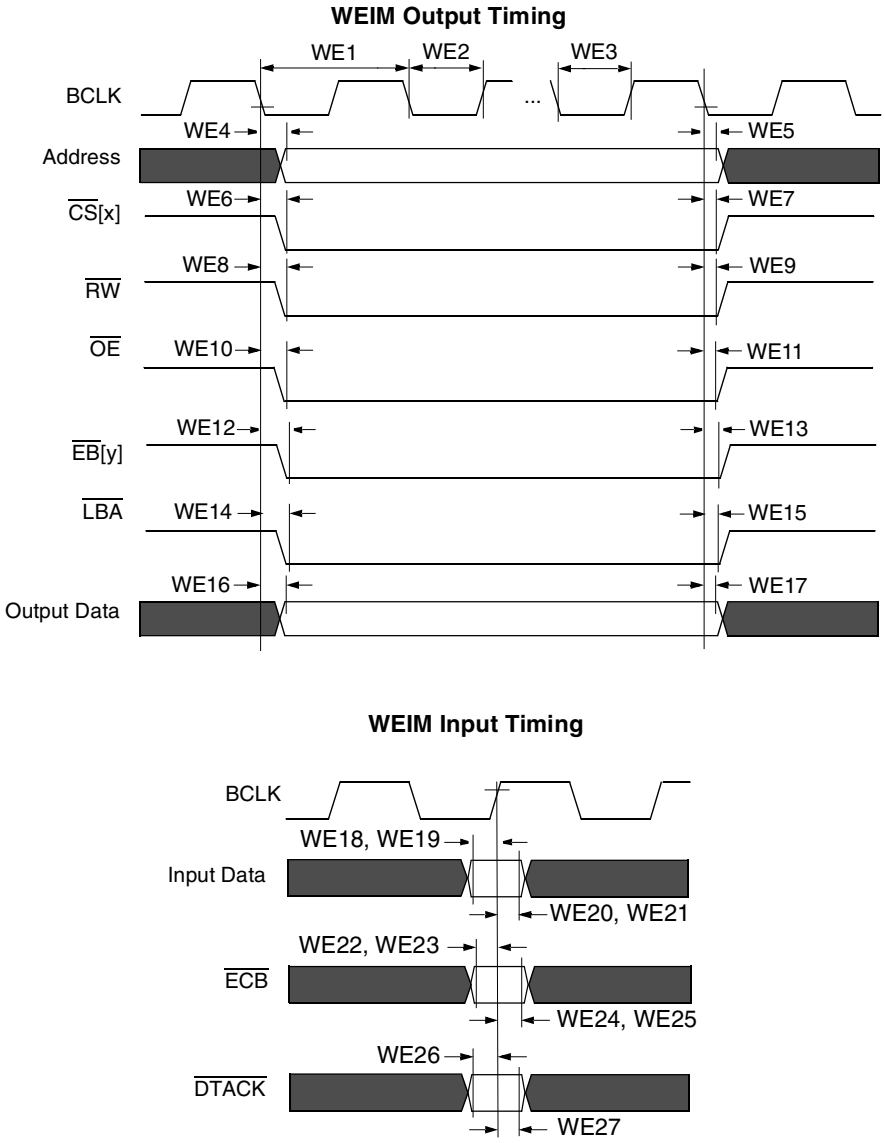


Figure 38. WEIM Bus Timing Diagram

Table 56. WEIM Bus Timing Parameters[1]

ID	Parameter	Min.	Max.	Unit
WE1	BCLK cycle time[2]	14.5	—	ns
WE2	BCLK low-level width[2]	7	—	ns
WE3	BCLK high-level width[2]	7	—	ns
WE4	Clock fall to address valid	15	21	ns
WE5	Clock rise/fall to address invalid	22	25	ns
WE6	Clock rise/fall to $\overline{CS}$[x] valid	15	19	ns
WE7	Clock rise/fall to $\overline{CS}$[x] invalid	3.3	5	ns

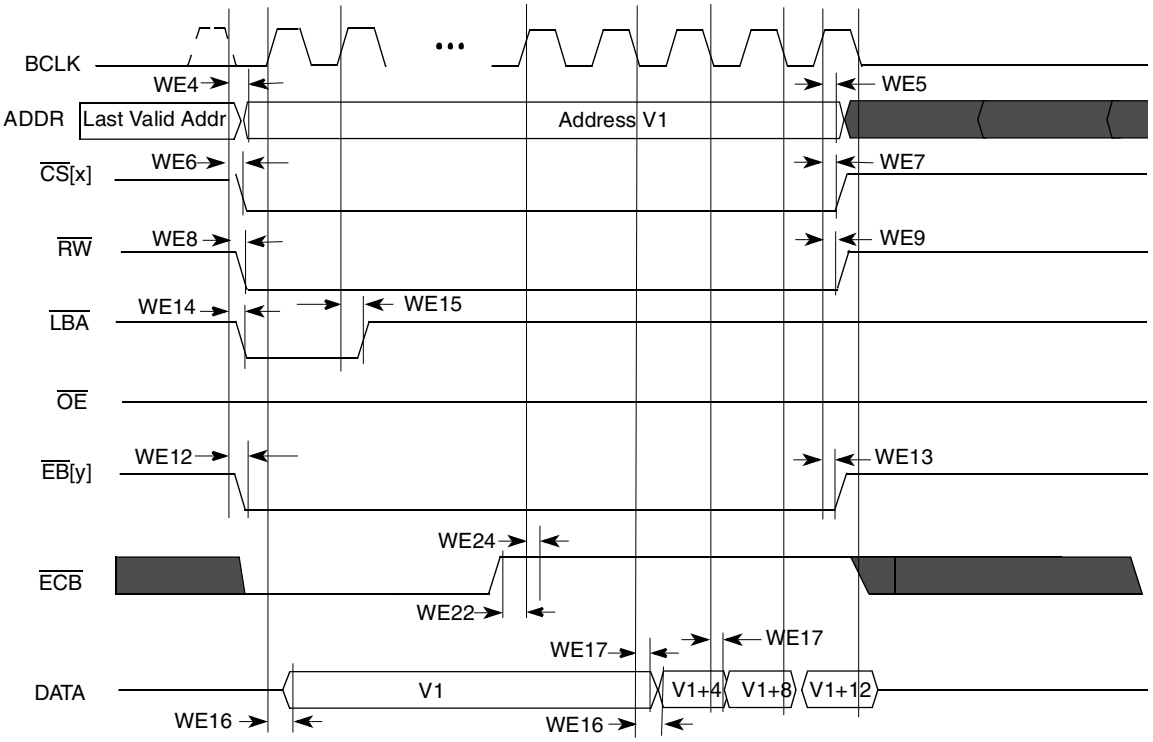


Figure 42. Synchronous Memory TIming Diagram for Burst Write Access—BCS=1, WSC=4, SYNC=1, DOL=0, PSR=1

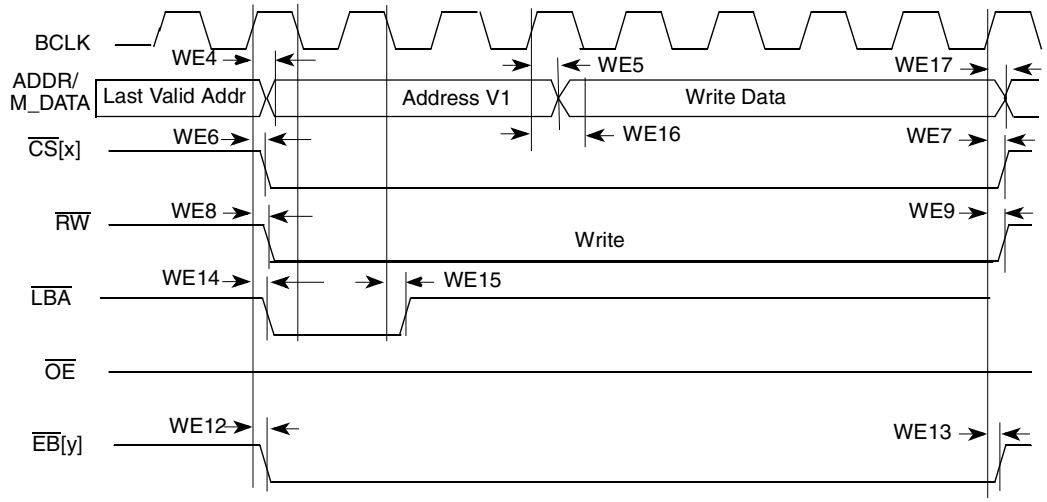


Figure 43. Muxed A/D Mode Timing Diagram for Synchronous Write Access—WSC=7, LBA=1, LBN=1, LAH=1

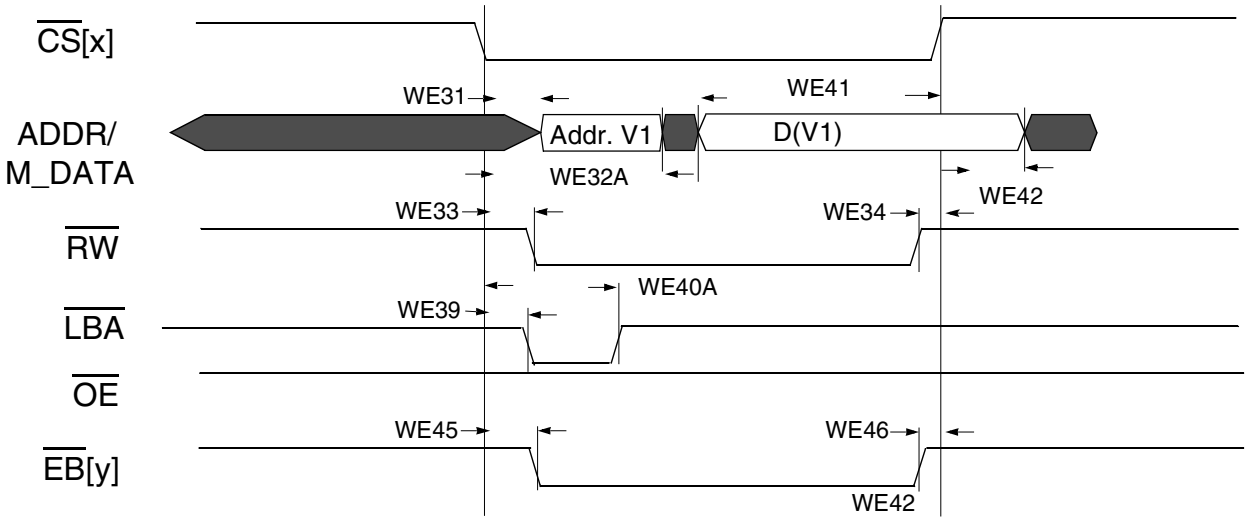


Figure 48. Asynchronous A/D Mux Write Access

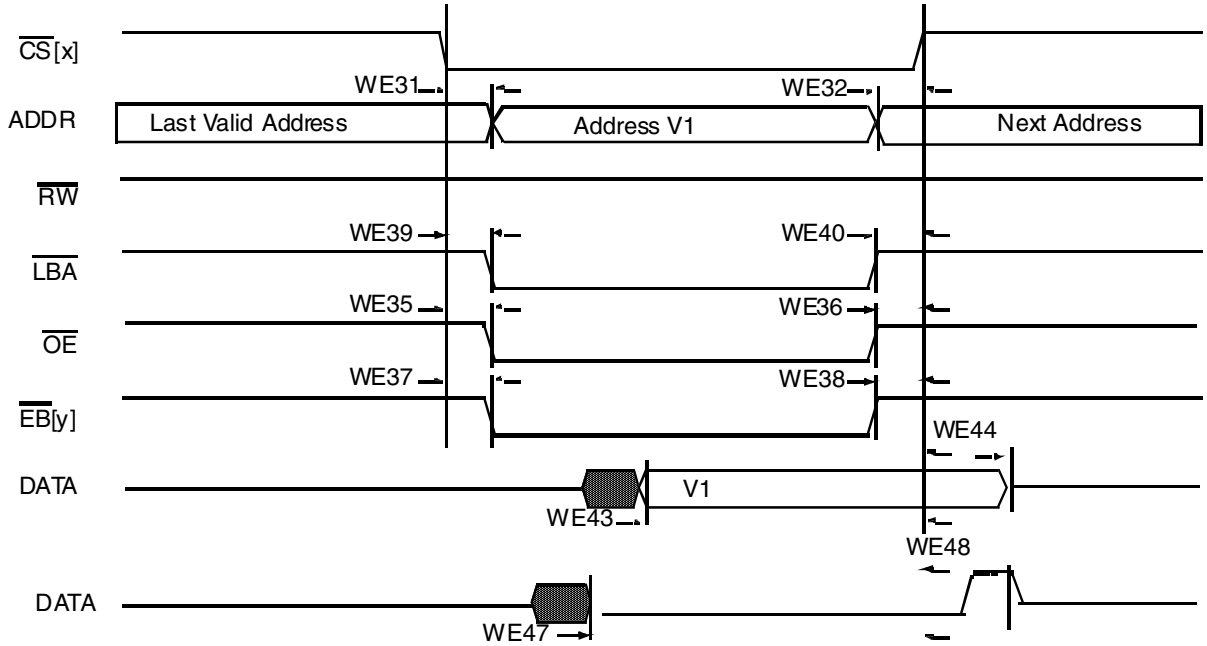


Figure 49. DTACK Read Access

Table 57. WEIM Asynchronous Timing Parameters Relative to Chip Select Table

Ref No.	Parameter	Determination By Synchronous Measured Parameters[1]	Min	Max (If 133 MHz is supported by SoC)	Unit
WE31	$\overline{CS}$[x] valid to Address Valid	WE4 – WE6 – CSA[2]	—	3 – CSA	ns
WE32	Address Invalid to $\overline{CS}$[x] invalid	WE7 – WE5 – CSN[3]	—	3 – CSN	ns

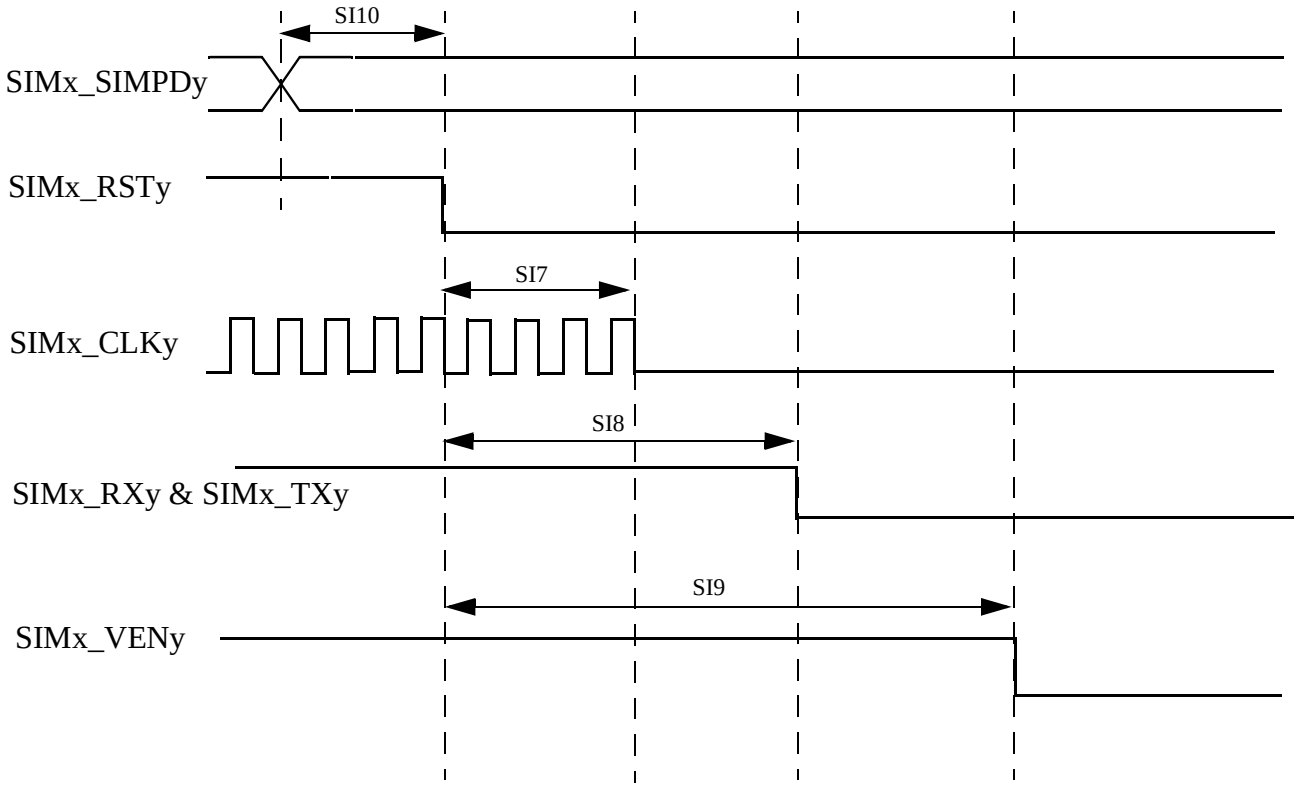


Figure 71. SmartCard Interface Power Down AC Timing

Table 77. Timing Requirements for Power-down Sequence

ID	PARAMETER	SYMBOL	Min.	Max.	Unit
SI7	SIM reset to SIM clock stop	$S_{rst2clk}$	0.9 × 1/Fckil	1.1 × 1/Fckil	ns
SI8	SIM reset to SIM Tx data low	$S_{rst2dat}$	1.8 × 1/Fckil	2.2 × 1/Fckil	ns
SI9	SIM reset to SIM voltage enable low	$S_{rst2ven}$	2.7 × 1/Fckil	3.3 × 1/Fckil	ns
SI10	SIM presence detect to SIM reset low	S_{pd2rst}	0.9 × 1/Fckil	1.1 × 1/Fckil	ns

3.7.15 System JTAG Controller (SJC) Timing

Figure 72 through Figure 75 show respectively the test clock input, boundary scan, test access port, and $\overline{\text{TRST}}$ timings for the SJC. Table 78 describes the SJC timing parameters (SJ1–SJ13) indicated in the figures.

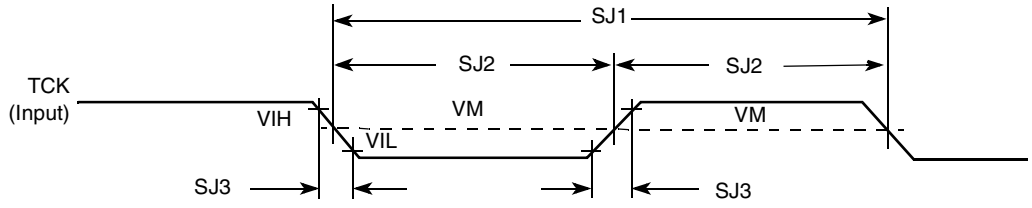


Figure 72. Test Clock Input Timing Diagram

Table 80. SLCDC Parallel Interface Timing Parameters

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{cyc}	Parallel clock cycle time	78 (±) t_{prop}	—	4923	ns
t_{ds}	Data setup time	(t_{cyc} / 2) (±) t_{prop}	—	—	—
t_{dh}	Data hold time	(t_{cyc} / 2) (±) t_{prop}	—	—	—
t_{rss}	Register select setup time	(t_{cyc} / 2) (±) t_{prop}	—	—	—
t_{rsh}	Register select hold time	(t_{cyc} / 2) (±) t_{prop}	—	—	—

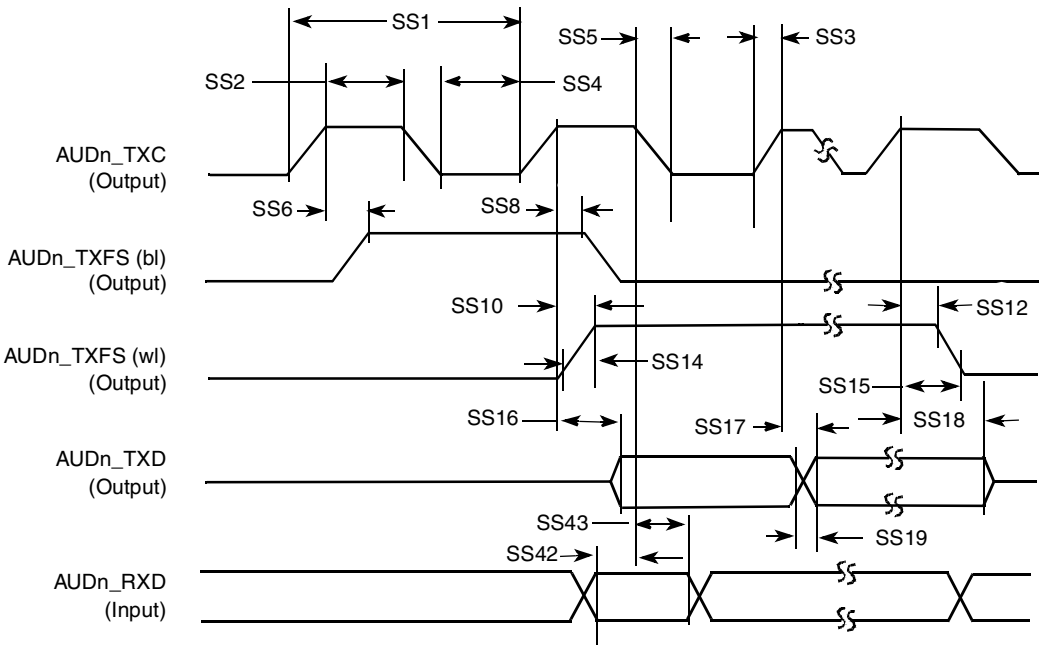
3.7.17 Synchronous Serial Interface (SSI) Timing

The following subsections describe SSI timing in four cases:

- Transmitter with external clock
- Receiver with external clock
- Transmitter with internal clock
- Receiver with internal clock

3.7.17.1 SSI Transmitter Timing with Internal Clock

Figure 78 shows the timing for SSI transmitter with internal clock, and Table 81 describes the timing parameters (SS1–SS52).



Note: SRXD Input in Synchronous mode only

Figure 78. SSI Transmitter with Internal Clock Timing Diagram

Table 83. SSI Transmitter Timing with External Clock

ID	Parameter	Min.	Max.	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36.0	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns
SS25	(Tx/Rx) CK clock low period	36.0	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS27	FS (bl) low/ high setup before (Tx) CK falling	–10.0	15.0	ns
SS29	FS (bl) low/ high setup before (Tx) CK falling	10.0	—	ns
SS31	FS (wl) low/ high setup before (Tx) CK falling	–10.0	15.0	ns
SS33	FS (wl) low/ high setup before (Tx) CK falling	10.0	—	ns
SS37	(Tx) CK high to STXD valid from high impedance	—	15.0	ns
SS38	(Tx) CK high to STXD high/low	—	15.0	ns
SS39	(Tx) CK high to STXD high impedance	—	15.0	ns
Synchronous External Clock Operation				
SS44	SRXD setup before (Tx) CK falling	10.0	—	ns
SS45	SRXD hold after (Tx) CK falling	2.0	—	ns
SS46	SRXD rise/fall time	—	6.0	ns

Note:

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables figures.
- All timings are on pads when SSI is being used for data transfer.
- ”Tx” and “Rx” refer, respectively, to the transmit and receive sections of the SSI.
- For internal frame sync operation using external clock, the FS timing is the same as that of Tx data (for example, during AC97 mode of operation).

3.7.17.4 SSI Receiver Timing with External Clock

Figure 81 shows the timing for SSI receiver with external clock. Table 84 describes the timing parameters (SS22–SS41) used in the figure.

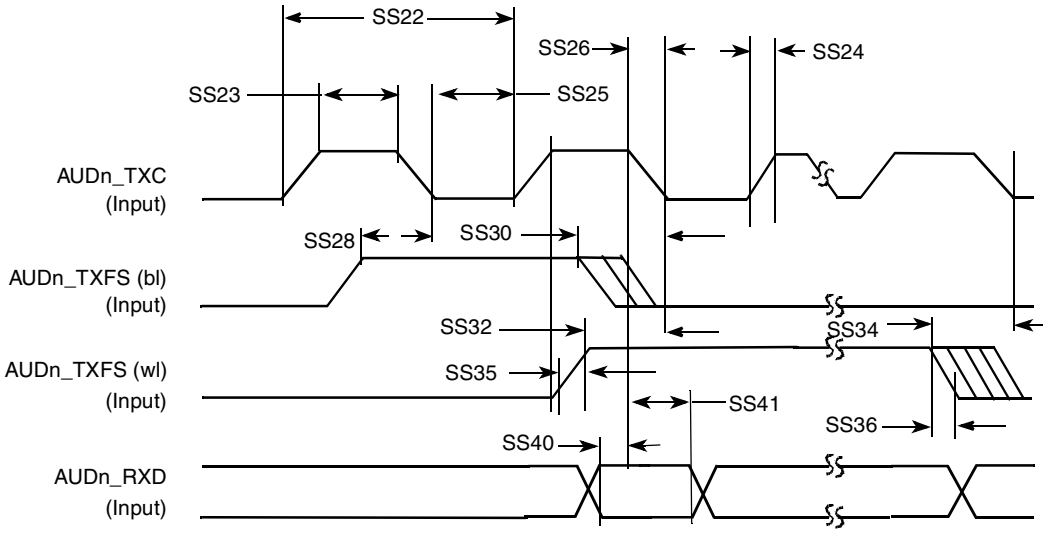


Figure 81. SSI Receiver with External Clock Timing Diagram

Table 84. SSI Receiver Timing with External Clock

ID	Parameter	Min.	Max.	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36.0	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns
SS25	(Tx/Rx) CK clock low period	36.0	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS28	FS (bl) low/high setup before (Tx) CK falling	–10.0	15.0	ns
SS30	FS (bl) low/high setup before (Tx) CK falling	10.0	—	ns
SS32	FS (wl) low/high setup before (Tx) CK falling	–10.0	15.0	ns
SS34	FS (wl) low/high setup before (Tx) CK falling	10.0	—	ns
SS35	(Tx/Rx) External FS rise time	—	6.0	ns
SS36	(Tx/Rx) External FS fall time	—	6.0	ns
SS40	SRXD setup time before (Rx) CK low	10.0	—	ns
SS41	SRXD hold time after (Rx) CK low	2.0	—	ns

Note:

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on pads when SSI is being used for data transfer.

- ”Tx” and “Rx” refer, respectively, to the transmit and receive sections of the SSI.
- For internal frame sync operation using external clock, the FS timing is the same as that of Tx data (for example, during AC97 mode of operation).

3.7.18 Touchscreen ADC Electrical Specifications and Timing

This section describes the electrical specifications, operation modes, and timing of the touchscreen ADC.

3.7.18.1 ADC Electrical Specifications

Table 85 shows the electrical specifications for the touchscreen ADC.

Table 85. Touchscreen ADC Electrical Specifications

Parameter	Conditions	Min.	Typ.	Max.	Unit
ADC					
Input sampling capacitance (C_S)	No pin/pad capacitance included	—	2	—	pF
Resolution	—		12		bits
Analog Bias					
Resistance value between *ref* and *agndref*	—	—	1.6	—	kΩ
Timing Characteristics					
Sampling rate (fs)	—	—	—	125	kHz
Internal ADC/TSC clock frequency	—	—	—	1.75	MHz
Multiplexed inputs	—		8		—
Data latency	—		12.5		clk cycles
Power-up time[1]	—		14		clk cycles
clk falling edge to sampling delay (tsd)	—	2	5	8	ns
soc input setup time before clk rising edge (tsocst)	—	0.5	1	3	ns
soc input hold time after clk rising edge (tsochld)	—	2	3	6	ns
eoc delay after clk rise edge (teoc)	With a 250 pF load	2	7	10	ns
Valid data out delay after eoc rise edge (tdata)	With a 250 pF load	5	8	13	ns
Power Supply Requirements					
Current consumption[2] NVCC_ADC QV_{DD}	—	—	—	2.1 0.5	mA mA

Figure 83 shows the timing for ADC normal operation.

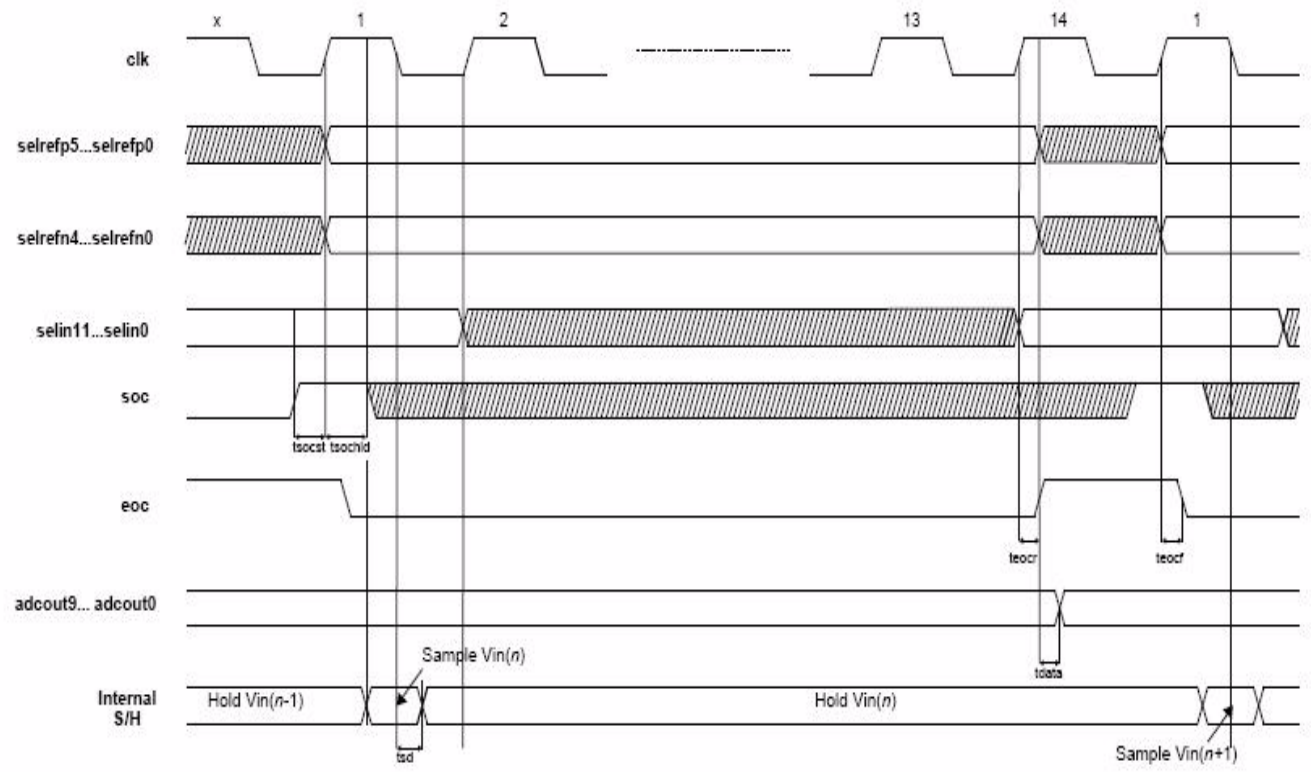


Figure 83. Timing for ADC Normal Operation

When the ADC is used so that the idle clock cycles occur between conversions (due to the negation of *soc*), the *selin* inputs must be stable at least 1 clock cycle before the clock's rising edge where the *soc* signal is latched. Also, *selrefp* and *selrefn* must be stable by the time the *soc* signal is latched. These conditions are met if *enadc=1* and *reset=0* throughout ADC operation, including the idle cycles. If the conditions are not met, or if power is lost during ADC operation, then a new start-up sequence is required for ADC to become operational again.

3.7.19.1 UART RS-232 Serial Mode Timing

3.7.19.1.1 UART Transmit Timing in RS-232 Serial Mode

Figure 85 shows the UART transmit timing in RS-232 serial mode, showing only 8 data bits and 1 stop bit. Table 86 describes the timing parameter (UA1) shown in the figure.

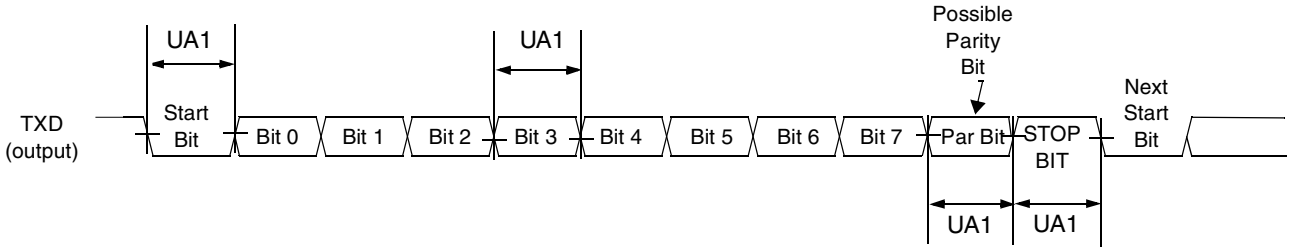


Figure 85. UART RS-232 Serial Mode Transmit Timing Diagram

Table 86. UART RS-232 Serial Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud\_rate}$ [1] – T_{ref_clk} [2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—

1 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

2 T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

3.7.19.1.2 UART Receive Timing in RS-232 Serial Mode

Figure 86 shows the UART receive timing in RS-232 serial mode, showing only 8 data bits and 1 stop bit. Table 87 describes the timing parameter (UA2) shown in the figure.

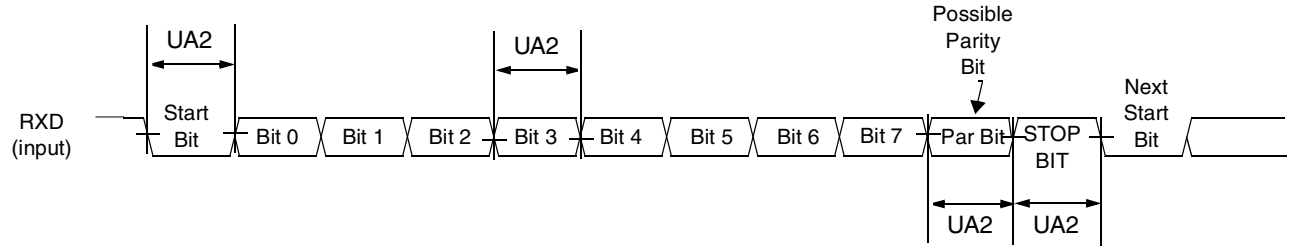


Figure 86. UART RS-232 Serial Mode Receive Timing Diagram

Table 87. UART RS-232 Serial Mode Receive Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
UA2	Receive bit time[1]	t_{Rbit}	$1/F_{baud\_rate}$ [2] – $1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$	—

1 The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.

2 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

4.3 Signal Contact Assignments—17 x 17 mm, 0.8 mm Pitch

Table 101 lists the 17×17 mm package i.MX25 signal contact assignments.

Table 101. 17×17 mm Package i.MX25 Signal Contact Assignment

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuration after Reset[1]
A0	A18	EMI2	DDR	OUTPUT	Low
A1	B17	EMI2	DDR	OUTPUT	Low
A2	C17	EMI2	DDR	OUTPUT	Low
A3	B18	EMI2	DDR	OUTPUT	Low
A4	C20	EMI2	DDR	OUTPUT	Low
A5	A19	EMI2	DDR	OUTPUT	Low
A6	C19	EMI2	DDR	OUTPUT	Low
A7	B19	EMI2	DDR	OUTPUT	Low
A8	D18	EMI2	DDR	OUTPUT	Low
A9	C18	EMI2	DDR	OUTPUT	Low
A10	A2	EMI1	DDR	OUTPUT	Low
MA10	D16	EMI2	DDR	OUTPUT	Low
A11	D20	EMI2	DDR	OUTPUT	Low
A12	D17	EMI2	DDR	OUTPUT	Low
A13	D19	EMI2	DDR	OUTPUT	Low
A14	A3	EMI1	DDR	OUTPUT	Low
A15	B4	EMI1	DDR	OUTPUT	Low
A16	C6	EMI1	DDR	OUTPUT	Low
A17	B5	EMI1	DDR	OUTPUT	Low
A18	D7	EMI1	DDR	OUTPUT	Low
A19	A4	EMI1	DDR	OUTPUT	Low
A20	B6	EMI1	DDR	OUTPUT	Low
A21	C7	EMI1	DDR	OUTPUT	Low
A22	A5	EMI1	DDR	OUTPUT	Low
A23	A6	EMI1	DDR	OUTPUT	Low
A24	B7	EMI1	DDR	OUTPUT	Low
A25	A7	EMI1	DDR	OUTPUT	Low
SD0	A12	EMI1	DDR	INPUT	Keeper
SD1	C13	EMI1	DDR	INPUT	Keeper
SD2	B13	EMI1	DDR	INPUT	Keeper

Table 101. 17×17 mm Package i.MX25 Signal Contact Assignment (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuration after Reset[1]
SD3	D14	EMI1	DDR	INPUT	Keeper
SD4	D13	EMI1	DDR	INPUT	Keeper
SD5	A13	EMI1	DDR	INPUT	Keeper
SD6	D12	EMI1	DDR	INPUT	Keeper
SD7	A10	EMI1	DDR	INPUT	Keeper
SD8	B9	EMI1	DDR	INPUT	Keeper
SD9	D10	EMI1	DDR	INPUT	Keeper
SD10	B10	EMI1	DDR	INPUT	Keeper
SD11	C10	EMI1	DDR	INPUT	Keeper
SD12	C9	EMI1	DDR	INPUT	Keeper
SD13	A9	EMI1	DDR	INPUT	Keeper
SD14	D9	EMI1	DDR	INPUT	Keeper
SD15	A8	EMI1	DDR	INPUT	Keeper
SDBA1	A16	EMI2	DDR	OUTPUT	Low
SDBA0	B15	EMI2	DDR	OUTPUT	Low
DQM0	C12	EMI1	DDR	OUTPUT	High
DQM1	C8	EMI1	DDR	OUTPUT	High
RAS	C14	EMI2	DDR	OUTPUT	High
CAS	C16	EMI2	DDR	OUTPUT	High
SDWE	A15	EMI2	DDR	OUTPUT	High
SDCKE0	D15	EMI2	DDR	OUTPUT	High
SDCKE1	C15	EMI2	DDR	OUTPUT	High
SDCLK	B14	EMI2	DDR	OUTPUT	Low
SDCLK_B	A14	EMI2	DDR	OUTPUT	High
SDQS0	B12	EMI2	DDR	INPUT	Keeper
SDQS1	B8	EMI2	DDR	INPUT	Keeper
EB0	B3	EMI1	DDR	OUTPUT	High
EB1	C5	EMI1	DDR	OUTPUT	High
OE	D6	EMI1	DDR	OUTPUT	High
CS0	C3	EMI1	DDR	OUTPUT	High
CS1	D3	EMI1	DDR	OUTPUT	High
CS2	B16	EMI2	DDR	OUTPUT	High

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