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**What is "Embedded - Microcontrollers"?**

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

**Applications of "Embedded - Microcontrollers"**

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 20MHz |
| Connectivity | I²C, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 25 |
| Program Memory Size | 3.5KB (2K x 14) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 128 x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V |
| Data Converters | A/D 11x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-SSOP (0.209", 5.30mm Width) |
| Supplier Device Package | 28-SSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic16f722a-e-ss |

**TABLE 3-1: STATUS BITS AND THEIR SIGNIFICANCE**

| $\overline{POR}$ | $\overline{BOR}$ | $\overline{TO}$ | $\overline{PD}$ | Condition |
|---|---|---|---|---|
| 0 | x | 1 | 1 | Power-on Reset or LDO Reset |
| 0 | x | 0 | x | Illegal, $\overline{TO}$ is set on $\overline{POR}$ |
| 0 | x | x | 0 | Illegal, $\overline{PD}$ is set on $\overline{POR}$ |
| 1 | 0 | 1 | 1 | Brown-out Reset |
| 1 | 1 | 0 | 1 | WDT Reset |
| 1 | 1 | 0 | 0 | WDT Wake-up |
| 1 | 1 | u | u | $\overline{MCLR}$ Reset during normal operation |
| 1 | 1 | 1 | 0 | $\overline{MCLR}$ Reset during Sleep or interrupt wake-up from Sleep |

**TABLE 3-2: RESET CONDITION FOR SPECIAL REGISTERS[2]**

| Condition | Program Counter | STATUS Register | PCON Register |
|---|---|---|---|
| Power-on Reset | 0000h | 0001 1xxx | ---- --0x |
| $\overline{MCLR}$ Reset during normal operation | 0000h | 000u uuuu | ---- --uu |
| $\overline{MCLR}$ Reset during Sleep | 0000h | 0001 0uuu | ---- --uu |
| WDT Reset | 0000h | 0000 1uuu | ---- --uu |
| WDT Wake-up | PC + 1 | uuu0 0uuu | ---- --uu |
| Brown-out Reset | 0000h | 0001 1uuu | ---- --u0 |
| Interrupt Wake-up from Sleep | PC + 1[1] | uuu1 0uuu | ---- --uu |

**Legend:** u = unchanged, x = unknown, – = unimplemented bit, reads as '0'.

**Note 1:** When the wake-up is due to an interrupt and Global Enable bit (GIE) is set, the return address is pushed on the stack and PC is loaded with the interrupt vector (0004h) after execution of PC + 1.

**2:** If a Status bit is not implemented, that bit will be read as '0'.

## 5.0    LOW DROPOUT (LDO) VOLTAGE REGULATOR

The PIC16F722A/723A devices differ from the PIC16LF722A/723A devices due to an internal Low Dropout (LDO) voltage regulator. The PIC16F722A/723A devices contain an internal LDO, while the PIC16LF722A/723A ones do not.

The lithography of the die allows a maximum operating voltage of 3.6V on the internal digital logic. In order to continue to support 5.0V designs, a LDO voltage regulator is integrated on the die. The LDO voltage regulator allows for the internal digital logic to operate at 3.2V, while I/O's operate at 5.0V (VDD).

The LDO voltage regulator requires an external bypass capacitor for stability. One of three pins, denoted as VCAP, can be configured for the external bypass capacitor. It is recommended that the capacitor be a ceramic cap between 0.1 to 1.0 µF. The VCAP pin is not intended to supply power to external loads. An external voltage regulator should be used if this functionality is required. In addition, external devices should not supply power to the VCAP pin.

On power-up, the external capacitor will look like a large load on the LDO voltage regulator. To prevent erroneous operation, the device is held in Reset while a constant current source charges the external capacitor. After the cap is fully charged, the device is released from Reset. For more information, refer to **Section 23.0 "Electrical Specifications"**.

See Configuration Word 2 register (Register 8-2) for VCAP enable bits.

## 6.2.1 ANSELA REGISTER

The ANSELA register (Register 6-4) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELA bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSELA bits has no affect on digital output functions. A pin with TRIS clear and ANSEL set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

**REGISTER 6-4:      ANSELA: PORTA ANALOG SELECT REGISTER**

| U-0 | U-0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|-----|-----|-------|-------|-------|-------|-------|-------|
| — | — | ANSA5 | ANSA4 | ANSA3 | ANSA2 | ANSA1 | ANSA0 |
| bit 7 | | | | | | | bit 0 |

| Legend: | | |
|---------|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared          x = Bit is unknown |

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **ANSA<5:0>**: Analog Select between Analog or Digital Function on pins RA<5:0>, respectively
0 = Digital I/O. Pin is assigned to port or digital special function.
1 = Analog input. Pin is assigned as analog input[1]. Digital input buffer disabled.

**Note 1:** When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

# PIC16(L)F722A/723A

TABLE 6-1: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Register on Page |
|------|-------|-------|-------|-------|-------|-------|-------|-------|------------------|
| ADCON0 | — | — | CHS3 | CHS2 | CHS1 | CHS0 | GO/DONE | ADON | 85 |
| ADCON1 | — | ADCS2 | ADCS1 | ADCS0 | — | — | ADREF1 | ADREF0 | 86 |
| ANSELA | — | — | ANSA5 | ANSA4 | ANSA3 | ANSA2 | ANSA1 | ANSA0 | 44 |
| APFCON | — | — | — | — | — | — | SSSEL | CCP2SEL | 42 |
| CPSCON0 | CPSON | — | — | — | CPSRNG1 | CPSRNG0 | CPSOUT | T0XCS | 112 |
| CPSCON1 | — | — | — | — | — | CPSCH2 | CPSCH1 | CPSCH0 | 113 |
| OPTION_REG | RBPU | INTEDG | T0CS | T0SE | PSA | PS2 | PS1 | PS0 | 19 |
| PORTA | RA7 | RA6 | RA5 | RA4 | RA3 | RA2 | RA1 | RA0 | 43 |
| SSPCON | WCOL | SSPOV | SSPEN | CKP | SSPM3 | SSPM2 | SSPM1 | SSPM0 | 152 |
| TRISA | TRISA7 | TRISA6 | TRISA5 | TRISA4 | TRISA3 | TRISA2 | TRISA1 | TRISA0 | 43 |

**Legend:** $x$ = unknown, $u$ = unchanged, — = unimplemented locations read as '0'. Shaded cells are not used by PORTA.
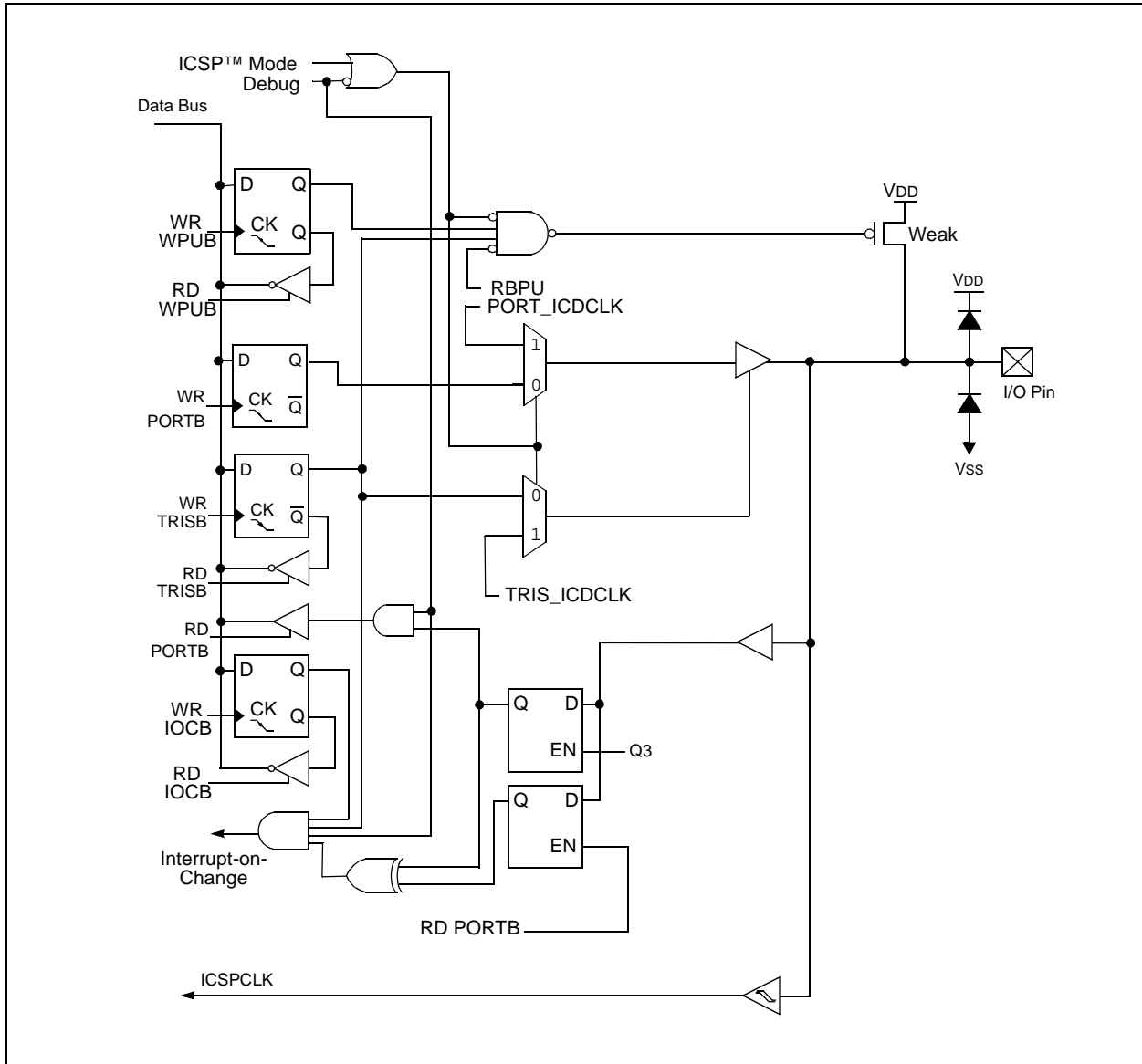
TABLE 6-2: SUMMARY OF CONFIGURATION WORD WITH CLOCK SOURCES

| Name | Bits | Bit -/7 | Bit -/6 | Bit 13/5 | Bit 12/4 | Bit 11/3 | Bit 10/2 | Bit 9/1 | Bit 8/0 | Register on Page |
|------|------|---------|---------|----------|----------|----------|----------|---------|---------|------------------|
| CONFIG2[1] | 13:8 | — | — | — | — | — | — | — | — | 78 |
| | 7:0 | — | — | VCAPEN1 | VCAPEN0 | WDTE | — | — | — | |

**Legend:** — = unimplemented location, read as '0'. Shaded cells are not used by clock sources.
**Note 1:** PIC16F722A/723A only.

**FIGURE 6-11:** **BLOCK DIAGRAM OF RB6**

## 6.5    PORTE and TRISE Registers

PORTE[1] is an 1-bit wide, input-only port. RE3 is input-only and its TRIS bit will always read as '1'.

Reading the PORTE register (Register 6-12) reads the status of the pins. RE3 reads '0' when MCLRE = 1.

### REGISTER 6-12:    PORTE: PORTE REGISTER

| U-0 | U-0 | U-0 | U-0 | R-x | U-0 | U-0 | U-0 |
|-----|-----|-----|-----|-----|-----|-----|-----|
| — | — | — | — | RE3 | — | — | — |
| bit 7 | | | | | | | bit 0 |

| Legend: | | |
|---------|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared          x = Bit is unknown |

bit 7-4      **Unimplemented**: Read as '0'

bit 3         **RE3**: PORTE I/O Pin bits[1]
$1$ = Port pin is > V$_{IH}$
$0$ = Port pin is < V$_{IL}$

bit 2-0      **Unimplemented**: Read as '0'

### REGISTER 6-13:    TRISE: PORTE TRI-STATE REGISTER

| U-0 | U-0 | U-0 | U-0 | R-1 | U-0 | U-0 | U-0 |
|-----|-----|-----|-----|-----|-----|-----|-----|
| — | — | — | — | TRISE3 | — | — | — |
| bit 7 | | | | | | | bit 0 |

| Legend: | | |
|---------|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared          x = Bit is unknown |

bit 7-4      **Unimplemented**: Read as '0'

bit 3         **TRISE3:** RE3 Port Tri-state Control bit
This bit is always '1' as RE3 is an input-only

bit 2-0      **Unimplemented**: Read as '0'

### TABLE 6-5:      SUMMARY OF REGISTERS ASSOCIATED WITH PORTE

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Register on Page |
|------|-------|-------|-------|-------|-------|-------|-------|-------|------------------|
| PORTE | — | — | — | — | RE3 | — | — | — | 69 |
| TRISE | — | — | — | — | TRISE3[1] | — | — | — | 69 |

**Legend:**    x = unknown, u = unchanged, – = unimplemented locations read as '0'. Shaded cells are not used by PORTE

**Note 1:**   This bit is always '1' as RE3 is input-only.

## 7.0 OSCILLATOR MODULE

### 7.1 Overview

The oscillator module has a wide variety of clock sources and selection features that allow it to be used in a wide range of applications while maximizing performance and minimizing power consumption. Figure 7-1 illustrates a block diagram of the oscillator module.

Clock sources can be configured from external oscillators, quartz crystal resonators, ceramic resonators and Resistor-Capacitor (RC) circuits. In addition, the system can be configured to use an internal calibrated high-frequency oscillator as clock source, with a choice of selectable speeds via software.

Clock source modes are configured by the FOSC bits in Configuration Word 1 (CONFIG1). The oscillator module can be configured for one of eight modes of operation.

1. RC – External Resistor-Capacitor (RC) with FOSC/4 output on OSC2/CLKOUT.
2. RCIO – External Resistor-Capacitor (RC) with I/O on OSC2/CLKOUT.
3. INTOSC – Internal oscillator with FOSC/4 output on OSC2 and I/O on OSC1/CLKIN.
4. INTOSCIO – Internal oscillator with I/O on OSC1/CLKIN and OSC2/CLKOUT.
5. EC – External clock with I/O on OSC2/CLKOUT.
6. HS – High Gain Crystal or Ceramic Resonator mode.
7. XT – Medium Gain Crystal or Ceramic Resonator Oscillator mode.
8. LP – Low-Power Crystal mode.

**FIGURE 7-1:** SIMPLIFIED PIC® MCU CLOCK SOURCE BLOCK DIAGRAM
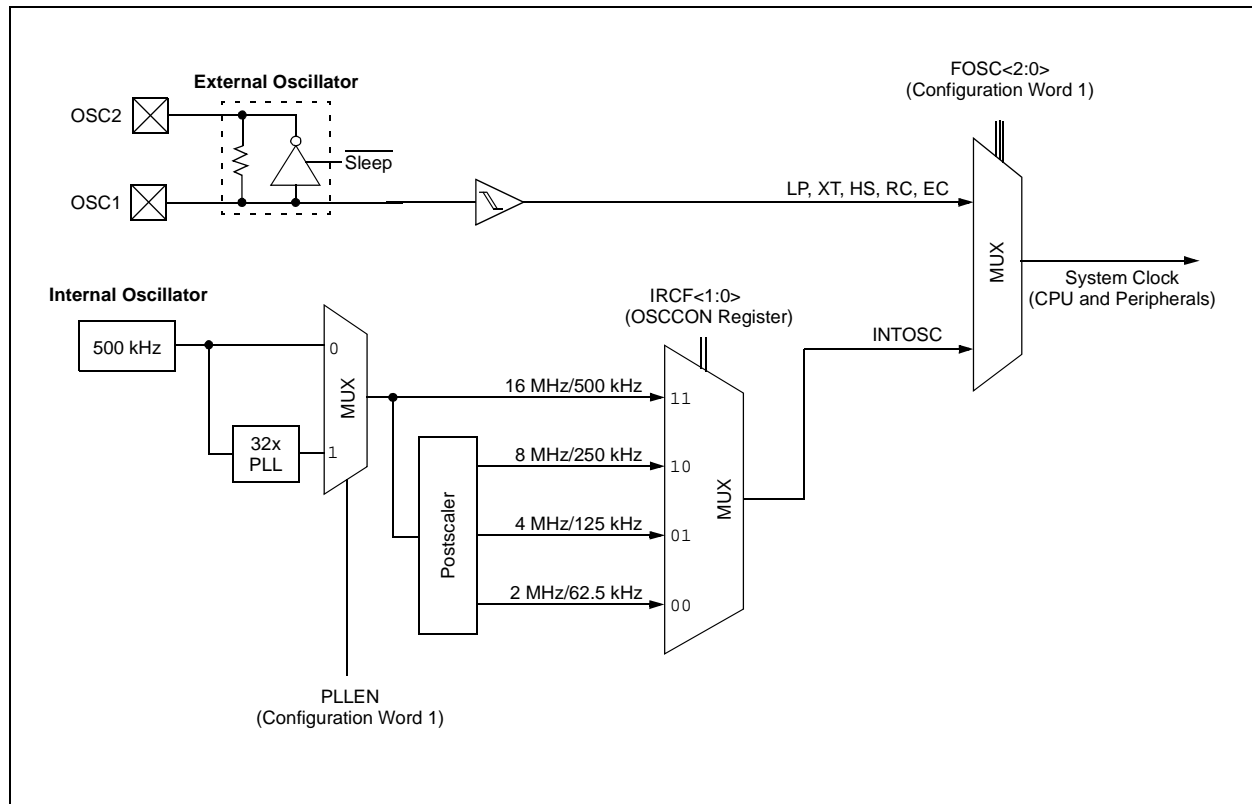
## 7.6 External Clock Modes
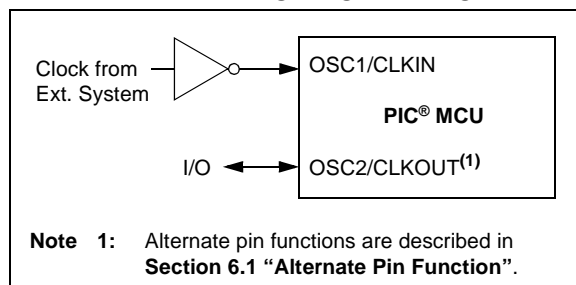
### 7.6.1 OSCILLATOR START-UP TIMER (OST)

If the oscillator module is configured for LP, XT or HS modes, the Oscillator Start-up Timer (OST) counts 1024 oscillations on the OSC1 pin before the device is released from Reset. This occurs following a Power-on Reset (POR) and when the Power-up Timer (PWRT) has expired (if configured), or a wake-up from Sleep. During this time, the program counter does not increment and program execution is suspended. The OST ensures that the oscillator circuit, using a quartz crystal resonator or ceramic resonator, has started and is providing a stable system clock to the oscillator module.

### 7.6.2 EC MODE

The External Clock (EC) mode allows an externally generated logic level as the system clock source. When operating in this mode, an external clock source is connected to the OSC1 input and the OSC2 is available for general purpose I/O. Figure 7-2 shows the pin connections for EC mode.

The Oscillator Start-up Timer (OST) is disabled when EC mode is selected. Therefore, there is no delay in operation after a Power-on Reset (POR) or wake-up from Sleep. Because the PIC® MCU design is fully static, stopping the external clock input will have the effect of halting the device while leaving all data intact. Upon restarting the external clock, the device will resume operation as if no time had elapsed.

**FIGURE 7-2:** **EXTERNAL CLOCK (EC) MODE OPERATION**



**Note 1:** Alternate pin functions are described in **Section 6.1 "Alternate Pin Function"**.

### 7.6.3 LP, XT, HS MODES

The LP, XT and HS modes support the use of quartz crystal resonators or ceramic resonators connected to OSC1 and OSC2 (Figure 7-3). The mode selects a low, medium or high gain setting of the internal inverter-amplifier to support various resonator types and speed.
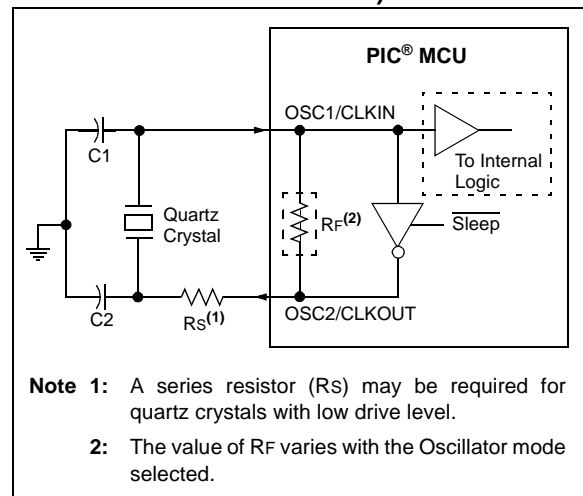
**LP** Oscillator mode selects the lowest gain setting of the internal inverter-amplifier. LP mode current consumption is the least of the three modes. This mode is best suited to drive resonators with a low drive level specification, for example, tuning fork type crystals.

**XT** Oscillator mode selects the intermediate gain setting of the internal inverter-amplifier. XT mode current consumption is the medium of the three modes. This mode is best suited to drive resonators with a medium drive level specification.

**HS** Oscillator mode selects the highest gain setting of the internal inverter-amplifier. HS mode current consumption is the highest of the three modes. This mode is best suited for resonators that require a high drive setting.

Figure 7-3 and Figure 7-4 show typical circuits for quartz crystal and ceramic resonators, respectively.

**FIGURE 7-3:** **QUARTZ CRYSTAL OPERATION (LP, XT OR HS MODE)**



**Note 1:** A series resistor (RS) may be required for quartz crystals with low drive level.

   **2:** The value of RF varies with the Oscillator mode selected.

**Note 1:** Quartz crystal characteristics vary according to type, package and manufacturer. The user should consult the manufacturer data sheets for specifications and recommended application.

   **2:** Always verify oscillator performance over the VDD and temperature range that is expected for the application.

   **3:** For oscillator design assistance, reference the following Microchip Applications Notes:

   • *AN826, Crystal Oscillator Basics and Crystal Selection for rfPIC® and PIC® Devices* (DS00826)

   • *AN849, Basic PIC® Oscillator Design* (DS00849)

   • *AN943, Practical PIC® Oscillator Analysis and Design* (DS00943)

   • *AN949, Making Your Oscillator Work* (DS00949)

## 8.2    Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out using ICSP™ for verification purposes.

> **Note:** The entire Flash program memory will be erased when the code protection is turned off. See the *"PIC16(L)F72X Memory Programming Specification"* (DS41332) for more information.

## 8.3    User ID

Four memory locations (2000h-2003h) are designated as ID locations where the user can store checksum or other code identification numbers. These locations are not accessible during normal execution, but are readable and writable during Program/Verify mode. Only the Least Significant 7 bits of the ID locations are reported when using MPLAB IDE. See the *"PIC16(L)F72X Memory Programming Specification"* (DS41332) for more information.

### 9.1.5  INTERRUPTS

The ADC module allows for the ability to generate an interrupt upon completion of an Analog-to-Digital conversion. The ADC interrupt flag is the ADIF bit in the PIR1 register. The ADC interrupt enable is the ADIE bit in the PIE1 register. The ADIF bit must be cleared in software.

> **Note 1:** The ADIF bit is set at the completion of every conversion, regardless of whether or not the ADC interrupt is enabled.
>
> **2:** The ADC operates during Sleep only when the F$_{RC}$ oscillator is selected.

This interrupt can be generated while the device is operating or while in Sleep. If the device is in Sleep, the interrupt will wake-up the device. Upon waking from Sleep, the next instruction following the SLEEP instruction is always executed. If the user is attempting to wake-up from Sleep and resume in-line code execution, the GIE and PEIE bits of the INTCON register must be disabled. If the GIE and PEIE bits of the INTCON register are enabled, execution will switch to the Interrupt Service Routine.

Please refer to **Section 9.1.5 "Interrupts"** for more information.

## 9.2  ADC Operation

### 9.2.1  STARTING A CONVERSION

To enable the ADC module, the ADON bit of the ADCON0 register must be set to a '1'. Setting the GO/DONE bit of the ADCON0 register to a '1' will start the Analog-to-Digital conversion.

> **Note:** The GO/DONE bit should not be set in the same instruction that turns on the ADC. Refer to **Section 9.2.6 "A/D Conversion Procedure"**.

### 9.2.2  COMPLETION OF A CONVERSION

When the conversion is complete, the ADC module will:

• Clear the GO/DONE bit
• Set the ADIF Interrupt Flag bit
• Update the ADRES register with new conversion result

### 9.2.3  TERMINATING A CONVERSION

If a conversion must be terminated before completion, the GO/DONE bit can be cleared in software. The ADRES register will be updated with the partially complete Analog-to-Digital conversion sample. Incomplete bits will match the last bit converted.

> **Note:** A device Reset forces all registers to their Reset state. Thus, the ADC module is turned off and any pending conversion is terminated.

### 9.2.4  ADC OPERATION DURING SLEEP

The ADC module can operate during Sleep. This requires the ADC clock source to be set to the F$_{RC}$ option. When the F$_{RC}$ clock source is selected, the ADC waits one additional instruction before starting the conversion. This allows the SLEEP instruction to be executed, which can reduce system noise during the conversion. If the ADC interrupt is enabled, the device will wake-up from Sleep when the conversion completes. If the ADC interrupt is disabled, the ADC module is turned off after the conversion completes, although the ADON bit remains set.

When the ADC clock source is something other than F$_{RC}$, a SLEEP instruction causes the present conversion to be aborted and the ADC module is turned off, although the ADON bit remains set.

### 9.2.5  SPECIAL EVENT TRIGGER

The Special Event Trigger of the CCP module allows periodic ADC measurements without software intervention. When this trigger occurs, the GO/DONE bit is set by hardware and the Timer1 counter resets to zero.

Using the Special Event Trigger does not assure proper ADC timing. It is the user's responsibility to ensure that the ADC timing requirements are met.

Refer to **Section 15.0 "Capture/Compare/PWM (CCP) Module"** for more information.

# PIC16(L)F722A/723A

## 13.0 TIMER2 MODULE

The Timer2 module is an 8-bit timer with the following features:

- 8-bit timer register (TMR2)
- 8-bit period register (PR2)
- Interrupt on TMR2 match with PR2
- Software programmable prescaler (1:1, 1:4, 1:16)
- Software programmable postscaler (1:1 to 1:16)

See Figure 13-1 for a block diagram of Timer2.

### 13.1 Timer2 Operation

The clock input to the Timer2 module is the system instruction clock (F$_{OSC}$/4). The clock is fed into the Timer2 prescaler, which has prescale options of 1:1, 1:4 or 1:16. The output of the prescaler is then used to increment the TMR2 register.

The values of TMR2 and PR2 are constantly compared to determine when they match. TMR2 will increment from 00h until it matches the value in PR2. When a match occurs, two things happen:

- TMR2 is reset to 00h on the next increment cycle.
- The Timer2 postscaler is incremented.

The match output of the Timer2/PR2 comparator is then fed into the Timer2 postscaler. The postscaler has postscale options of 1:1 to 1:16 inclusive. The output of the Timer2 postscaler is used to set the TMR2IF interrupt flag bit in the PIR1 register.

The TMR2 and PR2 registers are both fully readable and writable. On any Reset, the TMR2 register is set to 00h and the PR2 register is set to FFh.

Timer2 is turned on by setting the TMR2ON bit in the T2CON register to a '1'. Timer2 is turned off by clearing the TMR2ON bit to a '0'.

The Timer2 prescaler is controlled by the T2CKPS bits in the T2CON register. The Timer2 postscaler is controlled by the TOUTPS bits in the T2CON register. The prescaler and postscaler counters are cleared when:

- A write to TMR2 occurs.
- A write to T2CON occurs.
- Any device Reset occurs (Power-on Reset, $\overline{\text{MCLR}}$ Reset, Watchdog Timer Reset, or Brown-out Reset).

> **Note:** TMR2 is not cleared when T2CON is written.

**FIGURE 13-1: TIMER2 BLOCK DIAGRAM**
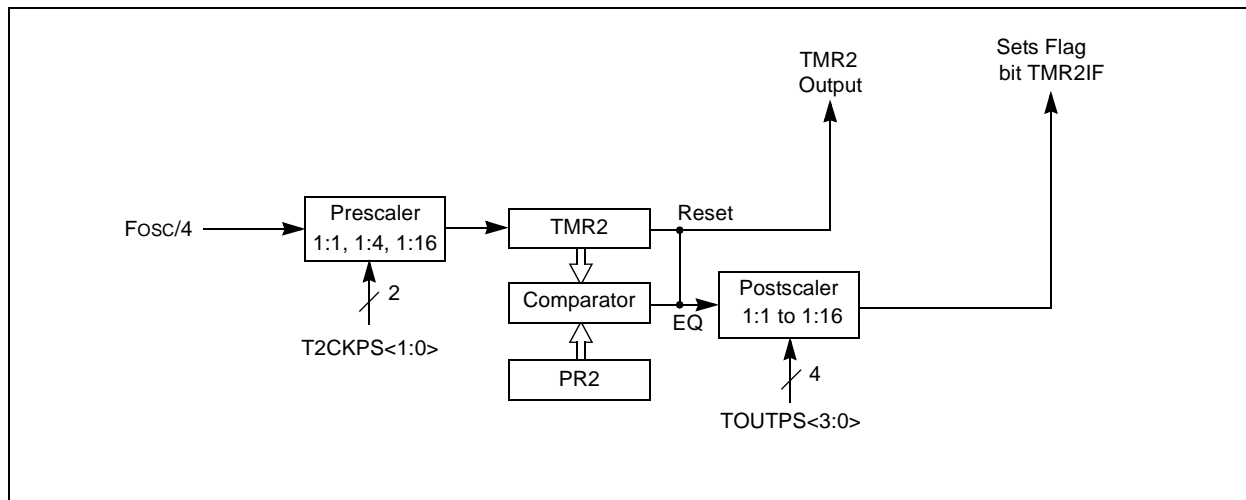
### 17.1.1    MASTER MODE

In Master mode, data transfer can be initiated at any time because the master controls the SCK line. Master mode determines when the slave (Figure 17-1, Processor 2) transmits data via control of the SCK line.

#### 17.1.1.1    Master Mode Operation

The SSP consists of a transmit/receive shift register (SSPSR) and a buffer register (SSPBUF). The SSPSR register shifts the data in and out of the device, MSb first. The SSPBUF register holds the data that is written out of the master until the received data is ready. Once the eight bits of data have been received, the byte is moved to the SSPBUF register. The Buffer Full Status bit, BF of the SSPSTAT register, and the SSP Interrupt Flag bit, SSPIF of the PIR1 register, are then set.

Any write to the SSPBUF register during transmission/reception of data will be ignored and the Write Collision Detect bit, WCOL of the SSPCON register, will be set. User software must clear the WCOL bit so that it can be determined if the following write(s) to the SSPBUF register completed successfully.

When the application software is expecting to receive valid data, the SSPBUF should be read before the next byte of data is written to the SSPBUF. The BF bit of the SSPSTAT register is set when SSPBUF has been loaded with the received data (transmission is complete). When the SSPBUF is read, the BF bit is cleared. This data may be irrelevant if the SPI is only a transmitter. The SSP interrupt may be used to determine when the transmission/reception is complete and the SSPBUF must be read and/or written. If interrupts are not used, then software polling can be done to ensure that a write collision does not occur. Example 17-1 shows the loading of the SSPBUF (SSPSR) for data transmission.

> **Note:** The SSPSR is not directly readable or writable and can only be accessed by addressing the SSPBUF register.

#### 17.1.1.2    Enabling Master I/O

To enable the serial port, the SSPEN bit of the SSPCON register, must be set. To reset or reconfigure SPI mode, clear the SSPEN bit, re-initialize the SSPCON register and then set the SSPEN bit. If a Master mode of operation is selected in the SSPM bits of the SSPCON register, the SDI, SDO and SCK pins will be assigned as serial port pins.

For these pins to function as serial port pins, they must have their corresponding data direction bits set or cleared in the associated TRIS register as follows:

- SDI configured as input
- SDO configured as output
- SCK configured as output

#### 17.1.1.3    Master Mode Setup

In Master mode, the data is transmitted/received as soon as the SSPBUF register is loaded with a byte value. If the master is only going to receive, SDO output could be disabled (programmed and used as an input). The SSPSR register will continue to shift in the signal present on the SDI pin at the programmed clock rate.

When initializing SPI Master mode operation, several options need to be specified. This is accomplished by programming the appropriate control bits in the SSPCON and SSPSTAT registers. These control bits allow the following to be specified:

- SCK as clock output
- Idle state of SCK (CKP bit)
- Data input sample phase (SMP bit)
- Output data on rising/falling edge of SCK (CKE bit)
- Clock bit rate

In Master mode, the SPI clock rate (bit rate) is user selectable to be one of the following:

- $F_{OSC}/4$ (or TCY)
- $F_{OSC}/16$ (or 4 • TCY)
- $F_{OSC}/64$ (or 16 • TCY)
- (Timer2 output)/2

This allows a maximum data rate of 5 Mbps (at $F_{OSC}$ = 20 MHz).

Figure 17-3 shows the waveforms for Master mode. The clock polarity is selected by appropriately programming the CKP bit of the SSPCON register. When the CKE bit is set, the SDO data is valid before there is a clock edge on SCK. The sample time of the input data is shown based on the state of the SMP bit and can occur at the middle or end of the data output time. The time when the SSPBUF is loaded with the received data is shown.

#### 17.1.1.4    Sleep in Master Mode

In Master mode, all module clocks are halted and the transmission/reception will remain in their current state, paused, until the device wakes from Sleep. After the device wakes up from Sleep, the module will continue to transmit/receive data.

## 17.2.4    ADDRESSING

Once the SSP module has been enabled, it waits for a Start condition to occur. Following the Start condition, the eight bits are shifted into the SSPSR register. All incoming bits are sampled with the rising edge of the clock line (SCL).

### 17.2.4.1    7-bit Addressing

In 7-bit Addressing mode (Figure 17-10), the value of register SSPSR<7:1> is compared to the value of register SSPADD<7:1>. The address is compared on the falling edge of the eighth clock (SCL) pulse. If the addresses match, and the BF and SSPOV bits are clear, the following events occur:

- The SSPSR register value is loaded into the SSPBUF register.
- The BF bit is set.
- An $\overline{ACK}$ pulse is generated.
- SSP interrupt flag bit, SSPIF of the PIR1 register, is set (interrupt is generated if enabled) on the falling edge of the ninth SCL pulse.

### 17.2.4.2    10-bit Addressing

In 10-bit Address mode, two address bytes need to be received by the slave (Figure 17-11). The five Most Significant bits (MSbs) of the first address byte specify if it is a 10-bit address. The R/$\overline{W}$ bit of the SSPSTAT register must specify a write so the slave device will receive the second address byte. For a 10-bit address, the first byte would equal '`1111 0 A9 A8 0`', where A9 and A8 are the two MSbs of the address.

The sequence of events for 10-bit address is as follows for reception:

1. Load SSPADD register with high byte of address.
2. Receive first (high) byte of address (bits SSPIF, BF and UA of the SSPSTAT register are set).
3. Read the SSPBUF register (clears bit BF).
4. Clear the SSPIF flag bit.
5. Update the SSPADD register with second (low) byte of address (clears UA bit and releases the SCL line).
6. Receive low byte of address (bits SSPIF, BF and UA are set).
7. Update the SSPADD register with the high byte of address. If match releases SCL line, this will clear bit UA.
8. Read the SSPBUF register (clears bit BF).
9. Clear flag bit SSPIF.

If data is requested by the master, once the slave has been addressed:

1. Receive repeated Start condition.
2. Receive repeat of high byte address with R/$\overline{W}$ = 1, indicating a read.
3. BF bit is set and the CKP bit is cleared, stopping SCL and indicating a read request.
4. SSPBUF is written, setting BF, with the data to send to the master device.
5. CKP is set in software, releasing the SCL line.

### 17.2.4.3    Address Masking

The Address Masking register (SSPMSK) is only accessible while the SSPM bits of the SSPCON register are set to '`1001`'. In this register, the user can select which bits of a received address the hardware will compare when determining an address match. Any bit that is set to a zero in the SSPMSK register, the corresponding bit in the received address byte and SSPADD register are ignored when determining an address match. By default, the register is set to all ones, requiring a complete match of a 7-bit address or the lower eight bits of a 10-bit address.

## 18.0 PROGRAM MEMORY READ

The Flash program memory is readable during normal operation over the full V$_{DD}$ range of the device. To read data from program memory, five Special Function Registers (SFRs) are used:

- PMCON1
- PMDATL
- PMDATH
- PMADRL
- PMADRH

The value written to the PMADRH:PMADRL register pair determines which program memory location is read. The read operation will be initiated by setting the RD bit of the PMCON1 register. The program memory Flash controller takes two instructions to complete the read. As a consequence, after the RD bit has been set, the next two instructions will be ignored. To avoid conflict with program execution, it is recommended that the two instructions following the setting of the RD bit are NOP. When the read completes, the result is placed in the PMDATLH:PMDATL register pair. Refer to Example 18-1 for sample code.

> **Note:** Code-protect does not effect the CPU from performing a read operation on the program memory. For more information, refer to **Section 8.2 "Code Protection"**

### EXAMPLE 18-1: PROGRAM MEMORY READ

```
        BANKSEL PMADRL  ;
        MOVF    MS_PROG_ADDR, W;
        MOVWF   PMADRH  ;MS Byte of Program Address to read
        MOVF    LS_PROG_ADDR, W;
        MOVWF   PMADRL  ;LS Byte of Program Address to read
        BANKSEL PMCON1  ;
        BSF     PMCON1, RD;Initiate Read
        NOP
        NOP             ;Any instructions here are ignored as program
                        ;memory is read in second cycle after BSF
        BANKSEL PMDATL  ;
        MOVF    PMDATL, W;W = LS Byte of Program Memory Read
        MOVWF   LOWPMBYTE;
        MOVF    PMDATH, W;W = MS Byte of Program Memory Read
        MOVWF   HIGHPMBYTE;
```

Required Sequence

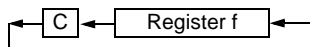# PIC16(L)F722A/723A

<div style="display: flex;">
<div>

**RLF**      **Rotate Left f through Carry**

| | |
|---|---|
| Syntax: | [ *label* ]    RLF    f,d |
| Operands: | $0 \leq f \leq 127$<br>$d \in [0,1]$ |
| Operation: | See description below |
| Status Affected: | C |
| Description: | The contents of register 'f' are rotated one bit to the left through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is stored back in register 'f'. |



| | |
|---|---|
| Words: | 1 |
| Cycles: | 1 |
| <u>Example:</u> | RLF     REG1,0 |

Before Instruction
```
REG1   =   1110 0110
C      =   0
```
After Instruction
```
REG1   =   1110 0110
W      =   1100 1100
C      =   1
```

**RRF**      **Rotate Right f through Carry**

| | |
|---|---|
| Syntax: | [ *label* ]    RRF    f,d |
| Operands: | $0 \leq f \leq 127$<br>$d \in [0,1]$ |
| Operation: | See description below |
| Status Affected: | C |
| Description: | The contents of register 'f' are rotated one bit to the right through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'. |



</div>
<div>

**SLEEP**      **Enter Sleep mode**

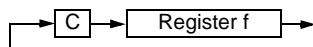| | |
|---|---|
| Syntax: | [ *label* ]   SLEEP |
| Operands: | None |
| Operation: | 00h $\rightarrow$ WDT,<br>0 $\rightarrow$ WDT prescaler,<br>1 $\rightarrow$ $\overline{TO}$,<br>0 $\rightarrow$ $\overline{PD}$ |
| Status Affected: | $\overline{TO}$, $\overline{PD}$ |
| Description: | The power-down Status bit, $\overline{PD}$ is cleared. Time-out Status bit, $\overline{TO}$ is set. Watchdog Timer and its prescaler are cleared.<br>The processor is put into Sleep mode with the oscillator stopped. |

**SUBLW**      **Subtract W from literal**

| | |
|---|---|
| Syntax: | [ *label* ]   SUBLW   k |
| Operands: | $0 \leq k \leq 255$ |
| Operation: | k - (W) $\rightarrow$ (W) |
| Status Affected: | C, DC, Z |
| Description: | The W register is subtracted (2's complement method) from the 8-bit literal 'k'. The result is placed in the W register. |

| | |
|---|---|
| C = 0 | W > k |
| C = 1 | W $\leq$ k |
| DC = 0 | W<3:0> > k<3:0> |
| DC = 1 | W<3:0> $\leq$ k<3:0> |

</div>
</div>

## 23.0   ELECTRICAL SPECIFICATIONS

**Absolute Maximum Ratings[†]**

Ambient temperature under bias ......................................................................................................... -40°C to +125°C

Storage temperature ....................................................................................................... -65°C to +150°C

Voltage on $V_{DD}$ with respect to $V_{SS}$, PIC16F722A/723A ................................................................... -0.3V to +6.5V

Voltage on $V_{CAP}$ pin with respect to $V_{SS}$, PIC16F722A/723A ........................................................... -0.3V to +4.0V

Voltage on $V_{DD}$ with respect to $V_{SS}$, PIC16LF722A/723A ............................................................... -0.3V to +4.0V

Voltage on $\overline{MCLR}$ with respect to Vss ................................................................................................ -0.3V to +9.0V

Voltage on all other pins with respect to $V_{SS}$ ......................................................................... -0.3V to ($V_{DD}$ + 0.3V)

Total power dissipation[1] ................................................................................................................ 800 mW

Maximum current out of $V_{SS}$ pin ........................................................................................................ 95 mA

Maximum current into $V_{DD}$ pin ......................................................................................................... 70 mA

Clamp current, $I_K$ ($V_{PIN} < 0$ or $V_{PIN} > V_{DD}$) .................................................................................. ± 20 mA

Maximum output current sunk by any I/O pin ..................................................................................... 25 mA

Maximum output current sourced by any I/O pin ................................................................................ 25 mA

Maximum current sunk by all ports[2], -40°C $\leq$ $T_A$ $\leq$ +85°C for industrial ....................................................... 200 mA

Maximum current sunk by all ports[2], -40°C $\leq$ $T_A$ $\leq$ +125°C for extended ....................................................... 90 mA

Maximum current sourced by all ports[2], 40°C $\leq$ $T_A$ $\leq$ +85°C for industrial .................................................. 140 mA

Maximum current sourced by all ports[2], -40°C $\leq$ $T_A$ $\leq$ +125°C for extended .................................................. 65 mA

**Note 1:**   Power dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum(V_{OI} \times I_{OL})$.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

## TABLE 23-2: OSCILLATOR PARAMETERS

| Param No. | Sym. | Characteristic | Freq. Tolerance | Min. | Typ† | Max. | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| OS08 | HFOSC | Internal Calibrated HFINTOSC Frequency[2] | ±2% | — | 16.0 | — | MHz | 0°C ≤ TA ≤ +85°C, VDD ≥ 2.5V |
| | | | ±5% | — | 16.0 | — | MHz | -40°C ≤ TA ≤ +125°C |
| OS08A | MFOSC | Internal Calibrated MFINTOSC Frequency[2] | ±2% | — | 500 | — | kHz | 0°C ≤ TA ≤ +85°C VDD ≥ 2.5V |
| | | | ±5% | — | 500 | 10 | kHz | -40°C ≤ TA ≤ +125°C |
| OS10* | TIOSC ST | HFINTOSC Wake-up from Sleep Start-up Time | — | — | 5 | 8 | µs | |
| | | MFINTOSC Wake-up from Sleep Start-up Time | — | — | 20 | 30 | µs | |

\*      These parameters are characterized but not tested.

†      Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min" values with an external clock applied to the OSC1 pin. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

**2:** To ensure these oscillator frequency tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 µF and 0.01 µF values in parallel are recommended.

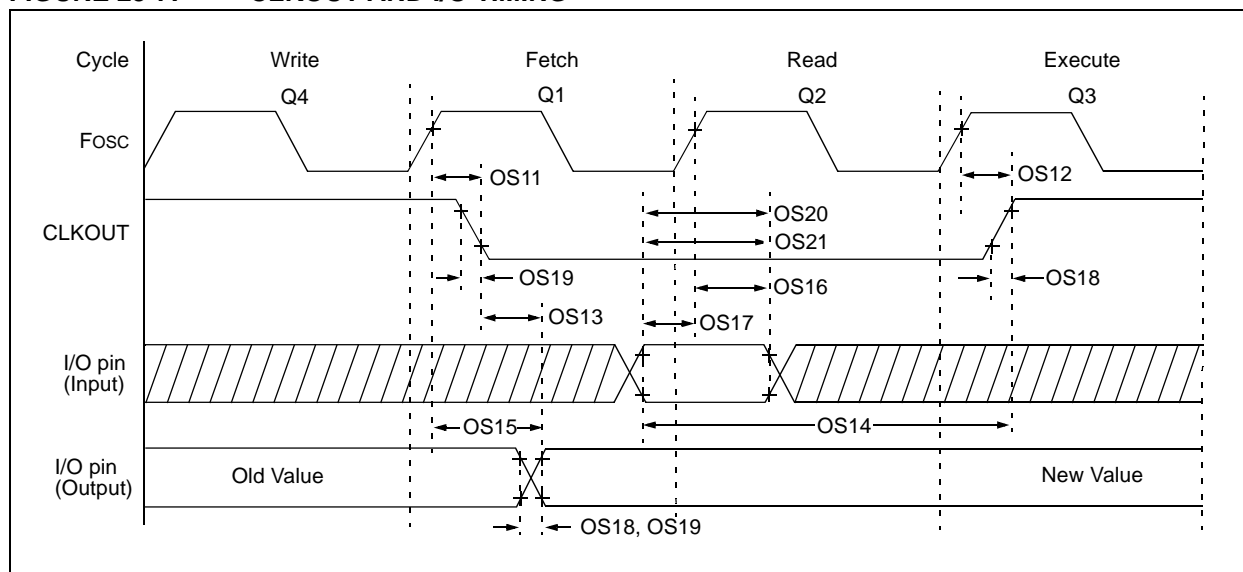**3:** By design.

## FIGURE 23-7: CLKOUT AND I/O TIMING

**TABLE 23-14: CAP SENSE OSCILLATOR SPECIFICATIONS**

| Param. No. | Symbol | Characteristic | | Min. | Typ† | Max. | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| CS01 | I$_{SRC}$ | Current Source | High | — | -5.8 | -6 | μA | -40, -85°C |
| | | | Medium | — | -1.1 | -3.2 | μA | |
| | | | Low | — | -0.2 | -0.9 | μA | |
| CS02 | I$_{SNK}$ | Current Sink | High | — | 6.6 | 6 | μA | -40, -85°C |
| | | | Medium | — | 1.3 | 3.2 | μA | |
| | | | Low | — | 0.24 | 0.9 | μA | |
| CS03 | VC$_{HYST}$ | Cap Hysteresis | High | — | 525 | — | mV | VC$_{TH}$-VC$_{TL}$ |
| | | | Medium | — | 375 | — | mV | |
| | | | Low | — | 280 | — | mV | |

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**FIGURE 23-22: CAP SENSE OSCILLATOR**
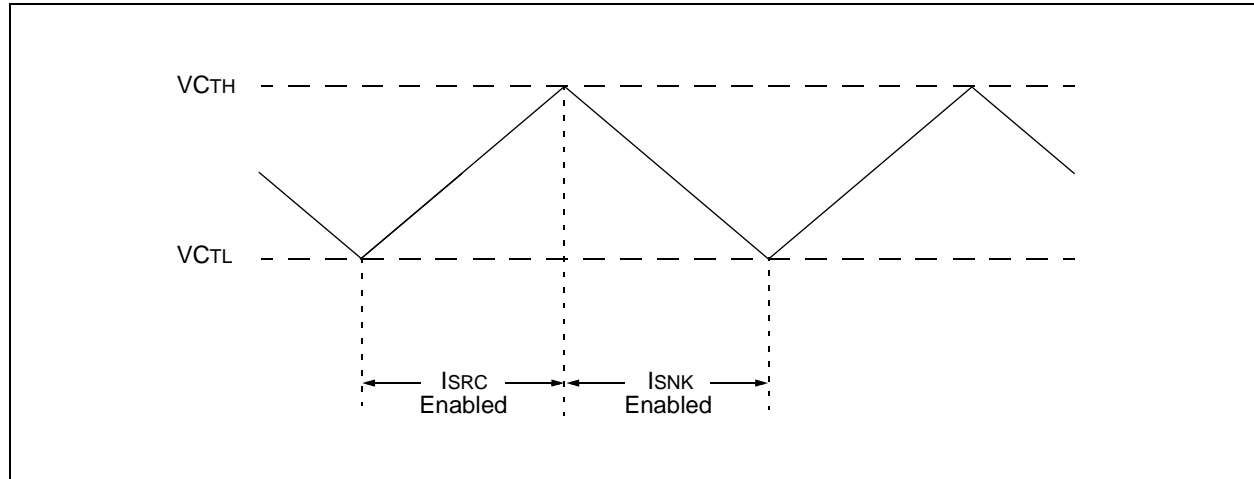
# PIC16(L)F722A/723A

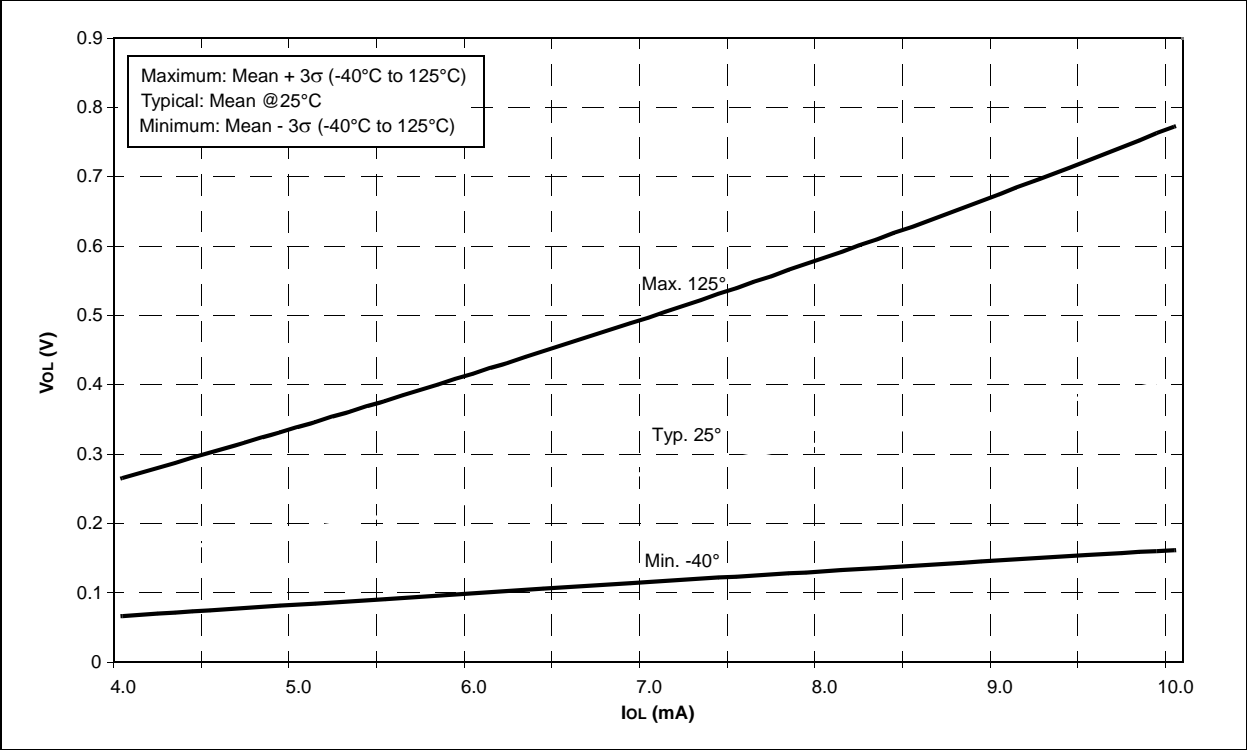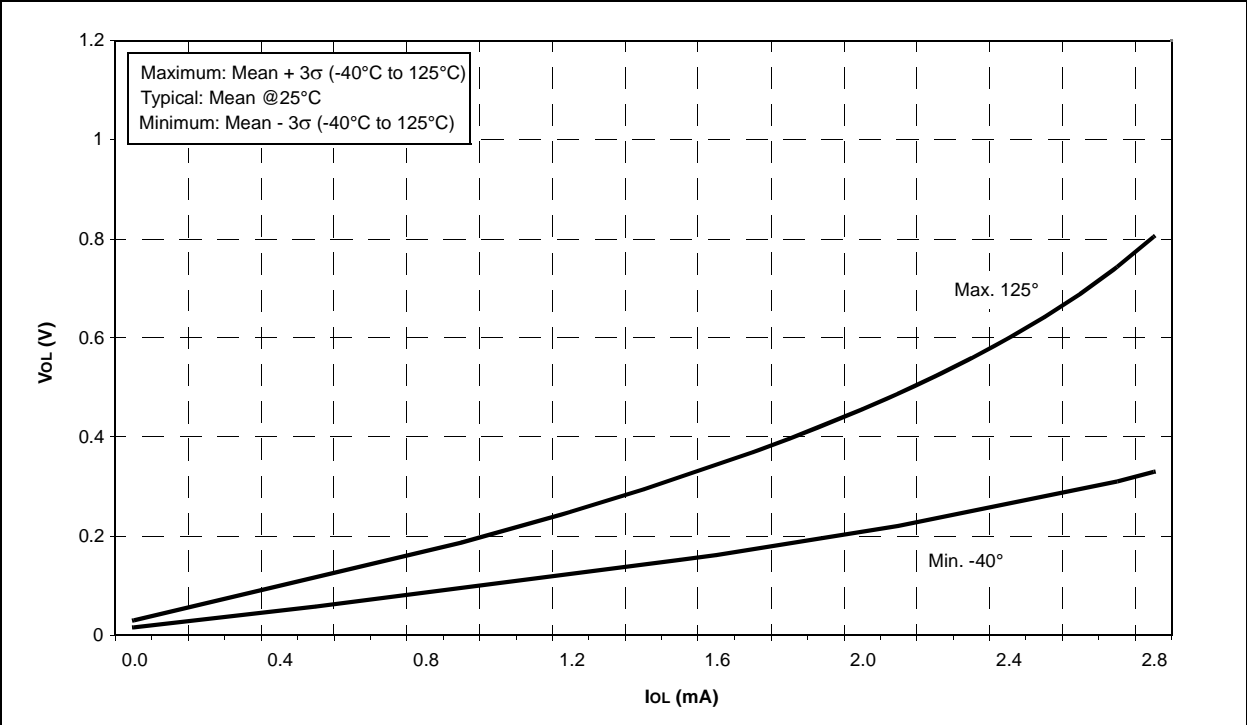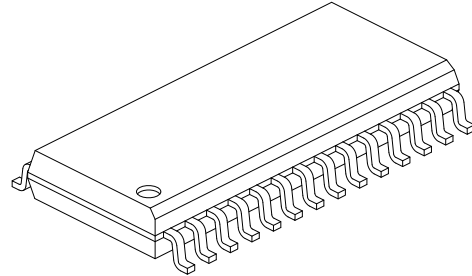**FIGURE 24-56:** V<sub>OL</sub> vs. I<sub>OL</sub> OVER TEMPERATURE, V<sub>DD</sub> = 3.6
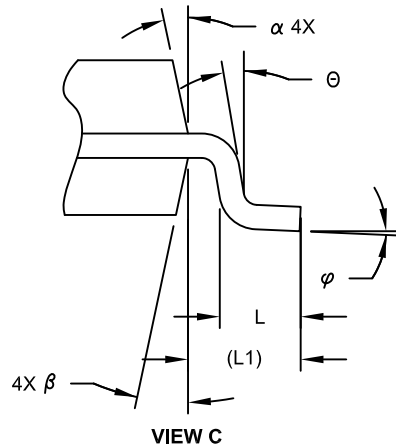


**FIGURE 24-57:** V<sub>OL</sub> vs. I<sub>OL</sub> OVER TEMPERATURE, V<sub>DD</sub> = 1.8V

**28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]**

| | | | | |
|---|---|---|---|---|
| **Note:** | For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging | | | |



**VIEW C**

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 28 | |
| Pitch | e | | 1.27 BSC | |
| Overall Height | A | - | - | 2.65 |
| Molded Package Thickness | A2 | 2.05 | - | - |
| Standoff § | A1 | 0.10 | - | 0.30 |
| Overall Width | E | | 10.30 BSC | |
| Molded Package Width | E1 | | 7.50 BSC | |
| Overall Length | D | | 17.90 BSC | |
| Chamfer (Optional) | h | 0.25 | - | 0.75 |
| Foot Length | L | 0.40 | - | 1.27 |
| Footprint | L1 | | 1.40 REF | |
| Lead Angle | Θ | 0° | - | - |
| Foot Angle | φ | 0° | - | 8° |
| Lead Thickness | c | 0.18 | - | 0.33 |
| Lead Width | b | 0.31 | - | 0.51 |
| Mold Draft Angle Top | α | 5° | - | 15° |
| Mold Draft Angle Bottom | β | 5° | - | 15° |

**Notes:**
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
    BSC: Basic Dimension. Theoretically exact value shown without tolerances.
    REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing C04-052C Sheet 2 of 2