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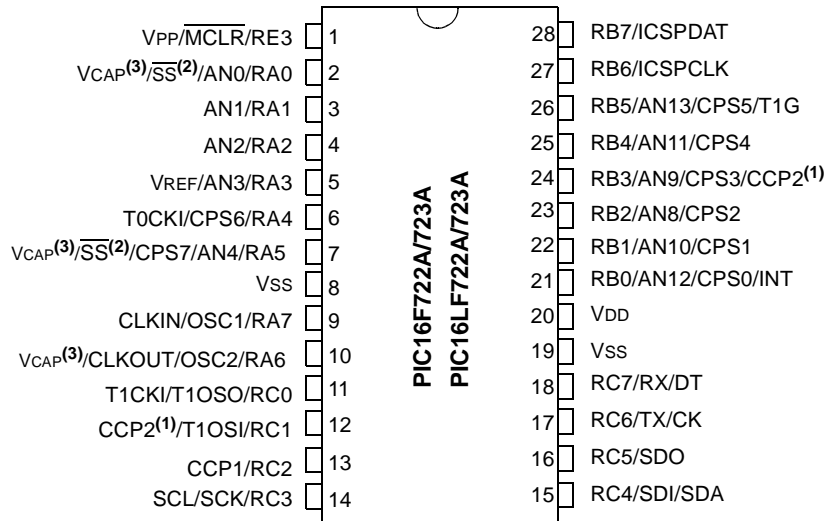
Details

| | |
|----------------------------|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 20MHz |
| Connectivity | I ² C, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 25 |
| Program Memory Size | 3.5KB (2K x 14) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 128 x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V |
| Data Converters | A/D 11x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-SSOP (0.209", 5.30mm Width) |
| Supplier Device Package | 28-SSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic16f722a-i-ss |

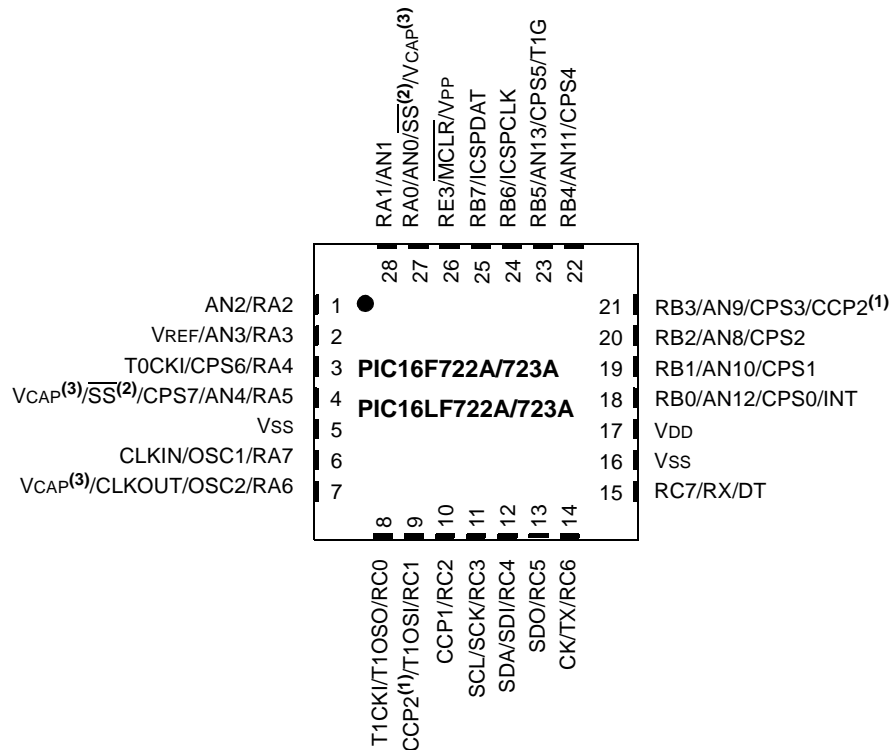
PIC16(L)F722A/723A

Pin Diagrams – 28-PIN SPDIP/SOIC/SSOP/QFN/UQFN (PIC16(L)F722A/723A)

SPDIP, SOIC, SSOP



QFN, UQFN



- Note 1:** CCP2 pin location may be selected as RB3 or RC1.
Note 2: SS pin location may be selected as RA5 or RA0.
Note 3: PIC16F722A/723A devices only.

1.0 DEVICE OVERVIEW

The PIC16(L)F722A/723A devices are covered by this data sheet. They are available in 28-pin packages. Figure 1-1 shows a block diagram of the PIC16(L)F722A/723A devices. Table 1-1 shows the pinout descriptions.

PIC16(L)F722A/723A

TABLE 2-1: PIC16(L)F722A/723A SPECIAL FUNCTION REGISTER SUMMARY

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on: POR, BOR | Page |
|-----------------------|---------|--|---------|---------|--|-----------------|--------------------------------|----------------------|---------|--------------------|--------|
| Bank 0 | | | | | | | | | | | |
| 00h ⁽²⁾ | INDF | Addressing this location uses contents of FSR to address data memory (not a physical register) | | | | | | | | xxxx xxxx | 22,30 |
| 01h | TMR0 | Timer0 Module Register | | | | | | | | xxxx xxxx | 91,30 |
| 02h ⁽²⁾ | PCL | Program Counter (PC) Least Significant Byte | | | | | | | | 0000 0000 | 21,30 |
| 03h ⁽²⁾ | STATUS | IRP | RP1 | RP0 | \overline{TO} | \overline{PD} | Z | DC | C | 0001 1xxx | 18,30 |
| 04h ⁽²⁾ | FSR | Indirect Data Memory Address Pointer | | | | | | | | xxxx xxxx | 22,30 |
| 05h | PORTA | RA7 | RA6 | RA5 | RA4 | RA3 | RA2 | RA1 | RA0 | xxxx xxxx | 43,30 |
| 06h | PORTB | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 | xxxx xxxx | 52,30 |
| 07h | PORTC | RC7 | RC6 | RC5 | RC4 | RC3 | RC2 | RC1 | RC0 | xxxx xxxx | 62,30 |
| 09h | PORTE | — | — | — | — | RE3 | — | — | — | ---- xxxx | 69,30 |
| 0Ah ^(1, 2) | PCLATH | — | — | — | Write Buffer for the upper 5 bits of the Program Counter | | | | | ---0 0000 | 21,30 |
| 0Bh ⁽²⁾ | INTCON | GIE | PEIE | TOIE | INTE | RBIE | TOIF | INTF | RBIF | 0000 000x | 36,30 |
| 0Ch | PIR1 | TMR1GIF | ADIF | RCIF | TXIF | SSPIF | CCP1IF | TMR2IF | TMR1IF | 0000 0000 | 39,30 |
| 0Dh | PIR2 | — | — | — | — | — | — | — | CCP2IF | ---- ---0 | 40,30 |
| 0Eh | TMR1L | Holding Register for the Least Significant Byte of the 16-bit TMR1 Register | | | | | | | | xxxx xxxx | 99,30 |
| 0Fh | TMR1H | Holding Register for the Most Significant Byte of the 16-bit TMR1 Register | | | | | | | | xxxx xxxx | 99,30 |
| 10h | T1CON | TMR1CS1 | TMR1CS0 | T1CKPS1 | T1CKPS0 | T1OSCEN | $\overline{T1SYN\overline{C}}$ | — | TMR1ON | 0000 00-0 | 103,30 |
| 11h | TMR2 | Timer2 Module Register | | | | | | | | 0000 0000 | 106,30 |
| 12h | T2CON | — | TOUTPS3 | TOUTPS2 | TOUTPS1 | TOUTPS0 | TMR2ON | T2CKPS1 | T2CKPS0 | -000 0000 | 107,30 |
| 13h | SSPBUF | Synchronous Serial Port Receive Buffer/Transmit Register | | | | | | | | xxxx xxxx | 147,30 |
| 14h | SSPCON | WCOL | SSPOV | SSPEN | CKP | SSPM3 | SSPM2 | SSPM1 | SSPM0 | 0000 0000 | 164,30 |
| 15h | CCPR1L | Capture/Compare/PWM Register (LSB) | | | | | | | | xxxx xxxx | 116,30 |
| 16h | CCPR1H | Capture/Compare/PWM Register (MSB) | | | | | | | | xxxx xxxx | 116,30 |
| 17h | CCP1CON | — | — | DC1B1 | DC1B0 | CCP1M3 | CCP1M2 | CCP1M1 | CCP1M0 | --00 0000 | 115,30 |
| 18h | RCSTA | SPEN | RX9 | SREN | CREN | ADDEN | FERR | OERR | RX9D | 0000 000x | 134,30 |
| 19h | TXREG | USART Transmit Data Register | | | | | | | | 0000 0000 | 133,30 |
| 1Ah | RCREG | USART Receive Data Register | | | | | | | | 0000 0000 | 131,30 |
| 1Bh | CCPR2L | Capture/Compare/PWM Register 2 (LSB) | | | | | | | | xxxx xxxx | 116,30 |
| 1Ch | CCPR2H | Capture/Compare/PWM Register 2 (MSB) | | | | | | | | xxxx xxxx | 116,30 |
| 1Dh | CCP2CON | — | — | DC2B1 | DC2B0 | CCP2M3 | CCP2M2 | CCP2M1 | CCP2M0 | --00 0000 | 115,30 |
| 1Eh | ADRES | A/D Result Register | | | | | | | | xxxx xxxx | 86,30 |
| 1Fh | ADCON0 | — | — | CHS3 | CHS2 | CHS1 | CHS0 | $\overline{GO/DONE}$ | ADON | --00 0000 | 85,30 |

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved.
Shaded locations are unimplemented, read as '0'.

- Note** 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8>, whose contents are transferred to the upper byte of the program counter.
- 2: These registers can be addressed from any bank.
- 3: Accessible only when SSPM<3:0> = 1001.
- 4: Accessible only when SSPM<3:0> ≠ 1001.
- 5: This bit is always '1' as RE3 is input-only.

5.0 LOW DROPOUT (LDO) VOLTAGE REGULATOR

The PIC16F722A/723A devices differ from the PIC16LF722A/723A devices due to an internal Low Dropout (LDO) voltage regulator. The PIC16F722A/723A devices contain an internal LDO, while the PIC16LF722A/723A ones do not.

The lithography of the die allows a maximum operating voltage of 3.6V on the internal digital logic. In order to continue to support 5.0V designs, a LDO voltage regulator is integrated on the die. The LDO voltage regulator allows for the internal digital logic to operate at 3.2V, while I/O's operate at 5.0V (VDD).

The LDO voltage regulator requires an external bypass capacitor for stability. One of three pins, denoted as VCAP, can be configured for the external bypass capacitor. It is recommended that the capacitor be a ceramic cap between 0.1 to 1.0 μ F. The VCAP pin is not intended to supply power to external loads. An external voltage regulator should be used if this functionality is required. In addition, external devices should not supply power to the VCAP pin.

On power-up, the external capacitor will look like a large load on the LDO voltage regulator. To prevent erroneous operation, the device is held in Reset while a constant current source charges the external capacitor. After the cap is fully charged, the device is released from Reset. For more information, refer to **Section 23.0 "Electrical Specifications"**.

See Configuration Word 2 register (Register 8-2) for VCAP enable bits.

PIC16(L)F722A/723A

6.4 PORTC and TRISC Registers

PORTC is a 8-bit wide, bidirectional port. The corresponding data direction register is TRISC (Register 6-11). Setting a TRISC bit (= 1) will make the corresponding PORTC pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISC bit (= 0) will make the corresponding PORTC pin an output (i.e., enable the output driver and put the contents of the output latch on the selected pin). Example 6-3 shows how to initialize PORTC.

Reading the PORTC register (Register 6-10) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch.

The TRISC register (Register 6-11) controls the PORTC pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISC register are maintained set when using them as analog inputs. I/O pins configured as analog input always read '0'.

EXAMPLE 6-3: INITIALIZING PORTC

```
BANKSEL PORTC      ;
CLRF   PORTC        ;Init PORTC
BANKSEL TRISC       ;
MOVLW   B'00001100' ;Set RC<3:2> as inputs
MOVWF   TRISC        ;and set RC<7:4,1:0>
                        ;as outputs
```

The location of the CCP2 function is controlled by the CCP2SEL bit in the APFCON register (refer to Register 6-1).

REGISTER 6-10: PORTC: PORTC REGISTER

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|-------|-------|-------|-------|-------|-------|-------|-------|
| RC7 | RC6 | RC5 | RC4 | RC3 | RC2 | RC1 | RC0 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-0 **RC<7:0>**: PORTC General Purpose I/O Pin bits

1 = Port pin is > V_{IH}

0 = Port pin is < V_{IL}

REGISTER 6-11: TRISC: PORTC TRI-STATE REGISTER

| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|--------|--------|--------|--------|--------|--------|--------|--------|
| TRISC7 | TRISC6 | TRISC5 | TRISC4 | TRISC3 | TRISC2 | TRISC1 | TRISC0 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-0 **TRISC<7:0>**: PORTC Tri-State Control bits

1 = PORTC pin configured as an input (tri-stated)

0 = PORTC pin configured as an output

9.1.5 INTERRUPTS

The ADC module allows for the ability to generate an interrupt upon completion of an Analog-to-Digital conversion. The ADC interrupt flag is the ADIF bit in the PIR1 register. The ADC interrupt enable is the ADIE bit in the PIE1 register. The ADIF bit must be cleared in software.

- Note 1:** The ADIF bit is set at the completion of every conversion, regardless of whether or not the ADC interrupt is enabled.
- 2:** The ADC operates during Sleep only when the FRC oscillator is selected.

This interrupt can be generated while the device is operating or while in Sleep. If the device is in Sleep, the interrupt will wake-up the device. Upon waking from Sleep, the next instruction following the SLEEP instruction is always executed. If the user is attempting to wake-up from Sleep and resume in-line code execution, the GIE and PEIE bits of the INTCON register must be disabled. If the GIE and PEIE bits of the INTCON register are enabled, execution will switch to the Interrupt Service Routine.

Please refer to **Section 9.1.5 “Interrupts”** for more information.

9.2 ADC Operation

9.2.1 STARTING A CONVERSION

To enable the ADC module, the ADON bit of the ADCON0 register must be set to a '1'. Setting the GO/DONE bit of the ADCON0 register to a '1' will start the Analog-to-Digital conversion.

Note: The GO/DONE bit should not be set in the same instruction that turns on the ADC. Refer to **Section 9.2.6 “A/D Conversion Procedure”**.

9.2.2 COMPLETION OF A CONVERSION

When the conversion is complete, the ADC module will:

- Clear the GO/DONE bit
- Set the ADIF Interrupt Flag bit
- Update the ADRES register with new conversion result

9.2.3 TERMINATING A CONVERSION

If a conversion must be terminated before completion, the GO/DONE bit can be cleared in software. The ADRES register will be updated with the partially complete Analog-to-Digital conversion sample. Incomplete bits will match the last bit converted.

Note: A device Reset forces all registers to their Reset state. Thus, the ADC module is turned off and any pending conversion is terminated.

9.2.4 ADC OPERATION DURING SLEEP

The ADC module can operate during Sleep. This requires the ADC clock source to be set to the FRC option. When the FRC clock source is selected, the ADC waits one additional instruction before starting the conversion. This allows the SLEEP instruction to be executed, which can reduce system noise during the conversion. If the ADC interrupt is enabled, the device will wake-up from Sleep when the conversion completes. If the ADC interrupt is disabled, the ADC module is turned off after the conversion completes, although the ADON bit remains set.

When the ADC clock source is something other than FRC, a SLEEP instruction causes the present conversion to be aborted and the ADC module is turned off, although the ADON bit remains set.

9.2.5 SPECIAL EVENT TRIGGER

The Special Event Trigger of the CCP module allows periodic ADC measurements without software intervention. When this trigger occurs, the GO/DONE bit is set by hardware and the Timer1 counter resets to zero.

Using the Special Event Trigger does not assure proper ADC timing. It is the user's responsibility to ensure that the ADC timing requirements are met.

Refer to **Section 15.0 “Capture/Compare/PWM (CCP) Module”** for more information.

9.3 A/D Acquisition Requirements

For the ADC to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The Analog Input model is shown in Figure 9-3. The source impedance (Rs) and the internal sampling switch (RSS) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (RSS) impedance varies over the device voltage (VDD), refer to Figure 9-3. **The maximum recommended impedance for analog sources is 10 kΩ.** As the source

impedance is decreased, the acquisition time may be decreased. After the analog input channel is selected (or changed), an A/D acquisition must be done before the conversion can be started. To calculate the minimum acquisition time, Equation 9-1 may be used. This equation assumes that 1/2 LSB error is used (256 steps for the ADC). The 1/2 LSB error is the maximum error allowed for the ADC to meet its specified resolution.

EQUATION 9-1: ACQUISITION TIME EXAMPLE

Assumptions: Temperature = 50°C and external impedance of 10kΩ 5.0V VDD

$$\begin{aligned} T_{ACQ} &= \text{Amplifier Settling Time} + \text{Hold Capacitor Charging Time} + \text{Temperature Coefficient} \\ &= T_{AMP} + T_C + T_{COFF} \\ &= 2\mu s + T_C + [(Temperature - 25^\circ C)(0.05\mu s/^\circ C)] \end{aligned}$$

The value for TC can be approximated with the following equations:

$$V_{APPLIED} \left(1 - \frac{1}{(2^{n+1}) - 1} \right) = V_{CHOLD} \quad ;[1] \text{ } V_{CHOLD} \text{ charged to within } 1/2 \text{ lsb}$$

$$V_{APPLIED} \left(1 - e^{\frac{-T_C}{RC}} \right) = V_{CHOLD} \quad ;[2] \text{ } V_{CHOLD} \text{ charge response to } V_{APPLIED}$$

$$V_{APPLIED} \left(1 - e^{\frac{-T_C}{RC}} \right) = V_{APPLIED} \left(1 - \frac{1}{(2^{n+1}) - 1} \right) \quad ;\text{combining [1] and [2]}$$

Note: Where n = number of bits of the ADC.

Solving for TC:

$$\begin{aligned} T_C &= -CHOLD(RIC + RSS + Rs) \ln(1/511) \\ &= -10pF(1k\Omega + 7k\Omega + 10k\Omega) \ln(0.001957) \\ &= 1.12\mu s \end{aligned}$$

Therefore:

$$\begin{aligned} T_{ACQ} &= 2\mu s + 1.12\mu s + [(50^\circ C - 25^\circ C)(0.05\mu s/^\circ C)] \\ &= 4.42\mu s \end{aligned}$$

Note 1: The reference voltage (VREF) has no effect on the equation, since it cancels itself out.

2: The charge holding capacitor (CHOLD) is not discharged after each conversion.

3: The maximum recommended impedance for analog sources is 10 kΩ. This is required to meet the pin leakage specification.

14.1 Analog MUX

The capacitive sensing module can monitor up to 8 inputs. The capacitive sensing inputs are defined as CPS<7:0>. To determine if a frequency change has occurred the user must:

- Select the appropriate CPS pin by setting the CPSCH<2:0> bits of the CPSCON1 register
- Set the corresponding ANSEL bit
- Set the corresponding TRIS bit
- Run the software algorithm

Selection of the CPSx pin while the module is enabled will cause the capacitive sensing oscillator to be on the CPSx pin. Failure to set the corresponding ANSEL and TRIS bits can cause the capacitive sensing oscillator to stop, leading to false frequency readings.

14.2 Capacitive Sensing Oscillator

The capacitive sensing oscillator consists of a constant current source and a constant current sink, to produce a triangle waveform. The CPSOUT bit of the CPSCON0 register shows the status of the capacitive sensing oscillator, whether it is a sinking or sourcing current. The oscillator is designed to drive a capacitive load (single PCB pad) and at the same time, be a clock source to either Timer0 or Timer1. The oscillator has three different current settings as defined by CPS-RNG<1:0> of the CPSCON0 register. The different current settings for the oscillator serve two purposes:

- Maximize the number of counts in a timer for a fixed-time base
- Maximize the count differential in the timer during a change in frequency

14.3 Timer Resources

To measure the change in frequency of the capacitive sensing oscillator, a fixed-time base is required. For the period of the fixed-time base, the capacitive sensing oscillator is used to clock either Timer0 or Timer1. The frequency of the capacitive sensing oscillator is equal to the number of counts in the timer divided by the period of the fixed-time base.

14.4 Fixed-Time Base

To measure the frequency of the capacitive sensing oscillator, a fixed-time base is required. Any timer resource or software loop can be used to establish the fixed-time base. It is up to the end user to determine the method in which the fixed-time base is generated.

Note: The fixed-time base can not be generated by the timer resource the capacitive sensing oscillator is clocking.

14.4.1 TIMER0

To select Timer0 as the timer resource for the capacitive sensing module:

- Set the T0XCS bit of the CPSCON0 register
- Clear the T0CS bit of the OPTION register

When Timer0 is chosen as the timer resource, the capacitive sensing oscillator will be the clock source for Timer0. Refer to **Section 11.0 “Timer0 Module”** for additional information.

14.4.2 TIMER1

To select Timer1 as the timer resource for the capacitive sensing module, set the TMR1CS<1:0> of the T1CON register to ‘11’. When Timer1 is chosen as the timer resource, the capacitive sensing oscillator will be the clock source for Timer1. Because the Timer1 module has a gate control, developing a time base for the frequency measurement can be simplified using either:

- The Timer0 overflow flag
- The Timer2 overflow flag
- The WDT overflow flag

It is recommended that one of these flags, in conjunction with the toggle mode of the Timer1 gate, is used to develop the fixed-time base required by the software portion of the capacitive sensing module. Refer to **Section 12.0 “Timer1 Module with Gate Control”** for additional information.

TABLE 14-1: TIMER1 ENABLE FUNCTION

| TMR1ON | TMR1GE | Timer1 Operation |
|--------|--------|------------------------|
| 0 | 0 | Off |
| 0 | 1 | Off |
| 1 | 0 | On |
| 1 | 1 | Count Enabled by input |

14.5 Software Control

The software portion of the capacitive sensing module is required to determine the change in frequency of the capacitive sensing oscillator. This is accomplished by the following:

- Setting a fixed-time base to acquire counts on Timer0 or Timer1
- Establishing the nominal frequency for the capacitive sensing oscillator
- Establishing the reduced frequency for the capacitive sensing oscillator due to an additional capacitive load
- Set the frequency threshold

14.5.1 NOMINAL FREQUENCY (NO CAPACITIVE LOAD)

To determine the nominal frequency of the capacitive sensing oscillator:

- Remove any extra capacitive load on the selected CPSx pin
- At the start of the fixed-time base, clear the timer resource
- At the end of the fixed-time base, save the value in the timer resource

The value of the timer resource is the number of oscillations of the capacitive sensing oscillator for the given time base. The frequency of the capacitive sensing oscillator is equal to the number of counts on in the timer divided by the period of the fixed-time base.

14.5.2 REDUCED FREQUENCY (ADDITIONAL CAPACITIVE LOAD)

The extra capacitive load will cause the frequency of the capacitive sensing oscillator to decrease. To determine the reduced frequency of the capacitive sensing oscillator:

- Add a typical capacitive load on the selected CPSx pin
- Use the same fixed-time base as the nominal frequency measurement
- At the start of the fixed-time base, clear the timer resource
- At the end of the fixed-time base, save the value in the timer resource

The value of the timer resource is the number of oscillations of the capacitive sensing oscillator with an additional capacitive load. The frequency of the capacitive sensing oscillator is equal to the number of counts on in the timer divided by the period of the fixed-time base. This frequency should be less than the value obtained during the nominal frequency measurement.

14.5.3 FREQUENCY THRESHOLD

The frequency threshold should be placed midway between the value of nominal frequency and the reduced frequency of the capacitive sensing oscillator. Refer to Application Note *AN1103, Software Handling for Capacitive Sensing* (DS01103) for more detailed information the software required for capacitive sensing module.

| | |
|--------------|--|
| Note: | For more information on general capacitive sensing refer to Application Notes: <ul style="list-style-type: none">• <i>AN1101, Introduction to Capacitive Sensing</i> (DS01101)• <i>AN1102, Layout and Physical Design Guidelines for Capacitive Sensing</i> (DS01102) |
|--------------|--|

16.1.2 AUSART ASYNCHRONOUS RECEIVER

The Asynchronous mode is typically used in RS-232 systems. The receiver block diagram is shown in Figure 16-2. The data is received on the RX/DT pin and drives the data recovery block. The data recovery block is actually a high-speed shifter operating at 16 times the baud rate, whereas the serial Receive Shift Register (RSR) operates at the bit rate. When all eight or nine bits of the character have been shifted in, they are immediately transferred to a two character First-In First-Out (FIFO) memory. The FIFO buffering allows reception of two complete characters and the start of a third character before software must start servicing the AUSART receiver. The FIFO and RSR registers are not directly accessible by software. Access to the received data is via the RCREG register.

16.1.2.1 Enabling the Receiver

The AUSART receiver is enabled for asynchronous operation by configuring the following three control bits:

- CREN = 1
- SYNC = 0
- SPEN = 1

All other AUSART control bits are assumed to be in their default state.

Setting the CREN bit of the RCSTA register enables the receiver circuitry of the AUSART. Clearing the SYNC bit of the TXSTA register configures the AUSART for asynchronous operation. Setting the SPEN bit of the RCSTA register enables the AUSART and automatically configures the RX/DT I/O pin as an input.

Note: When the SPEN bit is set the TX/CK I/O pin is automatically configured as an output, regardless of the state of the corresponding TRIS bit and whether or not the AUSART transmitter is enabled. The PORT latch is disconnected from the output driver so it is not possible to use the TX/CK pin as a general purpose output.

16.1.2.2 Receiving Data

The receiver data recovery circuit initiates character reception on the falling edge of the first bit. The first bit, also known as the Start bit, is always a zero. The data recovery circuit counts one-half bit time to the center of the Start bit and verifies that the bit is still a zero. If it is not a zero then the data recovery circuit aborts character reception, without generating an error, and resumes looking for the falling edge of the Start bit. If the Start bit zero verification succeeds then the data recovery circuit counts a full bit time to the center of the next bit. The bit is then sampled by a majority detect circuit and the resulting '0' or '1' is shifted into the RSR. This repeats until all data bits have been sampled and shifted into the RSR. One final bit time is measured and the level sampled. This is the Stop bit, which is always a '1'. If the data recovery circuit samples a '0' in the Stop bit position then a framing error is set for this character, otherwise the framing error is cleared for this character. Refer to **Section 16.1.2.4 "Receive Framing Error"** for more information on framing errors.

Immediately after all data bits and the Stop bit have been received, the character in the RSR is transferred to the AUSART receive FIFO and the RCIF interrupt flag bit of the PIR1 register is set. The top character in the FIFO is transferred out of the FIFO by reading the RCREG register.

Note: If the receive FIFO is overrun, no additional characters will be received until the overrun condition is cleared. Refer to **Section 16.1.2.5 "Receive Overrun Error"** for more information on overrun errors.

16.1.2.3 Receive Interrupts

The RCIF interrupt flag bit of the PIR1 register is set whenever the AUSART receiver is enabled and there is an unread character in the receive FIFO. The RCIF interrupt flag bit is read-only, it cannot be set or cleared by software.

RCIF interrupts are enabled by setting all of the following bits:

- RCIE, Receive Interrupt Enable bit of the PIE1 register
- PEIE, Peripheral Interrupt Enable bit of the INTCON register
- GIE, Global Interrupt Enable bit of the INTCON register

The RCIF interrupt flag bit of the PIR1 register will be set when there is an unread character in the FIFO, regardless of the state of interrupt enable bits.

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TABLE 16-2: REGISTERS ASSOCIATED WITH ASYNCHRONOUS RECEPTION

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR, BOR | Value on all other Resets |
|--------|------------------------------|--------|--------|--------|--------|--------|--------|--------|-------------------|---------------------------|
| INTCON | GIE | PEIE | T0IE | INTE | RBIE | T0IF | INTF | RBIF | 0000 000x | 0000 000x |
| PIE1 | TMR1GIE | ADIE | RCIE | TXIE | SSPIE | CCP1IE | TMR2IE | TMR1IE | 0000 0000 | 0000 0000 |
| PIR1 | TMR1GIF | ADIF | RCIF | TXIF | SSPIF | CCP1IF | TMR2IF | TMR1IF | 0000 0000 | 0000 0000 |
| RCREG | AUSART Receive Data Register | | | | | | | | 0000 0000 | 0000 0000 |
| RCSTA | SPEN | RX9 | SREN | CREN | ADDEN | FERR | OERR | RX9D | 0000 000x | 0000 000x |
| SPBRG | BRG7 | BRG6 | BRG5 | BRG4 | BRG3 | BRG2 | BRG1 | BRG0 | 0000 0000 | 0000 0000 |
| TRISC | TRISC7 | TRISC6 | TRISC5 | TRISC4 | TRISC3 | TRISC2 | TRISC1 | TRISC0 | 1111 1111 | 1111 1111 |
| TXSTA | CSRC | TX9 | TXEN | SYNC | — | BRGH | TRMT | TX9D | 0000 -010 | 0000 -010 |

Legend: x = unknown, - = unimplemented read as '0'. Shaded cells are not used for asynchronous reception.

REGISTER 17-2: SSPSTAT: SYNC SERIAL PORT STATUS REGISTER (SPI MODE)

| | | | | | | | |
|-------|-------|-----|-----|-----|-----|-----|-------|
| R/W-0 | R/W-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| SMP | CKE | D/A | P | S | R/W | UA | BF |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

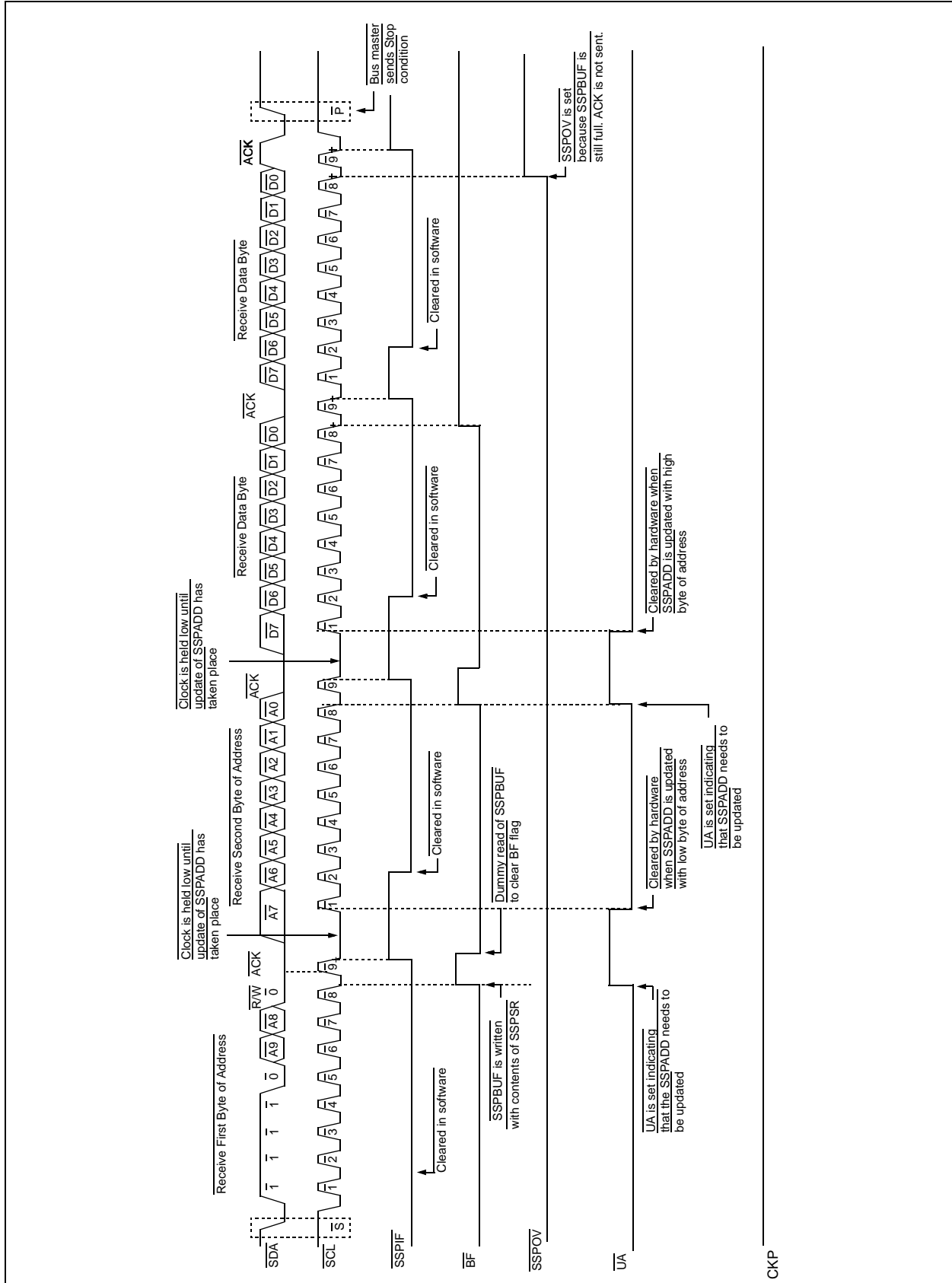
'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 7 **SMP:** SPI Data Input Sample Phase bit
SPI Master mode:
 1 = Input data sampled at end of data output time
 0 = Input data sampled at middle of data output time
SPI Slave mode:
 SMP must be cleared when SPI is used in Slave mode
- bit 6 **CKE:** SPI Clock Edge Select bit
SPI mode, CKP = 0:
 1 = Data stable on rising edge of SCK
 0 = Data stable on falling edge of SCK
SPI mode, CKP = 1:
 1 = Data stable on falling edge of SCK
 0 = Data stable on rising edge of SCK
- bit 5 **D/A:** Data/Address bit
 Used in I²C mode only.
- bit 4 **P:** Stop bit
 Used in I²C mode only.
- bit 3 **S:** Start bit
 Used in I²C mode only.
- bit 2 **R/W:** Read/Write Information bit
 Used in I²C mode only.
- bit 1 **UA:** Update Address bit
 Used in I²C mode only.
- bit 0 **BF:** Buffer Full Status bit
 1 = Receive complete, SSPBUF is full
 0 = Receive not complete, SSPBUF is empty

FIGURE 17-11: I²C SLAVE MODE TIMING (RECEPTION, 10-BIT ADDRESS)



SUBWF **Subtract W from f**

Syntax: `[label] SUBWF f,d`

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: $(f) - (W) \rightarrow (\text{destination})$

Status Affected: C, DC, Z

Description: Subtract (2's complement method) W register from register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

| | |
|--------|----------------------|
| C = 0 | $W > f$ |
| C = 1 | $W \leq f$ |
| DC = 0 | $W<3:0> > f<3:0>$ |
| DC = 1 | $W<3:0> \leq f<3:0>$ |

XORLW **Exclusive OR literal with W**

Syntax: `[label] XORLW k`

Operands: $0 \leq k \leq 255$

Operation: $(W) .XOR. k \rightarrow (W)$

Status Affected: Z

Description: The contents of the W register are XOR'ed with the 8-bit literal 'k'. The result is placed in the W register.

SWAPF **Swap Nibbles in f**

Syntax: `[label] SWAPF f,d`

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: $(f<3:0>) \rightarrow (\text{destination}<7:4>),$
 $(f<7:4>) \rightarrow (\text{destination}<3:0>)$

Status Affected: None

Description: The upper and lower nibbles of register 'f' are exchanged. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in register 'f'.

XORWF **Exclusive OR W with f**

Syntax: `[label] XORWF f,d`

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: $(W) .XOR. (f) \rightarrow (\text{destination})$

Status Affected: Z

Description: Exclusive OR the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

PIC16(L)F722A/723A

FIGURE 24-14: PIC16LF722A/723A MAXIMUM I_{DD} vs. V_{DD} OVER F_{OSC} , XT MODE

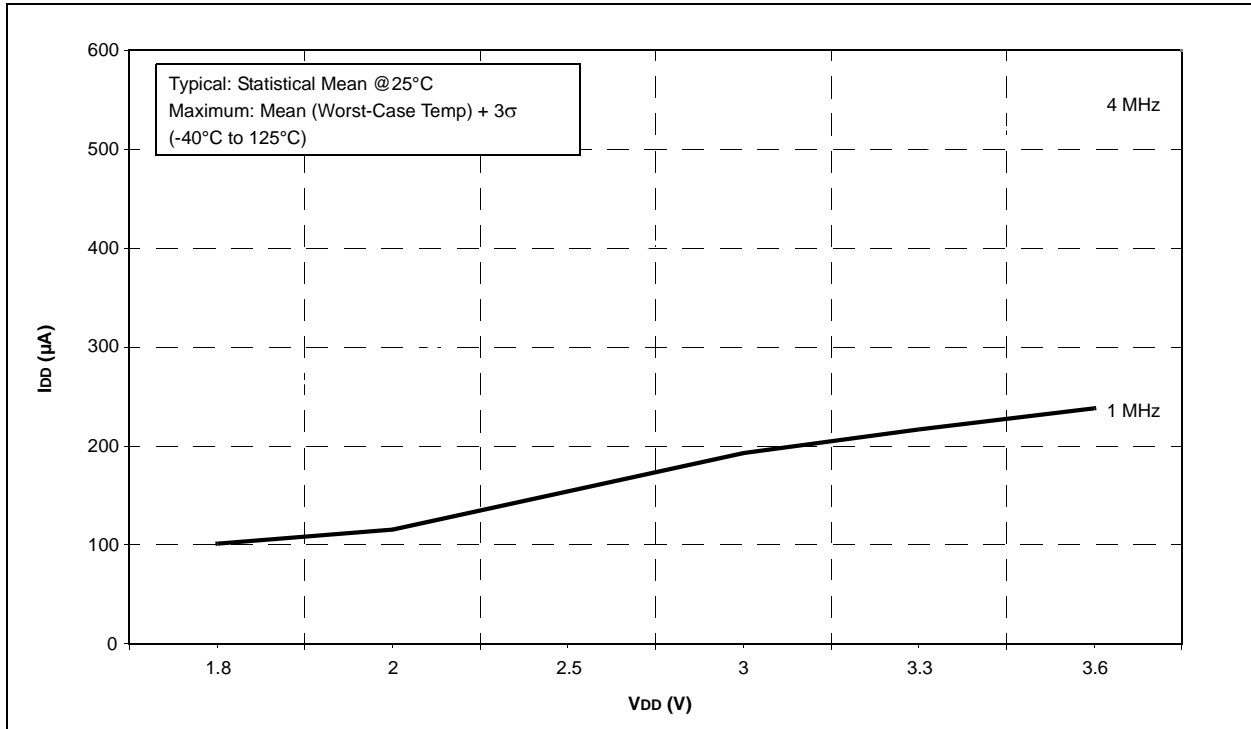
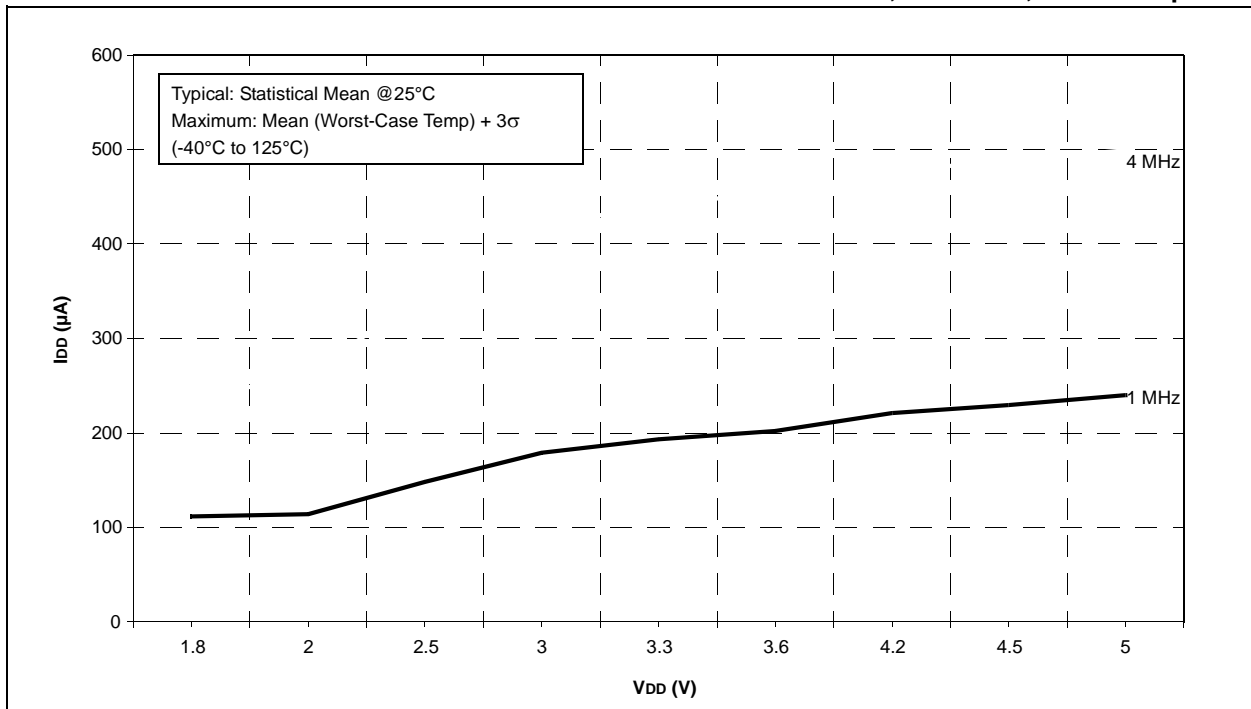


FIGURE 24-15: PIC16F722A/723A TYPICAL I_{DD} vs. V_{DD} OVER F_{OSC} , XT MODE, $V_{CAP} = 0.1\mu F$



PIC16(L)F722A/723A

FIGURE 24-44: PIC16LF722A/723A TYPICAL ADC IPD vs. VDD

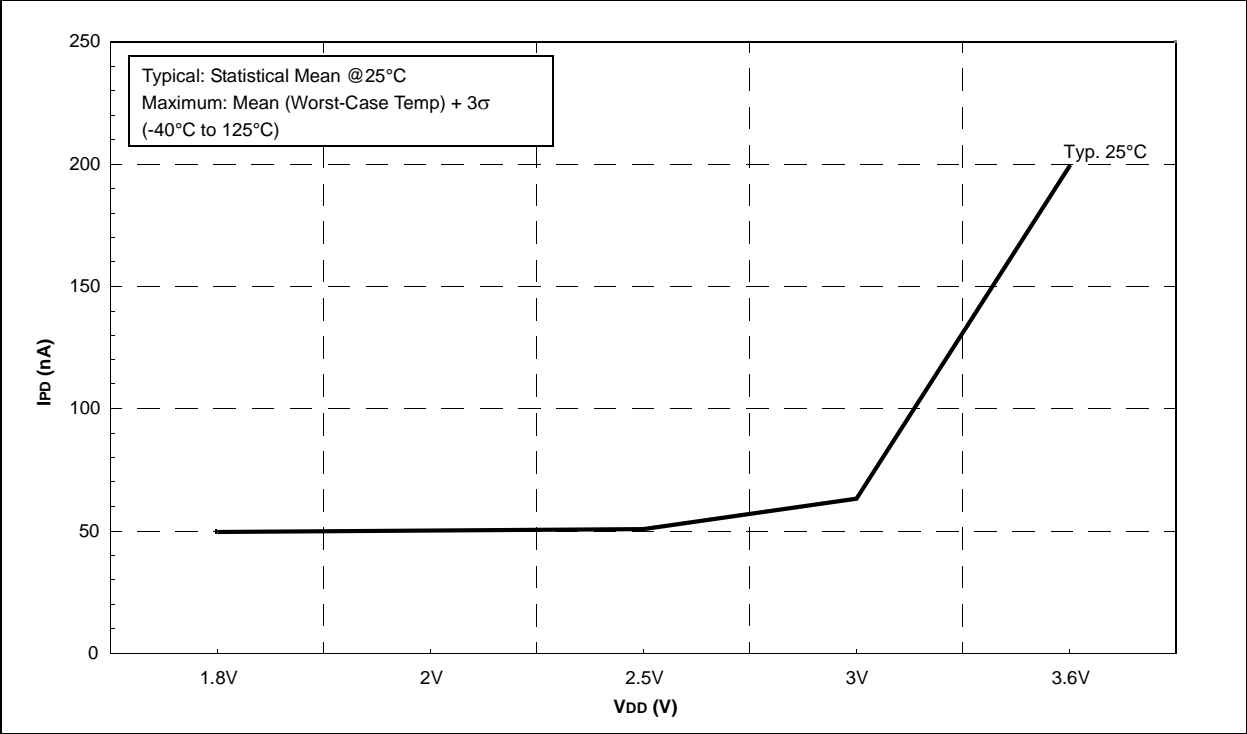


FIGURE 24-45: PIC16F722A/723A ADC IPD vs. VDD, VCAP = 0.1μF

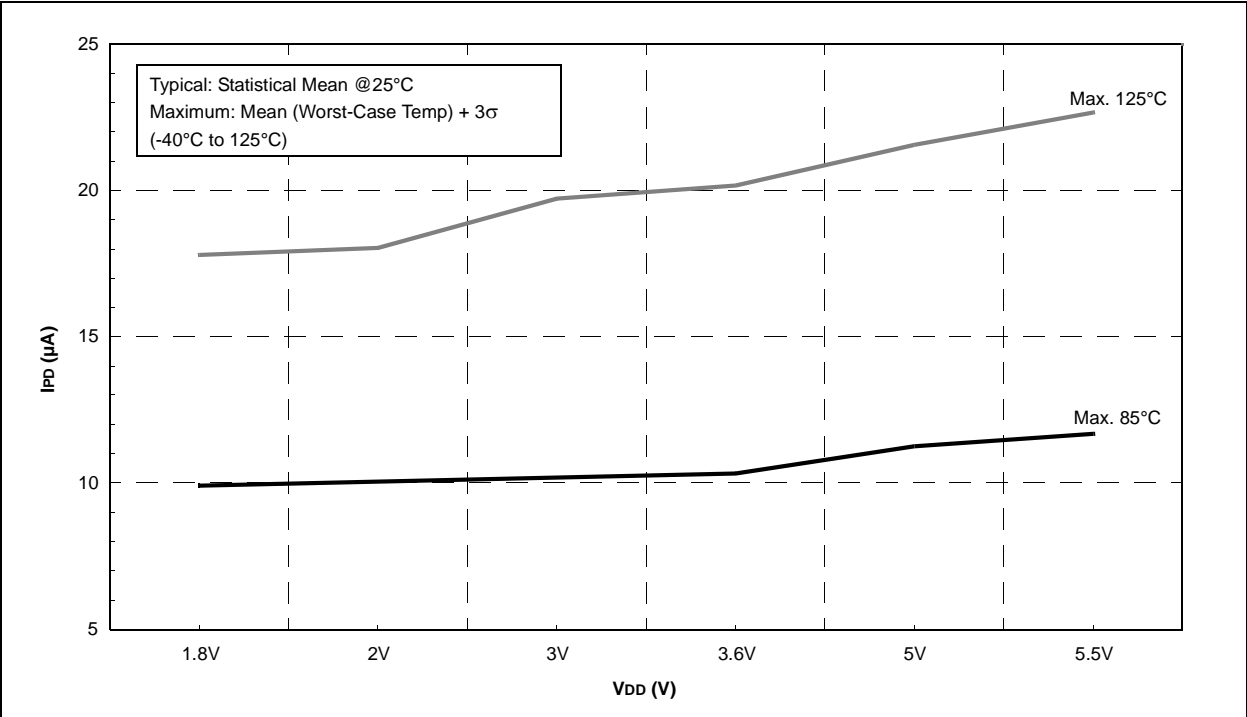


FIGURE 24-50: SCHMITT TRIGGER INPUT THRESHOLD V_{IN} vs. V_{DD} OVER TEMPERATURE

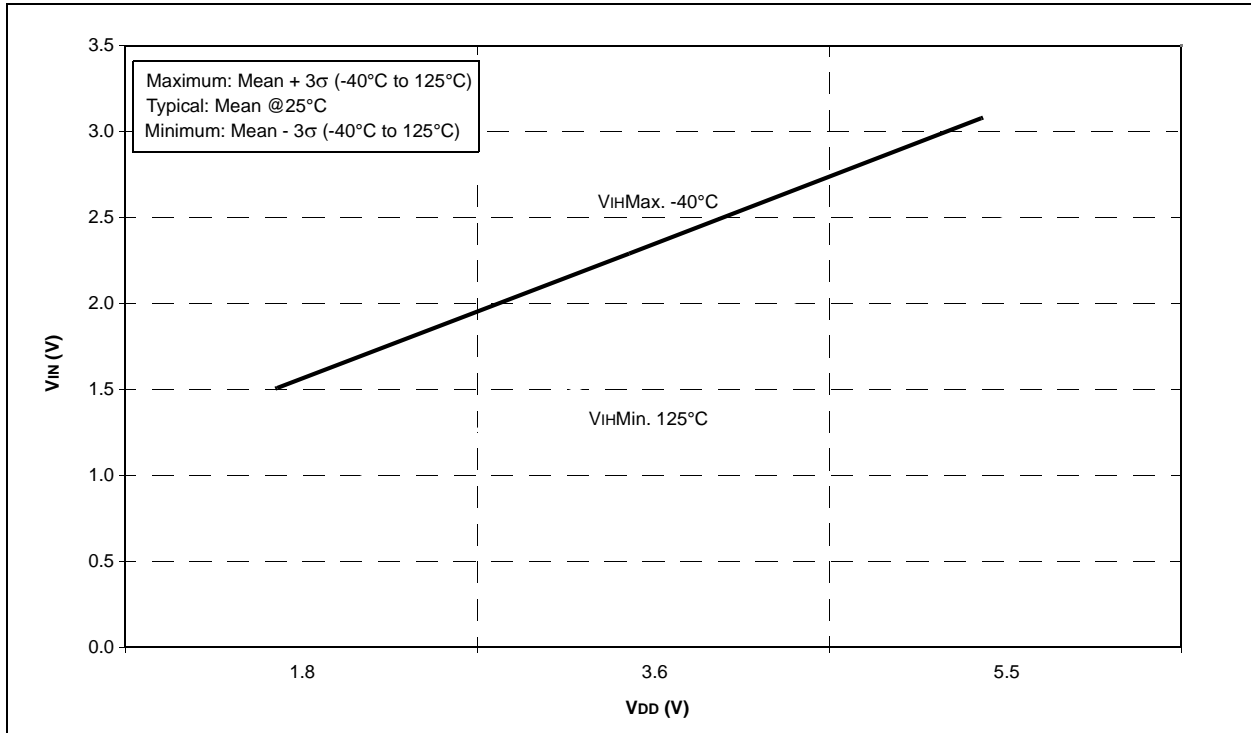


FIGURE 24-51: SCHMITT TRIGGER INPUT THRESHOLD V_{IN} vs. V_{DD} OVER TEMPERATURE

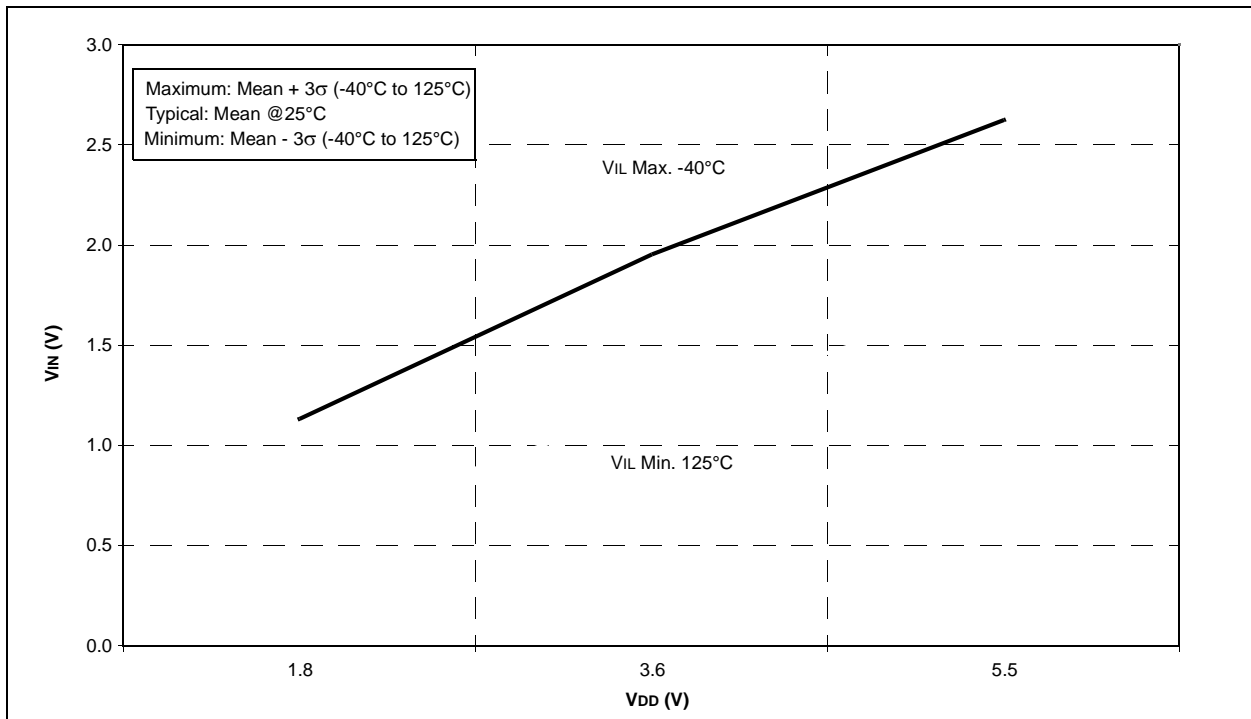


FIGURE 24-54: V_{OH} vs. I_{OH} OVER TEMPERATURE, $V_{DD} = 1.8V$

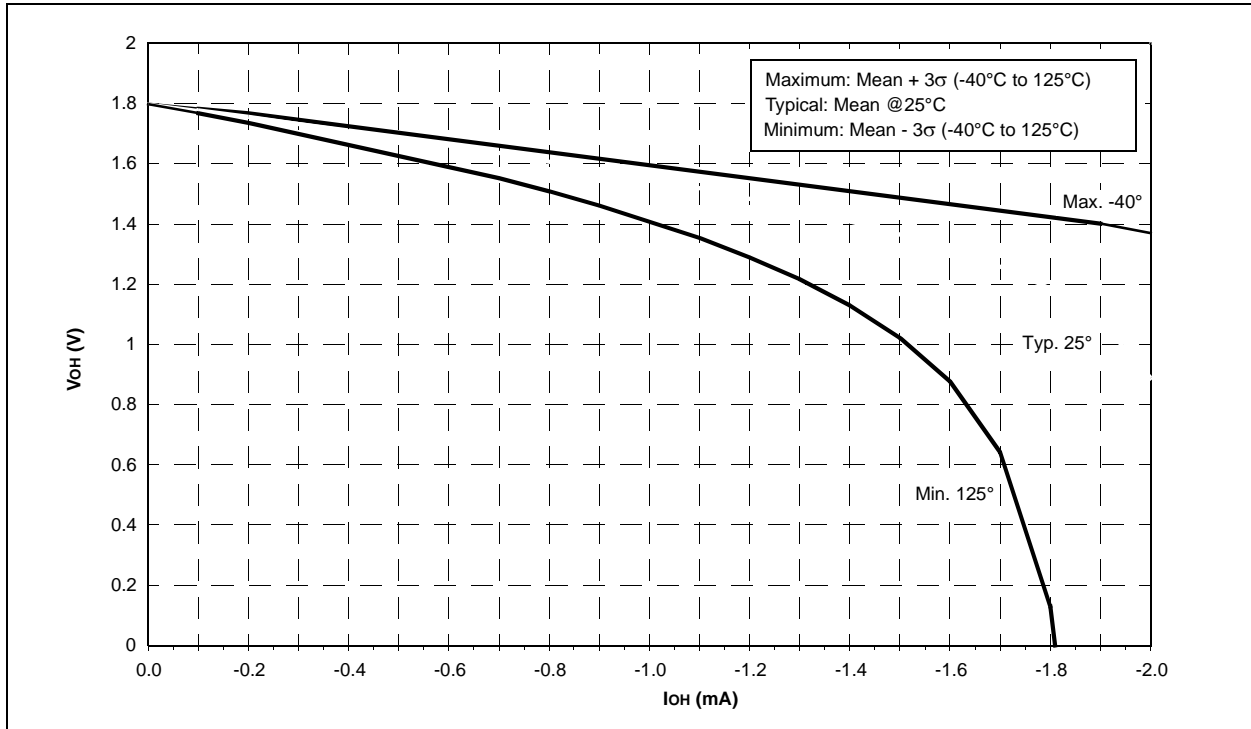
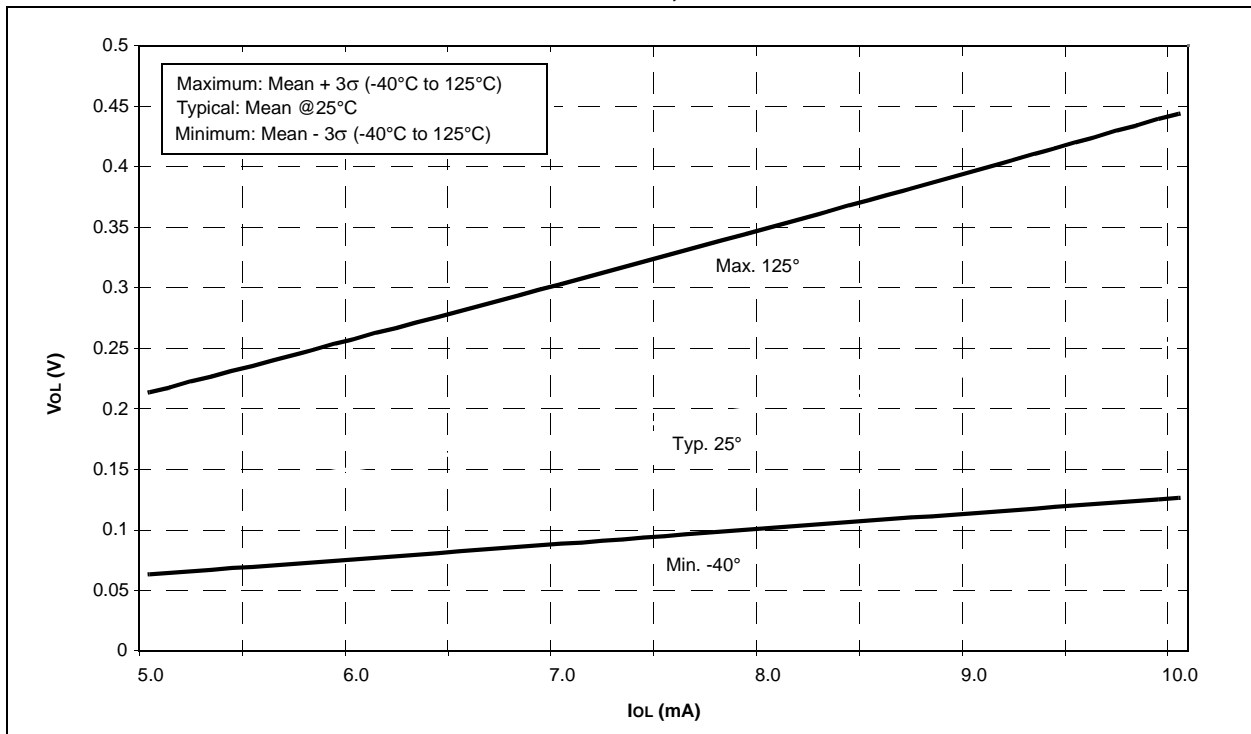
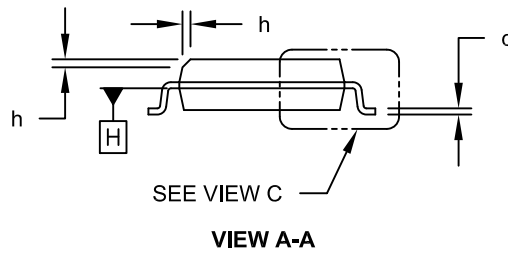
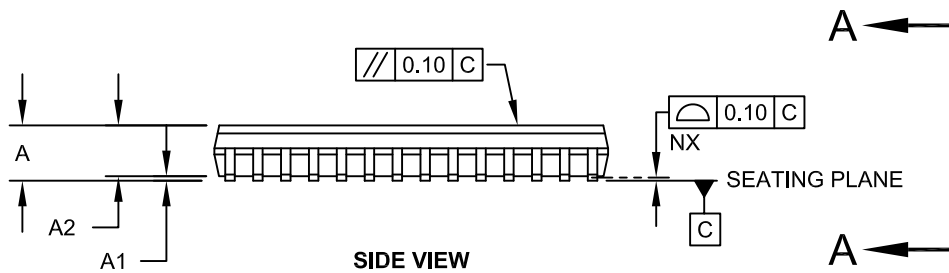
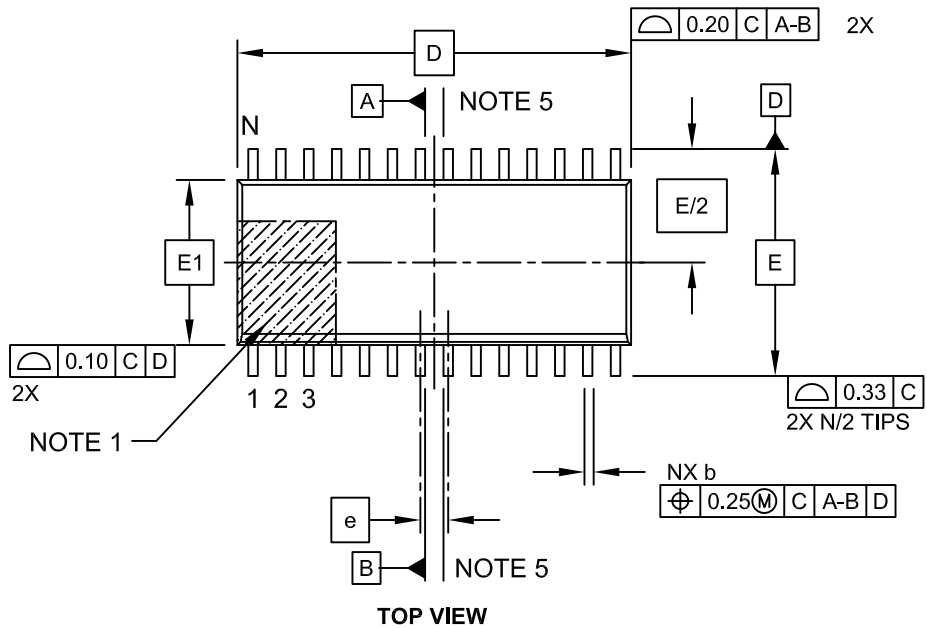


FIGURE 24-55: V_{OL} vs. I_{OL} OVER TEMPERATURE, $V_{DD} = 5.5V$





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