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#### Details

-XE

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I <sup>2</sup> C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 11x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf722a-e-ml

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

#### Pin Diagrams - 28-PIN SPDIP/SOIC/SSOP/QFN/UQFN (PIC16(L)F722A/723A)



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### 1.0 DEVICE OVERVIEW

The PIC16(L)F722A/723A devices are covered by this data sheet. They are available in 28-pin packages. Figure 1-1 shows a block diagram of the PIC16(L)F722A/723A devices. Table 1-1 shows the pinout descriptions.

#### FIGURE 2-3:

### PIC16(L)F722A SPECIAL FUNCTION REGISTERS

	00h	Indirect addr.(*)	80h	Indirect addr. <sup>(*)</sup>	100h	Indirect addr.(*)	180h
TMR0	01h	OPTION	81h	TMR0	101h	OPTION	181h
PCL	02h	PCL	82h	PCL	102h	PCL	182h
STATUS	03h	STATUS	83h	STATUS	103h	STATUS	183h
FSR	04h	FSR	84h	FSR	104h	FSR	184h
PORTA	05h	TRISA	85h		105h	ANSELA	185h
PORTB	06h	TRISB	86h		106h	ANSELB	186h
PORTC	07h	TRISC	87h		107h		187h
	08h		88h	CPSCON0	108h		188h
PORTE	09h	TRISE	89h	CPSCON1	109h		189h
PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18Ah
INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18Bh
PIR1	0Ch	PIE1	8Ch	PMDATL	10Ch	PMCON1	18Ch
PIR2	0Dh	PIE2	8Dh	PMADRL	10Dh	Reserved	18Dh
TMR1L	0Eh	PCON	8Eh	PMDATH	10Eh	Reserved	18Eh
TMR1H	0Fh	T1GCON	8Fh	PMADRH	10Fh	Reserved	18Fh
T1CON	10h	OSCCON	90h		110h		190h
TMR2	11h	OSCTUNE	91h		111h		191h
T2CON	12h	PR2	92h		112h		192h
SSPBUF	13h	SSPADD/SSPMS	K 93h		113h		193h
SSPCON	14h	SSPSTAT	94h		114h		194h
CCPR1L	15h	WPUB	95h		115h		195h
CCPR1H	16h	IOCB	96h		116h		196h
CCP1CON	17h		97h		117h		197h
RCSTA	18h	TXSTA	98h		118h		198h
TXREG	19h	SPBRG	99h		119h		199h
RCREG	1Ah		9Ah		11Ah		19Ah
CCPR2L	1Bh		9Bh		11Bh		19Bh
CCPR2H	1Ch	APFCON	9Ch		11Ch		19Ch
CCP2CON	1Dh	FVRCON	9Dh		11Dh		19Dh
ADRES	1Eh		9Eh		11Eh		19Eh
ADCON0	1Fh	ADCON1	9Fh		11Fh		19Fh
	20h		A0h		120h		1A0h
		General					
		Purpose					
		Register					
_		32 Bytes					
General			BFh				
Purpose			C0h				
96 Bytes			FFh		16Fh		1EEb
00 0,000		-	F0h		170h	-	1E0h
		Accesses		Accesses		Accesses	
		/01-/11				/01-/11	
	7Fh		FFh		17Fh		1FFh
Bank 0		Bank 1		Bank 2		Bank 3	

#### TABLE 3-5: INITIALIZATION CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	STATUS Register	PCON Register
Power-on Reset	0000h	0001 1xxx	0x
MCLR Reset during normal operation	0000h	000u uuuu	uu
MCLR Reset during Sleep	0000h	0001 Ouuu	uu
WDT Reset	0000h	0000 uuuu	uu
WDT Wake-up	PC + 1	uuu0 0uuu	uu
Brown-out Reset	0000h	0001 1xxx	10
Interrupt Wake-up from Sleep	PC + 1 <sup>(1)</sup>	uuul Ouuu	uu

**Legend:** u = unchanged, x = unknown, - = unimplemented bit, reads as '0'.

**Note 1:** When the wake-up is due to an interrupt and Global Interrupt Enable bit, GIE, is set, the PC is loaded with the interrupt vector (0004h) after execution of PC + 1.

#### TABLE 3-6: SUMMARY OF REGISTERS ASSOCIATED WITH RESETS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
STATUS	IRP	RP1	RP0	TO	PD	Z	DC	С	18
PCON	—	_	_	_	_	_	POR	BOR	20

**Legend:** u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition. Shaded cells are not used by Resets.

**Note 1:** Other (non Power-up) Resets include MCLR Reset and Watchdog Timer Reset during normal operation.











#### 7.4 Oscillator Control

The Oscillator Control (OSCCON) register (Figure 7-1) displays the status and allows frequency selection of the internal oscillator (INTOSC) system clock. The OSCCON register contains the following bits:

- Frequency selection bits (IRCF)
- Status Locked bits (ICSL)
- Status Stable bits (ICSS)

#### REGISTER 7-1: OSCCON: OSCILLATOR CONTROL REGISTER

U-0	U-0	R/W-1	R/W-0	R-q	R-q	U-0	U-0
—	—	IRCF1	IRCF0	ICSL	ICSS	—	—
bit 7							bit 0
Legend:							

3				
R = Readable bit	W = Writable bit	U = Unimplemented bit	, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	
q = Value depends on c	ondition			

bit 7-6	Unimplemented: Read as '0'
bit 5-4	IRCF<1:0>: Internal Oscillator Frequency Select bits
	When PLLEN = 1 (16 MHz INTOSC)
	11 <b>= 16 MHz</b>
	10 = 8 MHz (POR value)
	01 = 4  MHz
	00 = 2  MHz
	<u>When PLLEN = 0 (500 kHz INTOSC)</u>
	11 = 500  kHz
	10 = 250 kHz (POR value)
	01 = 125 kHz
	00 = 62.5  KHz
bit 3	ICSL: Internal Clock Oscillator Status Locked bit (2% Stable)
	1 = 16 MHz/500 kHz Internal Oscillator (HFIOSC) is in lock
	0 = 16 MHz/500 kHz Internal Oscillator (HFIOSC) has not yet locked
bit 2	ICSS: Internal Clock Oscillator Status Stable bit (0.5% Stable)
	1 = 16  MHz/500  kHz Internal Oscillator (HFIOSC) has stabilized to its maximum accuracy 0 = 16  MHz/500  kHz Internal Oscillator (HEIOSC) has not vet reached its maximum accuracy
hit 1 0	
	Uninpiententeu. Reau as 0

### 12.11 Timer1 Control Register

The Timer1 Control register (T1CON), shown in Register 12-1, is used to control Timer1 and select the various features of the Timer1 module.

#### REGISTER 12-1: T1CON: TIMER1 CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
TMR1CS1	TMR1CS0	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	—	TMR10N
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6	TMR1CS<1:0>: Timer1 Clock Source Select bits
	11 = Timer1 clock source is Capacitive Sensing Oscillator (CAPOSC)
	10 = Timer1 clock source is pin or oscillator:
	$\frac{\text{If } T10\text{SCEN} = 0}{100}$
	External clock from TTCKI pin (on the rising edge)
	$\frac{ I      OSOEN = 1}{Crystal oscillator on T1OSI/T1OSO pins}$
	01 = Timer1 clock source is system clock (Fosc)
	00 = Timer1 clock source is instruction clock (Fosc/4)
bit 5-4	T1CKPS<1:0>: Timer1 Input Clock Prescale Select bits
	11 = 1:8 Prescale value
	10 = 1:4 Prescale value
	01 = 1:2 Prescale value
	00 = 1:1 Prescale value
bit 3	T1OSCEN: LP Oscillator Enable Control bit
	1 = Dedicated Timer1 oscillator circuit enabled
	0 = Dedicated Timer1 oscillator circuit disabled
bit 2	<b>T1SYNC:</b> Timer1 External Clock Input Synchronization Control bit
	$\underline{TMR1CS<1:0>} = \underline{1X}$
	1 = Do not synchronize external clock input
	0 = Synchronize external clock input with system clock (FOSC)
	TMR1CS<1:0> = 0X
	This bit is ignored. Timer1 uses the internal clock when TMR1CS<1:0> = $1X$ .
bit 1	Unimplemented: Read as '0'
bit 0	TMR1ON: Timer1 On bit
	1 = Enables Timer1
	0 = Stops Timer1 (Clears Timer1 gate flip-flop)

<b>REGISTER 14</b>	l-2: CPSCO	ON1: CAPAC	ITIVE SENS	ING CONTR	OL REGISTE	R 1		
U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	
—		—	—	—	CPSCH2	CPSCH1	CPSCH0	
bit 7	bit 7 bit 0							
Legend:								
R = Readable bit W = Writable bit			bit	U = Unimplemented bit, read as '0'				
-n = Value at POR		'1' = Bit is set		'0' = Bit is cleared		x = Bit is unknown		

bit 7-3	Unimplemented: Read as '0'						
bit 2-0	CPSCH<2:0>: Capacitive Sensing Channel Select bits						
	If CPSON = 0:						
	These bits are ignored. No channel is selected.						
	<u>If CPSON = 1</u> :						
	000 = channel 0, (CPS0)						
	001 = channel 1, (CPS1)						
	010 = channel 2, (CPS2)						
	011 = channel 3, (CPS3)						
	100 = channel 4, (CPS4)						
	101 = channel 5, (CPS5)						
	110 = channel 6, (CPS6)						
	111 = channel 7, (CPS7)						

#### TABLE 14-2: SUMMARY OF REGISTERS ASSOCIATED WITH CAPACITIVE SENSING

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELA	—	—	ANSA5	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0	44
ANSELB	—	—	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	53
OPTION_REG	RBPU	INTEDG	TOCS	T0SE	PSA	PS2	PS1	PS0	19
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	37
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	39
T1CON	TMR1CS1	TMR1CS0	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	_	TMR10N	103
T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	107
TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	43
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	52

Legend: - = Unimplemented locations, read as '0', u = unchanged, x = unknown. Shaded cells are not used by the capacitive sensing module.

#### 15.3 PWM Mode

The PWM mode generates a Pulse-Width Modulated signal on the CCPx pin. The duty cycle, period and resolution are determined by the following registers:

- PR2
- T2CON
- CCPRxL
- CCPxCON

In Pulse-Width Modulation (PWM) mode, the CCP module produces up to a 10-bit resolution PWM output on the CCPx pin.

Figure 15-3 shows a simplified block diagram of PWM operation.

Figure 15-4 shows a typical waveform of the PWM signal.

For a step-by-step procedure on how to set up the CCP module for PWM operation, refer to **Section 15.3.8** "Setup for PWM Operation".

FIGURE 15-3: SIMPLIFIED PWM BLOCK DIAGRAM



The PWM output (Figure 15-4) has a time base (period) and a time that the output stays high (duty cycle).

FIGURE 15-4: CCP PWM OUTPUT



#### 15.3.1 CCPX PIN CONFIGURATION

In PWM mode, the CCPx pin is multiplexed with the PORT data latch. The user must configure the CCPx pin as an output by clearing the associated TRIS bit.

Either RC1 or RB3 can be selected as the CCP2 pin. Refer to **Section 6.1** "Alternate Pin Function" for more information.

Note:	Clearing	the	CCPxCON	register	will
	relinquish	CCF	x control of t	he CCPx	pin.

#### 15.3.4 PWM RESOLUTION

The resolution determines the number of available duty cycles for a given period. For example, a 10-bit resolution will result in 1024 discrete duty cycles, whereas an 8-bit resolution will result in 256 discrete duty cycles.

The maximum PWM resolution is ten bits when PR2 is 255. The resolution is a function of the PR2 register value as shown by Equation 15-4.

#### EQUATION 15-4: PWM RESOLUTION

Resolution = 
$$\frac{\log[4(PR2 + 1)]}{\log(2)}$$
 bits

Note: If the pulse-width value is greater than the period, the assigned PWM pin(s) will remain unchanged.

#### TABLE 15-5: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (Fosc = 20 MHz)

PWM Frequency	1.22 kHz	4.88 kHz	19.53 kHz	78.12 kHz	156.3 kHz	208.3 kHz
Timer Prescale (1, 4, 16)	16	4	1	1	1	1
PR2 Value	0xFF	0xFF	0xFF	0x3F	0x1F	0x17
Maximum Resolution (bits)	10	10	10	8	7	6.6

#### TABLE 15-6: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (Fosc = 8 MHz)

PWM Frequency	1.22 kHz	4.90 kHz	19.61 kHz	76.92 kHz	153.85 kHz	200.0 kHz
Timer Prescale (1, 4, 16)	16	4	1	1	1	1
PR2 Value	0x65	0x65	0x65	0x19	0x0C	0x09
Maximum Resolution (bits)	8	8	8	6	5	5

#### 15.3.5 OPERATION IN SLEEP MODE

In Sleep mode, the TMR2 register will not increment and the state of the module will not change. If the CCPx pin is driving a value, it will continue to drive that value. When the device wakes up, TMR2 will continue from its previous state.

#### 15.3.6 CHANGES IN SYSTEM CLOCK FREQUENCY

The PWM frequency is derived from the system clock frequency (Fosc). Any changes in the system clock frequency will result in changes to the PWM frequency. Refer to **Section 7.0** "**Oscillator Module**" for additional details.

#### 15.3.7 EFFECTS OF RESET

Any Reset will force all ports to Input mode and the CCP registers to their Reset states.

#### 15.3.8 SETUP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for PWM operation:

- 1. Disable the PWM pin (CCPx) output driver(s) by setting the associated TRIS bit(s).
- 2. Load the PR2 register with the PWM period value.
- Configure the CCP module for the PWM mode by loading the CCPxCON register with the appropriate values.
- Load the CCPRxL register and the DCxBx bits of the CCPxCON register, with the PWM duty cycle value.
- 5. Configure and start Timer2:
  - Clear the TMR2IF interrupt flag bit of the PIR1 register. See Note below.
  - Configure the T2CKPS bits of the T2CON register with the Timer2 prescale value.
  - Enable Timer2 by setting the TMR2ON bit of the T2CON register.
- 6. Enable PWM output pin:
  - Wait until Timer2 overflows, TMR2IF bit of the PIR1 register is set. See Note below.
  - Enable the PWM pin (CCPx) output driver(s) by clearing the associated TRIS bit(s).
  - **Note:** In order to send a complete duty cycle and period on the first PWM output, the above steps must be included in the setup sequence. If it is not critical to start with a complete PWM signal on the first output, then step 6 may be ignored.

#### 16.3.2 SYNCHRONOUS SLAVE MODE

The following bits are used to configure the AUSART for Synchronous slave operation:

- SYNC = 1
- CSRC = 0
- SREN = 0 (for transmit); SREN = 1 (for receive)
- CREN = 0 (for transmit); CREN = 1 (for receive)
- SPEN = 1

Setting the SYNC bit of the TXSTA register configures the device for synchronous operation. Clearing the CSRC bit of the TXSTA register configures the device as a slave. Clearing the SREN and CREN bits of the RCSTA register ensures that the device is in the Transmit mode, otherwise the device will be configured to receive. Setting the SPEN bit of the RCSTA register enables the AUSART.

#### 16.3.2.1 AUSART Synchronous Slave Transmit

The operation of the Synchronous Master and Slave modes are identical (refer to **Section 16.3.1.2 "Synchronous Master Transmission")**, except in the case of the Sleep mode. If two words are written to the TXREG and then the SLEEP instruction is executed, the following will occur:

- 1. The first character will immediately transfer to the TSR register and transmit.
- 2. The second word will remain in TXREG register.
- 3. The TXIF bit will not be set.
- After the first character has been shifted out of TSR, the TXREG register will transfer the second character to the TSR and the TXIF bit will now be set.
- If the PEIE and TXIE bits are set, the interrupt will wake the device from Sleep and execute the next instruction. If the GIE bit is also set, the program will call the Interrupt Service Routine.
- 16.3.2.2 Synchronous Slave Transmission Setup:
- 1. Set the SYNC and SPEN bits and clear the CSRC bit.
- 2. Clear the CREN and SREN bits.
- If using interrupts, ensure that the GIE and PEIE bits of the INTCON register are set and set the TXIE bit.
- 4. If 9-bit transmission is desired, set the TX9 bit.
- 5. Enable transmission by setting the TXEN bit.
- 6. Verify address detection is disabled by clearing the ADDEN bit of the RCSTA register.
- 7. If 9-bit transmission is selected, insert the Most Significant bit into the TX9D bit.
- 8. Start transmission by writing the Least Significant eight bits to the TXREG register.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
INTCON	GIE	PEIE	TOIE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000X	0000 000X
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111
TXREG	AUSART Transmit Data Register								0000 0000	0000 0000
TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010

#### TABLE 16-8: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE TRANSMISSION

Legend: x = unknown, - = unimplemented read as '0'. Shaded cells are not used for synchronous slave transmission.

PIC16LF722A/723A			$\begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise stated)} \\ \mbox{Operating temperature} & -40^\circ C \leq TA \leq +85^\circ C \mbox{ for industrial} \\ -40^\circ C \leq TA \leq +125^\circ C \mbox{ for extended} \end{array}$							
PIC16F722A/723A			<b>Standa</b> Operati	$\begin{array}{llllllllllllllllllllllllllllllllllll$						
Param. No.	Sym.	Characteristic	Min.	Min. Typ† Max. Units Conditions						
D001	Vdd	Supply Voltage	Supply Voltage							
		PIC16LF722A/723A	1.8 1.8 2.3 2.5		3.6 3.6 3.6 3.6	V V V V	Fosc $\leq$ 16 MHz: HFINTOSC, EC Fosc $\leq$ 4 MHz Fosc $\leq$ 20 MHz, EC Fosc $\leq$ 20 MHz, HS			
D001		PIC16F722A/723A	1.8 1.8 2.3 2.5		5.5 5.5 5.5 5.5	V V V V	$\begin{array}{l} \mbox{Fosc} \leq 16 \mbox{ MHz: HFINTOSC, EC} \\ \mbox{Fosc} \leq 4 \mbox{ MHz} \\ \mbox{Fosc} \leq 20 \mbox{ MHz, EC} \\ \mbox{Fosc} \leq 20 \mbox{ MHz, HS} \end{array}$			
D002*	Vdr	RAM Data Retention Voltage <sup>(1)</sup>								
		PIC16LF722A/723A	1.5	_	_	V	Device in Sleep mode			
D002*		PIC16F722A/723A	1.7	_	_	V	Device in Sleep mode			
-	VPOR*	Power-on Reset Release Voltage	_	1.6	<b>—</b>	V				
	VPORR*	Power-on Reset Rearm Voltage		•						
		PIC16LF722A/723A		0.8	-	V	Device in Sleep mode			
		PIC16F722A/723A		1.7	—	V	Device in Sleep mode			
D003	VFVR	Fixed Voltage Reference Voltage, Initial Accuracy	-5.5 -5.5 -5.5		5.5 5.5 5.5	% % %	$ \begin{array}{l} {\sf VFVR} = 1.024{\sf V},  {\sf VDD} \geq 2.5{\sf V} \\ {\sf VFVR} = 2.048{\sf V},  {\sf VDD} \geq 2.5{\sf V} \\ {\sf VFVR} = 4.096{\sf V},  {\sf VDD} \geq 4.75{\sf V}; \\ {\sf -40} \leq {\sf TA} \leq 85^{\circ}{\sf C} \\ \end{array} $			
			-6 -6 -6		6 6 6	% % %	$\label{eq:VFVR} \begin{split} &V{\sf FVR} = 1.024V,  V{\sf DD} \geq 2.5V \\ &V{\sf FVR} = 2.048V,  V{\sf DD} \geq 2.5V \\ &V{\sf FVR} = 4.096V,  V{\sf DD} \geq 4.75V; \\ &-40 \leq TA \leq 125^{\circ}{\sf C} \end{split}$			
D004*	SVDD	VDD Rise Rate to ensure internal Power-on Reset signal	0.05	_	_	V/ms	See Section 3.2 "Power-on Reset (POR)" for details.			

### 23.1 DC Characteristics: PIC16(L)F722A/723A-I/E (Industrial, Extended)

These parameters are characterized but not tested.

† Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

## TABLE 23-4:RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER,<br/>AND BROWN-OUT RESET PARAMETERS

Standard Operating Conditions (unless otherwise stated) Operating Temperature -40°C $\leq$ TA $\leq$ +125°C							
Param No.	Sym.	Characteristic	Min.	Тур†	Max.	Units	Conditions
30	ТмсL	MCLR Pulse Width (low)	2 5			μS μS	VDD = 3.3-5V, -40°C to +85°C VDD = 3.3-5V
31	TWDTLP	Low Power Watchdog Timer Time- out Period (No Prescaler)	10	18	27	ms	Vdd = 3.3V-5V
32	Tost	Oscillator Start-up Timer Period <sup>(1),</sup> (2)	—	1024		Tosc	(Note 3)
33*	TPWRT	Power-up Timer Period, $\overline{PWRTE} = 0$	40	65	140	ms	
34*	Tioz	I/O high-impedance from MCLR Low or Watchdog Timer Reset	—		2.0	μS	
35	Vbor	Brown-out Reset Voltage	2.38 1.80	2.5 1.9	2.73 2.11	V	BORV=2.5V BORV=1.9V
36*	VHYST	Brown-out Reset Hysteresis	0	25	50	mV	-40°C to +85°C
37*	TBORDC	Brown-out Reset DC Response Time	1	3	5 10	μS	$VDD \le VBOR$ , -40°C to +85°C $VDD \le VBOR$

These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- **Note 1:** Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min" values with an external clock applied to the OSC1 pin. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.
  - 2: By design.
  - **3:** Period of the slower clock.
  - 4: To ensure these voltage tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1  $\mu$ F and 0.01  $\mu$ F values in parallel are recommended.

#### FIGURE 23-10: TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS



#### FIGURE 24-28: PIC16LF722A/723A MAXIMUM BASE IPD vs. VDD





















### **PRODUCT IDENTIFICATION SYSTEM**

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO. Device Tap	IXI <sup>(1)</sup> X     XXX       I     I     I   <	Examples: a) PIC16F722A-E/SP 301 = Extended Temp., SPDIP package, QTP pattern #301
Device:	PIC16F722A, PIC16LF722A PIC16F723A, PIC16LF723A	<ul> <li>b) PIC16F722A-I/SO = Industrial Temp., SOIC package</li> </ul>
Tape and Reel Option:	Blank= Standard packaging (tube or tray) T = Tape and Reel <sup>(1)</sup>	
Temperature Range:	I = $-40^{\circ}$ C to+85°C (Industrial) E = $-40^{\circ}$ C to+125°C (Extended)	
Package: Pattern:	MV = UQFN ML = QFN SO = SOIC SP = SPDIP SS = SSOP 3-Digit Pattern Code for QTP (blank otherwise)	Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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