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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XF

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 11x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf722at-i-ml

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

3.6 Time-out Sequence

On power-up, the time-out sequence is as follows: first, PWRT time out is invoked after POR has expired, then OST is activated after the PWRT time out has expired. The total time out will vary based on oscillator configuration and \overrightarrow{PWRTE} bit status. For example, in EC mode with \overrightarrow{PWRTE} bit = 1 (\overrightarrow{PWRT} disabled), there will be no time-out at all. Figure 3-4, Figure 3-5 and Figure 3-6 depict time-out sequences.

Since the time outs occur from the POR pulse, if $\overline{\text{MCLR}}$ is kept low long enough, the time-outs will expire. Then, bringing $\overline{\text{MCLR}}$ high will begin execution immediately (see Figure 3-5). This is useful for testing purposes or to synchronize more than one PIC16(L)F722A/723A device operating in parallel.

Table 3-3 shows the Reset conditions for some special registers.

3.7 Power Control (PCON) Register

The Power Control (PCON) register has two Status bits to indicate what type of Reset that last occurred.

Bit 0 is \overrightarrow{BOR} (Brown-out Reset). \overrightarrow{BOR} is unknown on Power-on Reset. It must then be set by the user and checked on subsequent Resets to see if $\overrightarrow{BOR} = 0$, indicating that a brown-out has occurred. The \overrightarrow{BOR} Status bit is a "don't care" and is not necessarily predictable if the brown-out circuit is disabled (BOREN<1:0> = 00 in the Configuration Word register).

Bit 1 is POR (Power-on Reset). It is a '0' on Power-on Reset and unaffected otherwise. The user must write a '1' to this bit following a Power-on Reset. On a subsequent Reset, if POR is '0', it will indicate that a Power-on Reset has occurred (i.e., VDD may have gone too low).

For more information, see Section 3.5 "Brown-Out Reset (BOR)".

Occillator Configuration	Powe	er-up	Brown-o	Wake-up from	
	PWRTE = 0	PWRTE = 1	PWRTE = 0	PWRTE = 1	Sleep
XT, HS, LP ⁽¹⁾	TPWRT + 1024 • Tosc	1024 • Tosc	TPWRT + 1024 • Tosc	1024 • Tosc	1024 • Tosc
RC, EC, INTOSC	TPWRT	—	TPWRT	_	—

TABLE 3-2: TIME OUT IN VARIOUS SITUATIONS

Note 1: LP mode with T1OSC disabled.

TABLE 3-3: RESET BITS AND THEIR SIGNIFICANCE

POR	BOR	то	PD	Condition	
0	u	1	1	Power-on Reset	
1	0	1	1	Brown-out Reset	
u	u	0	u	WDT Reset	
u	u	0	0	WDT Wake-up	
u	u	u	u	MCLR Reset during normal operation	
u	u	1	0	MCLR Reset during Sleep	

Legend: u = unchanged, x = unknown











Register	Address	Power-on Reset/ Brown-out Reset ⁽¹⁾	MCLR Reset/ WDT Reset	Wake-up from Sleep through Interrupt/Time out
W		XXXX XXXX	uuuu uuuu	uuuu uuuu
INDF	00h/80h/ 100h/180h	XXXX XXXX	xxxx xxxx	սսսս սսսս
TMR0	01h/101h	XXXX XXXX	<u>uuuu</u> uuuu	uuuu uuuu
PCL	02h/82h/ 102h/182h	0000 0000	0000 0000	PC + 1 ⁽³⁾
STATUS	03h/83h/ 103h/183h	0001 1xxx	000q quuu ⁽⁴⁾	uuuq quuu ⁽⁴⁾
FSR	04h/84h/ 104h/184h	XXXX XXXX	uuuu uuuu	սսսս սսսս
PORTA	05h	xxxx xxxx	XXXX XXXX	uuuu uuuu
PORTB	06h	XXXX XXXX	XXXX XXXX	uuuu uuuu
PORTC	07h	xxxx xxxx	XXXX XXXX	uuuu uuuu
PORTE	09h	x	x	u
PCLATH	0Ah/8Ah/ 10Ah/18Ah	0 0000	0 0000	u uuuu
INTCON	0Bh/8Bh/ 10Bh/18Bh	0000 000x	0000 000x	uuuu uuuu ⁽²⁾
PIR1	0Ch	0000 0000	0000 0000	uuuu uuuu ⁽²⁾
PIR2	0Dh	0	0	u
TMR1L	0Eh	XXXX XXXX	uuuu uuuu	uuuu uuuu
TMR1H	0Fh	XXXX XXXX	<u>uuuu</u> uuuu	uuuu uuuu
T1CON	10h	0000 00-0	uuuu uu-u	uuuu uu-u
TMR2	11h	0000 0000	0000 0000	uuuu uuuu
T2CON	12h	-000 0000	-000 0000	-uuu uuuu
SSPBUF	13h	xxxx xxxx	XXXX XXXX	uuuu uuuu
SSPCON	14h	0000 0000	0000 0000	uuuu uuuu
CCPR1L	15h	XXXX XXXX	XXXX XXXX	uuuu uuuu
CCPR1H	16h	XXXX XXXX	XXXX XXXX	uuuu uuuu
CCP1CON	17h	00 0000	00 0000	uu uuuu
RCSTA	18h	0000 000x	0000 000x	uuuu uuuu
TXREG	19h	0000 0000	0000 0000	uuuu uuuu
RCREG	1Ah	0000 0000	0000 0000	uuuu uuuu
CCPR2L	1Bh	XXXX XXXX	XXXX XXXX	uuuu uuuu
CCPR2H	1Ch	XXXX XXXX	XXXX XXXX	uuuu uuuu
CCP2CON	1Dh	00 0000	00 0000	uu uuuu
ADRES	1Eh	XXXX XXXX	uuuu uuuu	uuuu uuuu
ADCON0	1Fh	00 0000	00 0000	uu uuuu
OPTION_REG	81h/181h	1111 1111	1111 1111	սսսս սսսս
TRISA	85h	1111 1111	1111 1111	սսսս սսսս
TRISB	86h	1111 1111	1111 1111	սսսս սսսս
TRISC	87h	1111 1111	1111 1111	սսսս սսսս
TRISE	89h	1	1	u

TABLE 3-4:INITIALIZATION CONDITION FOR REGISTERS

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition.

Note 1: If VDD goes too low, Power-on Reset will be activated and registers will be affected differently.

2: One or more bits in INTCON and/or PIR1 and PIR2 will be affected (to cause wake-up).

3: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

4: See Table 3-5 for Reset value for specific condition.

5: If Reset was due to brown-out, then bit 0 = 0. All other Resets will cause bit 0 = u.

5.0 LOW DROPOUT (LDO) VOLTAGE REGULATOR

The PIC16F722A/723A devices differ from the PIC16LF722A/723A devices due to an internal Low Dropout (LDO) voltage regulator. The PIC16F722A/723A devices contain an internal LDO, while the PIC16LF722A/723A ones do not.

The lithography of the die allows a maximum operating voltage of 3.6V on the internal digital logic. In order to continue to support 5.0V designs, a LDO voltage regulator is integrated on the die. The LDO voltage regulator allows for the internal digital logic to operate at 3.2V, while I/O's operate at 5.0V (VDD).

The LDO voltage regulator requires an external bypass capacitor for stability. One of three pins, denoted as VCAP, can be configured for the external bypass capacitor. It is recommended that the capacitor be a ceramic cap between 0.1 to $1.0 \,\mu$ F. The VCAP pin is not intended to supply power to external loads. An external voltage regulator should be used if this functionality is required. In addition, external devices should not supply power to the VCAP pin.

On power-up, the external capacitor will look like a large load on the LDO voltage regulator. To prevent erroneous operation, the device is held in Reset while a constant current source charges the external capacitor. After the cap is fully charged, the device is released from Reset. For more information, refer to **Section 23.0 "Electrical Specifications"**.

See Configuration Word 2 register (Register 8-2) for VCAP enable bits.

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
bit 7							bit 0
Legend:							
R = Readable b	oit	W = Writable	bit	U = Unimpler	mented bit, read	l as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown

REGISTER 6-5: PORTB: PORTB REGISTER

bit 7-0 RB<7:0>: PORTB I/O Pin bits

1 = Port pin is > VIH

0 = Port pin is < VIL

REGISTER 6-6: TRISB: PORTB TRI-STATE REGISTER

| R/W-1 |
|--------|--------|--------|--------|--------|--------|--------|--------|
| TRISB7 | TRISB6 | TRISB5 | TRISB4 | TRISB3 | TRISB2 | TRISB1 | TRISB0 |
| bit 7 | | | | | | | bit 0 |

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0

—

TRISB<7:0>: PORTB Tri-State Control bits

1 = PORTB pin configured as an input (tri-stated)

0 = PORTB pin configured as an output

REGISTER 6-7: WPUB: WEAK PULL-UP PORTB REGISTER

| R/W-1 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| WPUB7 | WPUB6 | WPUB5 | WPUB4 | WPUB3 | WPUB2 | WPUB1 | WPUB0 |
| bit 7 | | | | | | | bit 0 |

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **WPUB<7:0>**: Weak Pull-up Register bits

1 = Pull up enabled

0 = Pull up disabled

Note 1: Global RBPU bit of the OPTION register must be cleared for individual pull ups to be enabled.

2: The weak pull-up device is automatically disabled if the pin is in configured as an output.

PIC16(L)F722A/723A

FIGURE 6-12: BLOCK DIAGRAM OF RB7



12.6 Timer1 Gate

Timer1 can be configured to count freely or the count can be enabled and disabled using Timer1 gate circuitry. This is also referred to as Timer1 Gate Count Enable.

Timer1 gate can also be driven by multiple selectable sources.

12.6.1 TIMER1 GATE COUNT ENABLE

The Timer1 gate is enabled by setting the TMR1GE bit of the T1GCON register. The polarity of the Timer1 gate is configured using the T1GPOL bit of the T1GCON register.

When Timer1 Gate (T1G) input is active, Timer1 will increment on the rising edge of the Timer1 clock source. When Timer1 gate input is inactive, no incrementing will occur and Timer1 will hold the current count. See Figure 12-4 for timing details.

TABLE 12-3: TIMER1 GATE ENABLE SELECTIONS

T1CLK	T1GPOL	T1G	Timer1 Operation
\uparrow	0	0	Counts
\uparrow	0	1	Holds Count
\uparrow	1	0	Holds Count
\uparrow	1	1	Counts

12.6.2 TIMER1 GATE SOURCE SELECTION

The Timer1 gate source can be selected from one of four different sources. Source selection is controlled by the T1GSS bits of the T1GCON register. The polarity for each available source is also selectable. Polarity selection is controlled by the T1GPOL bit of the T1GCON register.

TABLE 12-4: TIMER1 GATE SOURCES

T1GSS	Timer1 Gate Source
00	Timer1 Gate Pin
01	Overflow of Timer0 (TMR0 increments from FFh to 00h)
10	Timer2 match PR2 (TMR2 increments to match PR2)
11	Count Enabled by WDT Overflow (Watchdog Time-out interval expired)

12.6.2.1 T1G Pin Gate Operation

The T1G pin is one source for Timer1 gate control. It can be used to supply an external source to the Timer1 gate circuitry.

12.6.2.2 Timer0 Overflow Gate Operation

When Timer0 increments from FFh to 00h, a low-tohigh pulse will automatically be generated and internally supplied to the Timer1 gate circuitry.

12.6.2.3 Timer2 Match Gate Operation

The TMR2 register will increment until it matches the value in the PR2 register. On the very next increment cycle, TMR2 will be reset to 00h. When this Reset occurs, a low-to-high pulse will automatically be generated and internally supplied to the Timer1 gate circuitry.

12.6.2.4 Watchdog Overflow Gate Operation

The Watchdog Timer oscillator, prescaler and counter will be automatically turned on when TMR1GE = 1 and T1GSS selects the WDT as a gate source for Timer1 (T1GSS = 11). TMR1ON does not factor into the oscillator, prescaler and counter enable. See Table .

The PSA and PS bits of the OPTION register still control what time-out interval is selected. Changing the prescaler during operation may result in a spurious capture.

Enabling the Watchdog Timer oscillator does not automatically enable a Watchdog Reset or Wake-up from Sleep upon counter overflow.

Note:	When using the WDT as a gate source for
	Timer1, operations that clear the Watchdog
	Timer (CLRWDT, SLEEP instructions) will
	affect the time interval being measured for
	capacitive sensing. This includes waking
	from Sleep. All other interrupts that might
	wake the device from Sleep should be
	disabled to prevent them from disturbing
	the measurement period.

As the gate signal coming from the WDT counter will generate different pulse widths depending on if the WDT is enabled, when the CLRWDT instruction is executed, and so on, Toggle mode must be used. A specific sequence is required to put the device into the correct state to capture the next WDT counter interval.

15.1 Capture Mode

In Capture mode, CCPRxH:CCPRxL captures the 16-bit value of the TMR1 register when an event occurs on pin CCPx. An event is defined as one of the following and is configured by the CCPxM<3:0> bits of the CCPxCON register:

- · Every falling edge
- Every rising edge
- Every 4th rising edge
- Every 16th rising edge

When a capture is made, the Interrupt Request Flag bit CCPxIF of the PIRx register is set. The interrupt flag must be cleared in software. If another capture occurs before the value in the CCPRxH, CCPRxL register pair is read, the old captured value is overwritten by the new captured value (refer to Figure 15-1).

15.1.1 CCPx PIN CONFIGURATION

In Capture mode, the CCPx pin should be configured as an input by setting the associated TRIS control bit.

Either RC1 or RB3 can be selected as the CCP2 pin. Refer to **Section 6.1** "Alternate Pin Function" for more information.

Note: If the CCPx pin is configured as an output, a write to the port can cause a capture condition.

FIGURE 15-1: CAPTURE MODE OPERATION BLOCK DIAGRAM



15.1.2 TIMER1 MODE SELECTION

Timer1 must be running in Timer mode or Synchronized Counter mode for the CCP module to use the capture feature. In Asynchronous Counter mode or when Timer1 is clocked at Fosc, the capture operation may not work.

15.1.3 SOFTWARE INTERRUPT

When the Capture mode is changed, a false capture interrupt may be generated. The user should keep the CCPxIE interrupt enable bit of the PIEx register clear to avoid false interrupts. Additionally, the user should clear the CCPxIF interrupt flag bit of the PIRx register following any change in operating mode.

Note: Clocking Timer1 from the system clock (Fosc) should not be used in Capture mode. In order for Capture mode to recognize the trigger event on the CCPx pin, Timer1 must be clocked from the instruction clock (Fosc/4) or from an external clock source.

15.1.4 CCP PRESCALER

There are four prescaler settings specified by the CCPxM<3:0> bits of the CCPxCON register. Whenever the CCP module is turned off, or the CCP module is not in Capture mode, the prescaler counter is cleared. Any Reset will clear the prescaler counter.

Switching from one capture prescaler to another does not clear the prescaler and may generate a false interrupt. To avoid this unexpected operation, turn the module off by clearing the CCPxCON register before changing the prescaler (refer to Example 15-1).

EXAMPLE 15-1: CHANGING BETWEEN CAPTURE PRESCALERS

BANKSEI	CCP1CON	;Set Bank bits to point
		;to CCP1CON
CLRF	CCP1CON	;Turn CCP module off
MOVLW	NEW_CAPT_PS	G;Load the W reg with
		; the new prescaler
		; move value and CCP ON
MOVWF	CCP1CON	;Load CCP1CON with this
		; value

15.1.5 CAPTURE DURING SLEEP

Capture mode depends upon the Timer1 module for proper operation. There are two options for driving the Timer1 module in Capture mode. It can be driven by the instruction clock (Fosc/4), or by an external clock source.

If Timer1 is clocked by Fosc/4, then Timer1 will not increment during Sleep. When the device wakes from Sleep, Timer1 will continue from its previous state.

If Timer1 is clocked by an external clock source, then Capture mode will operate as defined in **Section 15.1** "**Capture Mode**".

16.3 AUSART Synchronous Mode

Synchronous serial communications are typically used in systems with a single master and one or more slaves. The master device contains the necessary circuitry for baud rate generation and supplies the clock for all devices in the system. Slave devices can take advantage of the master clock by eliminating the internal clock generation circuitry.

There are two signal lines in Synchronous mode: a bidirectional data line and a clock line. Slaves use the external clock supplied by the master to shift the serial data into and out of their respective receive and transmit shift registers. Since the data line is bidirectional, synchronous operation is half-duplex only. Half-duplex refers to the fact that master and slave devices can receive and transmit data but not both simultaneously. The AUSART can operate as either a master or slave device.

Start and Stop bits are not used in synchronous transmissions.

16.3.1 SYNCHRONOUS MASTER MODE

The following bits are used to configure the AUSART for Synchronous Master operation:

- SYNC = 1
- CSRC = 1
- SREN = 0 (for transmit); SREN = 1 (for receive)
- CREN = 0 (for transmit); CREN = 1 (for receive)
- SPEN = 1

Setting the SYNC bit of the TXSTA register configures the device for synchronous operation. Setting the CSRC bit of the TXSTA register configures the device as a master. Clearing the SREN and CREN bits of the RCSTA register ensures that the device is in the Transmit mode, otherwise the device will be configured to receive. Setting the SPEN bit of the RCSTA register enables the AUSART.

16.3.1.1 Master Clock

Synchronous data transfers use a separate clock line, which is synchronous with the data. A device configured as a master transmits the clock on the TX/ CK line. The TX/CK pin output driver is automatically enabled when the AUSART is configured for synchronous transmit or receive operation. Serial data bits change on the leading edge to ensure they are valid at the trailing edge of each clock. One clock cycle is generated for each data bit. Only as many clock cycles are generated as there are data bits.

16.3.1.2 Synchronous Master Transmission

Data is transferred out of the device on the RX/DT pin. The RX/DT and TX/CK pin output drivers are automatically enabled when the AUSART is configured for synchronous master transmit operation.

A transmission is initiated by writing a character to the TXREG register. If the TSR still contains all or part of a previous character, the new character data is held in the TXREG until the last bit of the previous character has been transmitted. If this is the first character, or the previous character has been completely flushed from the TSR, the data in the TXREG is immediately transferred to the TSR. The transmission of the character commences immediately following the transfer of the data to the TSR from the TXREG.

Each data bit changes on the leading edge of the master clock and remains valid until the subsequent leading clock edge.

Note: The TSR register is not mapped in data memory, so it is not available to the user.

16.3.1.3 Synchronous Master Transmission Setup:

- Initialize the SPBRG register and the BRGH bit to achieve the desired baud rate (refer to Section 16.2 "AUSART Baud Rate Generator (BRG)").
- 2. Enable the synchronous master serial port by setting bits SYNC, SPEN and CSRC.
- 3. Disable Receive mode by clearing bits SREN and CREN.
- 4. Enable Transmit mode by setting the TXEN bit.
- 5. If 9-bit transmission is desired, set the TX9 bit.
- 6. If interrupts are desired, set the TXIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
- 7. If 9-bit transmission is selected, the ninth bit should be loaded in the TX9D bit.
- 8. Start transmission by loading data to the TXREG register.

REGISTER 1	7-2: SSPS1	TAT: SYNC SI	ERIAL POR	RT STATUS R	EGISTER (S	PI MODE)	
R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0	R-0
SMP	CKE	D/A	Р	S	R/W	UA	BF
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimplei	mented bit, rea	d as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	nown
bit 7 bit 6	SMP: SPI Dat <u>SPI Master m</u> 1 = Input data 0 = Input data <u>SPI Slave mo</u> SMP must be CKE : SPI Clo <u>SPI mode, CH</u> 1 = Data stab <u>SPI mode, CH</u> 1 = Data stab 0 = Data stab	ta Input Sample <u>ode:</u> a sampled at er a sampled at minde: cleared when the Edge Select $\underline{\langle P = 0:}$ le on rising edg $\underline{\langle P = 1:}$ le on falling edg le on rising edg	e Phase bit ad of data out iddle of data SPI is used in t bit ge of SCK ge of SCK ge of SCK ge of SCK	put time output time n Slave mode			
bit 5	D/A: Data/Ad Used in I ² C m	dress bit node only.					
bit 4	P: Stop bit Used in I ² C m	node only.					
bit 3	S: Start bit Used in I ² C m	node only.					
bit 2	R/W: Read/W Used in I ² C m	Information	n bit				
bit 1	UA: Update A Used in I ² C m	Address bit node only.					
bit 0	BF : Buffer Fu 1 = Receive c 0 = Receive r	Il Status bit complete, SSPE not complete, S	BUF is full SPBUF is en	npty			

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REGISTER 18-1: PMCON1: PROGRAM MEMORY CONTROL 1 REGISTER

R-1	U-0	U-0	U-0	U-0	U-0	U-0	R/S-0
Reserved	—	—	—	—	—	—	RD
bit 7							bit 0

Legend:		S = Setable bit, cleared in hardware			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit <i>r</i> Reserved. Read as 1. Maintain this bit set.

bit 6-1 Unimplemented: Read as '0'

bit 0 RD: Read Control bit

 1 = Initiates an program memory read (The RD is cleared in hardware; the RD bit can only be set (not cleared) in software).

0 = Does not initiate a program memory read

REGISTER 18-2: PMDATH: PROGRAM MEMORY DATA HIGH REGISTER

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	PMD13	PMD12	PMD11	PMD10	PMD9	PMD8
bit 7							bit 0
Legend:							

Legenu.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 Unimplemented: Read as '0'

bit 5-0 **PMD<13:8>:** The value of the program memory word pointed to by PMADRH and PMADRL after a Program Memory Read command.

REGISTER 18-3: PMDATL: PROGRAM MEMORY DATA LOW REGISTER

| R/W-x |
|-------|-------|-------|-------|-------|-------|-------|-------|
| PMD7 | PMD6 | PMD5 | PMD4 | PMD3 | PMD2 | PMD1 | PMD0 |
| bit 7 | | | | | | | bit 0 |

Legend:						
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'				
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			

bit 7-0 **PMD<7:0>:** The value of the program memory word pointed to by PMADRH and PMADRL after a Program Memory Read command.

22.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

22.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

22.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a highspeed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

22.9 PICkit 3 In-Circuit Debugger/ Programmer

The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a fullspeed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming[™] (ICSP[™]).

22.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.

23.4 DC Characteristics: PIC16(L)F722A/723A-I/E (Continued)

	DC C	HARACTERISTICS	$\begin{array}{l} \mbox{Standard Operating Conditions (unless otherwise stated)} \\ \mbox{Operating temperature } -40^{\circ}\mbox{C} \leq T\mbox{Ta} \leq +85^{\circ}\mbox{C for industrial} \\ -40^{\circ}\mbox{C} \leq T\mbox{A} \leq +125^{\circ}\mbox{C for extended} \end{array}$					
Param No.	Sym.	Characteristic Min. Typ† Max. Units		Conditions				
D130	Eр	Cell Endurance	100	1k	—	E/W	Temperature during programming: $10^{\circ}C \le TA \le 40^{\circ}C$	
D131		VDD for Read	Vmin	—	—	V		
		Voltage on MCLR/VPP during Erase/Program	8.0	—	9.0	V	Temperature during programming: $10^{\circ}C \le TA \le 40^{\circ}C$	
		VDD for Bulk Erase	2.7	3	—	V	Temperature during programming: $10^{\circ}C \le TA \le 40^{\circ}C$	
D132	VPEW	VDD for Write or Row Erase	2.7	-	—	V	VMIN = Minimum operating voltage VMAX = Maximum operating voltage	
	IPPPGM	Current on MCLR/VPP during Erase/Write	—	_	5.0	mA	Temperature during programming: $10^{\circ}C \le TA \le 40^{\circ}C$	
	IDDPGM	Current on VDD during Erase/ Write	—		5.0	mA	Temperature during programming: $10^{\circ}C \le TA \le 40^{\circ}C$	
D133	TPEW	Erase/Write cycle time	—		2.8	ms	Temperature during programming: $10^{\circ}C \le TA \le 40^{\circ}C$	
D134	TRETD	Characteristic Retention	40	—	—	Year	Provided no other specifications are violated	
		VCAP Capacitor Charging						
D135		Charging current	_	200	_	μA		
D135A		Source/sink capability when charging complete	_	0.0	_	mA		

Legend: TBD = To Be Determined

These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in RC mode.

2: Negative current is defined as current sourced by the pin.

3: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

4: Including OSC2 in CLKOUT mode.

23.7 AC Characteristics: PIC16F722A/723A-I/E



FIGURE 23-3: CLOCK TIMING





Param. No.	Symbol	Characteristic		Min.	Тур†	Max.	Units	Conditions
CS01	ISRC	Current Source	High	—	-5.8	-6	μΑ	
			Medium	—	-1.1	-3.2	μΑ	-40, -85°C
			Low	—	-0.2	-0.9	μΑ	
CS02	Isnk	Current Sink	High	—	6.6	6	μΑ	
			Medium	_	1.3	3.2	μΑ	-40, -85°C
			Low	—	0.24	0.9	μΑ	
CS03	VCHYST	Cap Hysteresis	High	—	525		mV	
			Medium	—	375		mV	VCTH-VCTL
			Low	_	280		mV	

TABLE 23-14: CAP SENSE OSCILLATOR SPECIFICATIONS

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.



FIGURE 23-22: CAP SENSE OSCILLATOR



FIGURE 24-34: PIC16LF722A/723A BOR IPD vs. VDD











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25.2 Package Details

The following sections give the technical details of the packages.

28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units					
Dimension	n Limits	MIN	NOM	MAX		
Number of Pins	Ν		28			
Pitch	е		.100 BSC			
Top to Seating Plane	Α	-	-	.200		
Molded Package Thickness	A2	.120	.135	.150		
Base to Seating Plane	A1	.015	_	-		
Shoulder to Shoulder Width	Е	.290	.310	.335		
Molded Package Width	E1	.240	.285	.295		
Overall Length	D	1.345	1.365	1.400		
Tip to Seating Plane	L	.110	.130	.150		
Lead Thickness	С	.008	.010	.015		
Upper Lead Width	b1	.040	.050	.070		
Lower Lead Width	b	.014	.018	.022		
Overall Row Spacing §	eB	-	-	.430		

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. § Significant Characteristic.
- 3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- 4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-070B

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO. Device Tap	IXI ⁽¹⁾ X XXX I I I <	Examples: a) PIC16F722A-E/SP 301 = Extended Temp., SPDIP package, QTP pattern #301
Device:	PIC16F722A, PIC16LF722A PIC16F723A, PIC16LF723A	 b) PIC16F722A-I/SO = Industrial Temp., SOIC package
Tape and Reel Option:	Blank= Standard packaging (tube or tray) T = Tape and Reel ⁽¹⁾	
Temperature Range:	I = -40° C to+85°C (Industrial) E = -40° C to+125°C (Extended)	
Package: Pattern:	MV = UQFN ML = QFN SO = SOIC SP = SPDIP SS = SSOP 3-Digit Pattern Code for QTP (blank otherwise)	Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.