



Welcome to E-XFL.COM

#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I <sup>2</sup> C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 11x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf723a-e-ss

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

## PIC16(L)F72X Family Types

Device	Data Sheet Index	Program Memory Flash (words)	Data SRAM (bytes)	High-Endurance Flash Memory (bytes)	ا/O's <sup>(2)</sup>	8-bit ADC (ch)	CapSense (ch)	Timers (8/16-bit)	AUSART	SSP (I <sup>2</sup> C/SPI)	CCP	Debug <sup>(1)</sup>	XLP
PIC16(L)F707	(1)	8192	363	0	36	14	32	4/2	1	1	2	Ι	Y
PIC16(L)F720	(2)	2048	128	128	18	12	_	2/1	1	1	1	I	Y
PIC16(L)F721	(2)	4096	256	128	18	12		2/1	1	1	1	Ι	Y
PIC16(L)F722	(4)	2048	128	0	25	11	8	2/1	1	1	2	I	Y
PIC16(L)F722A	(3)	2048	128	0	25	11	8	2/1	1	1	2	Ι	Y
PIC16(L)F723	(4)	4096	192	0	25	11	8	2/1	1	1	2	I	Y
PIC16(L)F723A	(3)	4096	192	0	25	11	8	2/1	1	1	2	Ι	Y
PIC16(L)F724	(4)	4096	192	0	36	14	16	2/1	1	1	2	Ι	Y
PIC16(L)F726	(4)	8192	368	0	25	11	8	2/1	1	1	2	I	Y
PIC16(L)F727	(4)	8192	368	0	36	14	16	2/1	1	1	2	Ι	Y

**Note 1:** I - Debugging, Integrated on Chip; H - Debugging, Requires Debug Header.

2: One pin is input-only.

Data Sheet Index: (Unshaded devices are described in this document.)

- 1: DS41418 PIC16(L)F707 Data Sheet, 40/44-Pin Flash, 8-bit Microcontrollers
- 2: DS41430 PIC16(L)F720/721 Data Sheet, 20-Pin Flash, 8-bit Microcontrollers
- 3: DS41417 PIC16(L)F722A/723A Data Sheet, 28-Pin Flash, 8-bit Microcontrollers
- 4: DS41341 PIC16(L)F72X Data Sheet, 28/40/44-Pin Flash, 8-bit Microcontrollers

## 2.2.2.1 STATUS Register

The STATUS register, shown in Register 2-1, contains:

- the arithmetic status of the ALU
- · the Reset status
- the bank select bits for data memory (SRAM)

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the TO and PD bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, CLRF STATUS will clear the upper three bits and set the Z bit. This leaves the STATUS register as '000u uluu' (where u = unchanged).

It is recommended, therefore, that only BCF, BSF, SWAPF and MOVWF instructions are used to alter the STATUS register, because these instructions do not affect any Status bits. For other instructions not affecting any Status bits (Refer to Section 21.0 "Instruction Set Summary").

Note 1:	The C and DC bits operate as Borrow
	and Digit Borrow out bits, respectively, in
	subtraction.

<b>REGISTER 2</b>	-1: STATU	IS: STATUS I	REGISTER							
R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x			
IRP	RP1	RP0	TO	PD	Z	DC <sup>(1)</sup>	C <sup>(1)</sup>			
bit 7						·	bit 0			
Legend:										
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	d as '0'				
-n = Value at P	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	nown			
bit 7	IRP: Register 1 = Bank 2, 3 0 = Bank 0, 1	Bank Select b (100h-1FFh) (00h-FFh)	it (used for inc	direct addressi	ng)					
bit 6-5	<b>RP&lt;1:0&gt;:</b> Reg 00 = Bank 0 ( 01 = Bank 1 ( 10 = Bank 2 ( 11 = Bank 3 (	gister Bank Se (00h-7Fh) (80h-FFh) (100h-17Fh) (180h-1FFh)	ect bits (used	for direct add	ressing)					
bit 4	<b>TO:</b> Time-out 1 = After pow 0 = A WDT tir	bit er-up, CLRWDT me-out occurre	instruction or d	SLEEP instruc	tion					
bit 3	<b>PD:</b> Power-do 1 = After pow 0 = By execut	PD: Power-down bit 1 = After power-up or by the CLRWDT instruction 0 = By execution of the SLEEP instruction								
bit 2	<b>Z:</b> Zero bit 1 = The resul 0 = The resul	t of an arithmet t of an arithmet	ic or logic ope ic or logic ope	eration is zero eration is not ze	ero					
bit 1	<b>DC:</b> Digit Car	ry/Digit Borrow ut from the 4th	bit (ADDWF, A low-order bit o	DDLW, SUBLW,	, SUBWF instruc	tions) <sup>(1)</sup>				

- 0 = No carry-out from the 4th low-order bit of the result
- bit 0 C: Carry/Borrow bit<sup>(1)</sup> (ADDWF, ADDLW, SUBLW, SUBWF instructions)<sup>(1)</sup> 1 = A carry-out from the Most Significant bit of the result occurred
  - 0 = No carry-out from the Most Significant bit of the result occurred
- **Note 1:** For Borrow, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (RRF, RLF) instructions, this bit is loaded with either the high-order or low-order bit of the source register.

## 2.2.2.3 PCON Register

The Power Control (PCON) register contains flag bits (refer to Table 3-2) to differentiate between a:

- Power-on Reset (POR)
- Brown-out Reset (BOR)
- Watchdog Timer Reset (WDT)
- External MCLR Reset

The PCON register also controls the software enable of the BOR.

The PCON register bits are shown in Register 2-3.

## REGISTER 2-3: PCON: POWER CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-q	R/W-q
—	—	—	—	—	—	POR	BOR
bit 7							bit 0

Legend:						
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'						
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			
q = Value depends on c	ondition					

hit 7-2	Unimplemented: Read as '0'
bit 1	POR: Power-on Reset Status bit
	<ul> <li>1 = No Power-on Reset occurred</li> <li>0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)</li> </ul>
bit 0	<ul> <li>BOR: Brown-out Reset Status bit</li> <li>1 = No Brown-out Reset occurred</li> <li>0 = A Brown-out Reset occurred (must be set in software after a Power-on Reset or Brown-out Reset occurs)</li> </ul>

**Note 1:** Set BOREN<1:0> = 01 in the Configuration Word register for this bit to control the  $\overline{\text{BOR}}$ .

#### 4.5.1 INTCON REGISTER

The INTCON register is a readable and writable register, which contains the various enable and flag bits for TMR0 register overflow, PORTB change and external RB0/INT/SEG0 pin interrupts.

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

#### REGISTER 4-1: INTCON: INTERRUPT CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE	PEIE	TOIE	INTE	RBIE <sup>(1)</sup>	T0IF <sup>(2)</sup>	INTF	RBIF
bit 7							bit 0

Legend:				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 7	GIE: Global Interrupt Enable bit
	<ul><li>1 = Enables all unmasked interrupts</li><li>0 = Disables all interrupts</li></ul>
bit 6	<b>PEIE:</b> Peripheral Interrupt Enable bit 1 = Enables all unmasked peripheral interrupts 0 = Disables all peripheral interrupts
bit 5	<b>TolE:</b> Timer0 Overflow Interrupt Enable bit 1 = Enables the Timer0 interrupt 0 = Disables the Timer0 interrupt
bit 4	INTE: RB0/INT External Interrupt Enable bit 1 = Enables the RB0/INT external interrupt 0 = Disables the RB0/INT external interrupt
bit 3	<b>RBIE:</b> PORTB Change Interrupt Enable bit <sup>(1)</sup> 1 = Enables the PORTB change interrupt 0 = Disables the PORTB change interrupt
bit 2	<b>T0IF:</b> Timer0 Overflow Interrupt Flag bit <sup>(2)</sup> 1 = TMR0 register has overflowed (must be cleared in software) 0 = TMR0 register did not overflow
bit 1	INTF: RB0/INT External Interrupt Flag bit 1 = The RB0/INT external interrupt occurred (must be cleared in software) 0 = The RB0/INT external interrupt did not occur
bit 0	<ul> <li><b>RBIF:</b> PORTB Change Interrupt Flag bit</li> <li>1 = When at least one of the PORTB general purpose I/O pins changed state (must be cleared in software)</li> </ul>
	0 = None of the PORTB general purpose I/O pins have changed state
Note 1.	The expression hits in the IOCD register must also be act

- **Note 1:** The appropriate bits in the IOCB register must also be set.
  - 2: T0IF bit is set when Timer0 rolls over. Timer0 is unchanged on Reset and should be initialized before clearing T0IF bit.

#### 4.5.2 PIE1 REGISTER

The PIE1 register contains the interrupt enable bits, as shown in Register 4-2.

**Note:** Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimplei	mented bit, read	l as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	nown
bit 7	<b>TMR1GIE:</b> Til	mer1 Gate Inte	rrupt Enable	bit	at .		
	0 = Disable th	ne Timer1 gate	acquisition co	omplete interru	pt		
bit 6	ADIE: A/D Co	onverter (ADC)	Interrupt Ena	able bit			
	1 = Enables t 0 = Disables t	he ADC interru	pt 				
bit 5	RCIE: USAR	T Receive Inter	rupt Enable b	bit			
	1 = Enables t 0 = Disables t	he USART rec the USART rec	eive interrupt eive interrupt	t			
bit 4	TXIE: USART	Transmit Inter	rupt Enable b	oit			
	1 = Enables t 0 = Disables t	he USART tran the USART tran	nsmit interrupt nsmit interrup	t ot			
bit 3	SSPIE: Synch	hronous Serial	Port (SSP) In	nterrupt Enable	bit		
	1 = Enables t 0 = Disables t	he SSP interru the SSP interru	pt ipt				
bit 2	CCP1IE: CCF	P1 Interrupt En	able bit				
	1 = Enables t 0 = Disables t	he CCP1 interr the CCP1 inter	rupt rupt				
bit 1	TMR2IE: TM	R2 to PR2 Mate	ch Interrupt E	nable bit			
	1 = Enables t 0 = Disables t	he Timer2 to P the Timer2 to F	R2 match inte R2 match int	errupt errupt			
bit 0	TMR1IE: Time	er1 Overflow Ir	nterrupt Enabl	le bit			
	1 = Enables t 0 = Disables t	he Timer1 ovei the Timer1 ove	flow interrupt rflow interrup	t t			

#### REGISTER 4-2: PIE1: PERIPHERAL INTERRUPT ENABLE REGISTER 1

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x			
RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0			
bit 7							bit 0			
Legend:										
R = Readable b	R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'			l as '0'						
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cleared x = Bit is unknown			nown			

#### REGISTER 6-5: PORTB: PORTB REGISTER

bit 7-0 RB<7:0>: PORTB I/O Pin bits

1 = Port pin is > VIH

0 = Port pin is < VIL

#### REGISTER 6-6: TRISB: PORTB TRI-STATE REGISTER

| R/W-1  |
|--------|--------|--------|--------|--------|--------|--------|--------|
| TRISB7 | TRISB6 | TRISB5 | TRISB4 | TRISB3 | TRISB2 | TRISB1 | TRISB0 |
| bit 7  |        |        |        |        |        |        | bit 0  |

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0

**—** 

TRISB<7:0>: PORTB Tri-State Control bits

1 = PORTB pin configured as an input (tri-stated)

0 = PORTB pin configured as an output

#### REGISTER 6-7: WPUB: WEAK PULL-UP PORTB REGISTER

| R/W-1 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| WPUB7 | WPUB6 | WPUB5 | WPUB4 | WPUB3 | WPUB2 | WPUB1 | WPUB0 |
| bit 7 |       |       |       |       |       |       | bit 0 |

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **WPUB<7:0>**: Weak Pull-up Register bits

1 = Pull up enabled

0 = Pull up disabled

**Note 1:** Global RBPU bit of the OPTION register must be cleared for individual pull ups to be enabled.

2: The weak pull-up device is automatically disabled if the pin is in configured as an output.

# PIC16(L)F722A/723A



## 7.6.4 EXTERNAL RC MODES

The external Resistor-Capacitor (RC) modes support the use of an external RC circuit. This allows the designer maximum flexibility in frequency choice while keeping costs to a minimum when clock accuracy is not required. There are two modes: RC and RCIO.

In RC mode, the RC circuit connects to OSC1. OSC2/ CLKOUT outputs the RC oscillator frequency divided by 4. This signal may be used to provide a clock for external circuitry, synchronization, calibration, test or other application requirements. Figure 7-5 shows the external RC mode connections.



In RCIO mode, the RC circuit is connected to OSC1. OSC2 becomes an additional general purpose I/O pin.

The RC oscillator frequency is a function of the supply voltage, the resistor (REXT) and capacitor (CEXT) values and the operating temperature. Other factors affecting the oscillator frequency are:

- threshold voltage variation
- component tolerances
- · packaging variations in capacitance

The user also needs to take into account variation due to tolerance of external RC components used.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
OSCCON	—	—	IRCF1	IRCF0	ICSL	ICSS	_	—	73
OSCTUNE	—	—	TUN5	TUN4	TUN3	TUN2	TUN1	TUN0	74

#### TABLE 7-1: SUMMARY OF REGISTERS ASSOCIATED WITH CLOCK SOURCES

**Legend:** x = unknown, u = unchanged, – = unimplemented locations read as '0'. Shaded cells are not used by oscillators.

Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
CONFIG1	13:8	_	_	DEBUG	PLLEN	_	BORV	BOREN1	BOREN0	77
	7:0		CP	MCLRE	PWRTE	WDTE		FOSC<2:0>		- 77

**Legend:** — = unimplemented location, read as '0'. Shaded cells are not used by clock sources.

# 9.1 ADC Configuration

When configuring and using the ADC the following functions must be considered:

- Port configuration
- Channel selection
- ADC voltage reference selection
- ADC conversion clock source
- Interrupt control
- Results formatting

#### 9.1.1 PORT CONFIGURATION

The ADC can be used to convert both analog and digital signals. When converting analog signals, the I/O pin should be configured for analog by setting the associated TRIS and ANSEL bits. Refer to **Section 6.0 "I/O Ports"** for more information.

Note:	Analog voltages on any pin that is defined										
	as a digital input may cause the input										
	buffer to conduct excess current.										

#### 9.1.2 CHANNEL SELECTION

The CHS bits of the ADCON0 register determine which channel is connected to the sample and hold circuit.

When changing channels, a delay is required before starting the next conversion. Refer to **Section 9.2 "ADC Operation"** for more information.

## 9.1.3 ADC VOLTAGE REFERENCE

The ADREF bits of the ADCON1 register provides control of the positive voltage reference. The positive voltage reference can be either VDD, an external voltage source or the internal Fixed Voltage Reference. The negative voltage reference is always connected to the ground reference. See **Section 10.0** "**Fixed Voltage Reference**" for more details.

#### 9.1.4 CONVERSION CLOCK

The source of the conversion clock is software selectable via the ADCS bits of the ADCON1 register. There are seven possible clock options:

- Fosc/2
- Fosc/4
- Fosc/8
- Fosc/16
- Fosc/32
- Fosc/64
- FRC (dedicated internal oscillator)

The time to complete one bit conversion is defined as TAD. One full 8-bit conversion requires 10 TAD periods as shown in Figure 9-2.

For correct conversion, the appropriate TAD specification must be met. Refer to the A/D conversion requirements in **Section 23.0 "Electrical Specifications"** for more information. Table 9-1 gives examples of appropriate ADC clock selections.

Note: Unless using the FRC, any changes in the system clock frequency will change the ADC clock frequency, which may adversely affect the ADC result.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ADCON0	—	—	CHS3	CHS2	CHS1	CHS0	GO/ DONE	ADON	85
ADCON1	—	ADCS2	ADCS1	ADCS0	—	—	ADREF1	ADREF0	86
ANSELA	—	—	ANSA5	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0	44
ANSELB	—	—	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	53
ADRES			A/[	D Result Re	egister Byte				86
CCP2CON	—	—	DC2B1	DC2B0	CCP2M3	CCP2M2	CCP2M1	CCP2M0	115
FVRCON	FVRRDY	FVREN	_	—	—	—	ADFVR1	ADFVR0	90
INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	36
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	37
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	39
TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	43
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	52

## TABLE 9-2: SUMMARY OF ASSOCIATED ADC REGISTERS

**Legend:** x = unknown, u = unchanged, - = unimplemented read as '0', <math>q = value depends on condition. Shaded cells are not used for ADC module.

#### 11.1.3 SOFTWARE PROGRAMMABLE PRESCALER

A single software programmable prescaler is available for use with either Timer0 or the Watchdog Timer (WDT), but not both simultaneously. The prescaler assignment is controlled by the PSA bit of the OPTION register. To assign the prescaler to Timer0, the PSA bit must be cleared to a '0'.

There are eight prescaler options for the Timer0 module ranging from 1:2 to 1:256. The pres ca le values are selectable via the PS<2:0> bits of the OPTION register. In order to have a 1:1 prescaler value for the Timer0 module, the prescaler must be assigned to the WDT module.

The prescaler is not readable or writable. When assigned to the Timer0 module, all instructions writing to the TMR0 register will clear the prescaler.

Note:	When the prescaler is assigned to WDT, a
	CLRWDT instruction will clear the prescaler
	along with the WDT.

#### 11.1.4 TIMER0 INTERRUPT

Timer0 will generate an interrupt when the TMR0 register overflows from PH to 00h. The T0IF interrupt flag bit of the INTCON register is set every time the TMR0 register overflows, regardless of whether or not the Timer0 interrupt is enabled. The T0IF bit can only be cleared in software. The Timer0 interrupt enable is the T0IE bit of the INTCON register.

Note:	The Timer0 interrupt cannot wake the
	processor from Sleep since the timer is
	frozen during Sleep.

#### 11.1.5 8-BIT COUNTER MODE SYNCHRONIZATION

When in 8-Bit Counter mode, the incrementing edge on the T0CKI pin must be synchronized to the instruction clock. Synchronization can be accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the instruction clock. The high and low periods of the external clocking source must meet the timing requirements as shown in **Section 23.0** "**Electrical Specifications**".

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELB	—	—	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	53
CCP1CON	—	—	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	115
CCP2CON	—	—	DC2B1	DC2B0	CCP2M3	CCP2M2	CCP2M1	CCP2M0	115
INTCON	GIE	PEIE	TOIE	INTE	RBIE	T0IF	INTF	RBIF	36
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	37
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	39
PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	52
TMR1H	Holding Reg	ister for the	Most Signifi	cant Byte of	the 16-bit T	MR1 Regis	ter		99
TMR1L	Holding Reg	ister for the	Least Signif	icant Byte o	f the 16-bit 1	MR1 Regis	ster		99
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	52
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	62
T1CON	TMR1CS1	TMR1CS0	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	—	TMR10N	103
T1GCON	TMR1GE	T1GPOL	T1GTM	T1GSPM	T1GGO/ DONE	T1GVAL	T1GSS1	T1GSS0	104

#### TABLE 12-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER1

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the Timer1 module.

## 14.6 Operation During Sleep

The capacitive sensing oscillator will continue to run as long as the module is enabled, independent of the part being in Sleep. In order for the software to determine if a frequency change has occurred, the part must be awake. However, the part does not have to be awake when the timer resource is acquiring counts. One way to acquire the Timer1 counts while in Sleep is to have Timer1 gated with the overflow of the Watchdog Timer. This can be accomplished using the following steps:

- 1. Configure the Watchdog Time-out overflow as the Timer1's gate source T1GSS<1:0> = 11.
- 2. Set Timer1 gate to toggle mode by setting the T1GTM bit of the T1GCON register.
- 3. Set the TMR1GE bit of the T1GCON register.
- 4. Set TMR1ON bit of the T1CON register.
- 5. Enable capacitive sensing module with the appropriate current settings and pin selection.
- 6. Clear Timer1.
- 7. Put the part to Sleep.
- 8. On the first WDT overflow, the capacitive sensing oscillator will begin to increment Timer1. Then put the part to Sleep.
- 9. On the second WDT overflow Timer1 will stop incrementing. Then run the software routine to determine if a frequency change has occurred.

Refer to Section 12.0 "Timer1 Module with Gate Control" for additional information.

- Note 1: When using the WDT to set the interval on Timer1, any other source that wakes the part up early will cause the WDT overflow to be delayed, affecting the value captured by Timer1.
  - 2: Timer0 does not operate when in Sleep, and therefore cannot be used for capacitive sense measurements in Sleep.

R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R-0	R/W-0
CPSON	_	—	—	CPSRNG1	CPSRNG0	CPSOUT	TOXCS
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	nented bit, read	as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	iown
bit 7	<b>CPSON:</b> Capa 1 = Capacitiv 0 = Capacitiv	acitive Sensing e sensing mod e sensing mod	Module Enal ule is operatii ule is shut off	ble bit ng and consume:	s no operating c	urrent	
bit 6-4	Unimplemen	ted: Read as '	)'				
bit 3-2	CPSRNG<1:C 00 = Oscillato 01 = Oscillato 10 = Oscillato 11 = Oscillato	D>: Capacitive : for is Off. or is in low rangor is in medium or is in high ran	Sensing Oscil le. Charge/dis range. Charg ge. Charge/di	llator Range bit scharge curren je/discharge cu ischarge currer	s t is nominally 0. Irrent is nomina nt is nominally 1	1 μΑ. lly 1.2 μΑ. 8 μΑ.	
bit 1	<b>CPSOUT:</b> Cap 1 = Oscillator 0 = Oscillator	pacitive Sensin is sourcing cu is sinking curr	g Oscillator S rrent (Current ent (Current f	Status bit t flowing out the lowing into the	e pin) pin)		
bit 0	<b>TOXCS:</b> Time If TOCS = 1 The TOXCS b 1 = Timer0 C 0 = Timer0 C If TOCS = 0 Timer0 clock s	r0 External Clo it controls whic lock Source is lock Source is source is contro	ck Source Se h clock exterr the capacitive the TOCKI pir olled by the co	elect bit nal to the core/ e sensing oscill n ore/Timer0 mod	Timer0 module ator dule and is Fose	supplies Timer c/4.	0:

#### REGISTER 14-1: CPSCON0: CAPACITIVE SENSING CONTROL REGISTER 0

# 15.0 CAPTURE/COMPARE/PWM (CCP) MODULE

The Capture/Compare/PWM module is a peripheral which allows the user to time and control different events. In Capture mode, the peripheral allows the timing of the duration of an event. The Compare mode allows the user to trigger an external event when a predetermined amount of time has expired. The PWM mode can generate a Pulse-Width Modulated signal of varying frequency and duty cycle.

The timer resources used by the module are shown in Table 15-1.

Additional information on CCP modules is available in the Application Note *AN594, Using the CCP Modules* (DS00594).

#### TABLE 15-1: CCP MODE – TIMER RESOURCES REQUIRED

CCP Mode	Timer Resource				
Capture	Timer1				
Compare	Timer1				
PWM	Timer2				

CCP1 Mode	CCP2 Mode	Interaction
Capture	Capture	Same TMR1 time base
Capture	Compare	Same TMR1 time base <sup>(1, 2)</sup>
Compare	Compare	Same TMR1 time base <sup>(1, 2)</sup>
PWM	PWM	The PWMs will have the same frequency and update rate (TMR2 interrupt). The rising edges will be aligned.
PWM	Capture	None
PWM	Compare	None

## TABLE 15-2: INTERACTION OF TWO CCP MODULES

**Note 1:** If CCP2 is configured as a Special Event Trigger, CCP1 will clear Timer1, affecting the value captured on the CCP2 pin.

2: If CCP1 is in Capture mode and CCP2 is configured as a Special Event Trigger, CCP2 will clear Timer1, affecting the value captured on the CCP1 pin.

Note:	CCPRx	and	CCPx	throughout	this
	documer	nt refer	to CCP	R1 or CCPR2	and
	CCP1 or	CCP2	2, respec	tively.	

	SYNC = 0, BRGH = 1											
Fosc = 8.000 MHz		) MHz	Fosc = 4.000 MHz		Fosc = 3.6864 MHz			Fosc = 1.000 MHz				
RATE	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300	_	_	—				_		_	300	0.16	207
1200	—	—	—	1202	0.16	207	1200	0.00	191	1202	0.16	51
2400	2404	0.16	207	2404	0.16	103	2400	0.00	95	2404	0.16	25
9600	9615	0.16	51	9615	0.16	25	9600	0.00	23	—	_	—
10417	10417	0.00	47	10417	0.00	23	10473	0.53	21	10417	0.00	5
19.2k	19231	0.16	25	19.23k	0.16	12	19.2k	0.00	11	—	_	—
57.6k	55556	-3.55	8	—	—	—	57.60k	0.00	3	—	—	—
115.2k	—	—	—	—	_	—	115.2k	0.00	1	_	_	—

#### TABLE 16-5: BAUD RATES FOR ASYNCHRONOUS MODES









# 25.0 PACKAGING INFORMATION

## 25.1 Package Marking Information



\* Standard PICmicro<sup>®</sup> device marking consists of Microchip part number, year code, week code and traceability code. For PICmicro device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

## 28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-052C Sheet 1 of 2

#### 28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]





	Units				
Dimensio	n Limits	MIN	NOM	MAX	
Number of Pins	Ν	28			
Pitch	е	0.65 BSC			
Overall Height	А	-	-	2.00	
Molded Package Thickness	A2	1.65	1.75	1.85	
Standoff	A1	0.05	-	-	
Overall Width	E	7.40	7.80	8.20	
Molded Package Width	E1	5.00	5.30	5.60	
Overall Length	D	9.90	10.20	10.50	
Foot Length	L	0.55	0.75	0.95	
Footprint		1.25 REF			
Lead Thickness	С	0.09	-	0.25	
Foot Angle	¢	0°	4°	8°	
Lead Width	b	0.22	-	0.38	

#### Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
- 3. Dimensioning and tolerancing per ASME Y14.5M.
  - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
    - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073B

28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS			
Dimension	MIN	NOM	MAX	
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	С		7.20	
Contact Pad Width (X28)	X1			0.45
Contact Pad Length (X28)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2073A