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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 11x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf723at-i-so

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Pin Diagrams - 28-PIN SPDIP/SOIC/SSOP/QFN/UQFN (PIC16(L)F722A/723A)



2.2.2.1 STATUS Register

The STATUS register, shown in Register 2-1, contains:

- the arithmetic status of the ALU
- · the Reset status
- the bank select bits for data memory (SRAM)

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the TO and PD bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, CLRF STATUS will clear the upper three bits and set the Z bit. This leaves the STATUS register as '000u uluu' (where u = unchanged).

It is recommended, therefore, that only BCF, BSF, SWAPF and MOVWF instructions are used to alter the STATUS register, because these instructions do not affect any Status bits. For other instructions not affecting any Status bits (Refer to Section 21.0 "Instruction Set Summary").

Note 1:	The C and DC bits operate as Borrow
	and Digit Borrow out bits, respectively, in
	subtraction.

REGISTER 2	-1: STATU	IS: STATUS I	REGISTER				
R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	TO	PD	Z	DC ⁽¹⁾	C ⁽¹⁾
bit 7						·	bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	d as '0'	
-n = Value at P	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	nown
bit 7	IRP: Register 1 = Bank 2, 3 0 = Bank 0, 1	Bank Select b (100h-1FFh) (00h-FFh)	it (used for inc	direct addressi	ng)		
bit 6-5	RP<1:0>: Reg 00 = Bank 0 (01 = Bank 1 (10 = Bank 2 (11 = Bank 3 (gister Bank Se (00h-7Fh) (80h-FFh) (100h-17Fh) (180h-1FFh)	ect bits (used	for direct add	ressing)		
bit 4	TO: Time-out 1 = After pow 0 = A WDT tir	bit er-up, CLRWDT me-out occurre	instruction or d	SLEEP instruc	tion		
bit 3	PD: Power-do 1 = After pow 0 = By execut	own bit er-up or by the tion of the SLE:	CLRWDT instr	uction			
bit 2	Z: Zero bit 1 = The resul 0 = The resul	t of an arithmet t of an arithmet	ic or logic ope ic or logic ope	eration is zero eration is not ze	ero		
bit 1	DC: Digit Car	ry/Digit Borrow ut from the 4th	bit (ADDWF, A low-order bit o	DDLW, SUBLW,	, SUBWF instruc	tions) ⁽¹⁾	

- 0 = No carry-out from the 4th low-order bit of the result
- bit 0 C: Carry/Borrow bit⁽¹⁾ (ADDWF, ADDLW, SUBLW, SUBWF instructions)⁽¹⁾ 1 = A carry-out from the Most Significant bit of the result occurred
 - 0 = No carry-out from the Most Significant bit of the result occurred
- **Note 1:** For Borrow, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (RRF, RLF) instructions, this bit is loaded with either the high-order or low-order bit of the source register.

4.5.5 PIR2 REGISTER

The PIR2 register contains the interrupt flag bits, as shown in Register 4-5.

Note:	Interrupt flag bits are set when an interrupt							
	condition occurs, regardless of the state of							
	its corresponding enable bit or the global							
	enable bit, GIE of the INTCON register.							
	User software should ensure the							
	appropriate interrupt flag bits are clear prior							
	to enabling an interrupt.							

REGISTER 4-5: PIR2: PERIPHERAL INTERRUPT REQUEST REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	CCP2IF
bit 7							bit 0

Legend:				
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'				
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 7-1 Unimplemented: Read as '0'

bit 0 CCP2IF: CCP2 Interrupt Flag bit

Capture Mode:

1 = A TMR1 register capture occurred (must be cleared in software)

0 = No TMR1 register capture occurred

Compare Mode:

1 = A TMR1 register compare match occurred (must be cleared in software)

0 = No TMR1 register compare match occurred

PWM mode:

Unused in this mode

TABLE 4-1: SUMMARY OF REGISTERS ASSOCIATED WITH INTERRUPTS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	TOIE	INTE	RBIE	T0IF	INTF	RBIF	36
OPTION_REG	RBPU	INTEDG	TOCS	T0SE	PSA	PS2	PS1	PS0	19
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	37
PIE2	—	—	—	—	—	_	—	CCP2IE	38
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	39
PIR2	_	_	_			_	_	CCP2IF	40

Legend: - = Unimplemented locations, read as '0', u = unchanged, x = unknown. Shaded cells are not used by the Capture, Compare and PWM.

6.0 I/O PORTS

There are as many as thirty-five general purpose I/O pins available. Depending on which peripherals are enabled, some or all of the pins may not be available as general purpose I/O. In general, when a peripheral is enabled, the associated pin may not be used as a general purpose I/O pin.

6.1 Alternate Pin Function

The Alternate Pin Function Control (APFCON) register is used to steer specific peripheral input and output functions between different pins. The APFCON register is shown in Register 6-1. For this device family, the following functions can be moved between different pins:

- SS (Slave Select)
- CCP2

REGISTER 6-1: APFCON: ALTERNATE PIN FUNCTION CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	SSSEL	CCP2SEL
bit 7							bit 0

Legend:								
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'					
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown					

bit 7-2	Unimplemented: Read as '0'.
bit 1	SSSEL: SS Input Pin Selection bit
	0 = <u>SS</u> function is on RA5/AN4/CPS7/SS/VCAP 1 = <u>SS</u> function is on RA0/AN0/SS/VCAP
bit 0	CCP2SEL: CCP2 Input/Output Pin Selection bit
	0 = CCP2 function is on RC1/T1OSI/CCP2 1 = CCP2 function is on RB3/CCP2

6.2.1 ANSELA REGISTER

The ANSELA register (Register 6-4) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELA bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSELA bits has no affect on digital output functions. A pin with TRIS clear and ANSEL set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

REGISTER 6-4: ANSELA: PORTA ANALOG SELECT REGISTER

'1' = Bit is set

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	ANSA5	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0
bit 7							bit 0
Legend:							
R = Readable	R = Readable bit $W = Writable bit U = Unimplemented bit, read as '0'$			d as '0'			

'0' = Bit is cleared

bit 7-6 Unimplemented: Read as '0'

-n = Value at POR

bit 5-0 **ANSA<5:0>**: Analog Select between Analog or Digital Function on pins RA<5:0>, respectively 0 = Digital I/O. Pin is assigned to port or digital special function. 1 = Analog input. Pin is assigned as analog input⁽¹⁾. Digital input buffer disabled.

Note 1: When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

x = Bit is unknown

6.3 PORTB and TRISB Registers

PORTB is an 8-bit wide, bidirectional port. The corresponding data direction register is TRISB (Register 6-6). Setting a TRISB bit (= 1) will make the corresponding PORTB pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISB bit (= 0) will make the corresponding PORTB pin an output (i.e., enable the output driver and put the contents of the output latch on the selected pin). Example 6-2 shows how to initialize PORTB.

Reading the PORTB register (Register 6-5) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch.

The TRISB register (Register 6-6) controls the PORTB pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISB register are maintained set when using them as analog inputs. I/O pins configured as analog input always read '0'. Example 6-2 shows how to initialize PORTB.

EXAMPLE 6-2: INITIALIZING PORTB

BANKSEL PORTB ; CLRF PORTB ;Init PORTB BANKSEL ANSELB CLRF ANSELB ;Make RB<7:0> digital BANKSEL TRISB : MOVT.W B'11110000'; Set RB<7:4> as inputs ;and RB<3:0> as outputs MOVWF TRISB ;

Note: The ANSELB register must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0'.

6.3.1 ANSELB REGISTER

The ANSELB register (Register 6-9) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELB bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSELB bits has no affect on digital output functions. A pin with TRIS clear and ANSELB set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

6.3.2 WEAK PULL UPS

Each of the PORTB pins has an individually configurable internal weak pull up. Control bits WPUB<7:0> enable or disable each pull up (see Register 6-7). Each weak pull up is automatically turned off when the port pin is configured as an output. All pull ups are disabled on a Power-on Reset by the RBPU bit of the OPTION register.

6.3.3 INTERRUPT-ON-CHANGE

All of the PORTB pins are individually configurable as an interrupt-on-change pin. Control bits IOCB<7:0> enable or disable the interrupt function for each pin. Refer to Register 6-8. The interrupt-on-change feature is disabled on a Power-on Reset.

For enabled interrupt-on-change pins, the present value is compared with the old value latched on the last read of PORTB to determine which bits have changed or mismatched the old value. The 'mismatch' outputs of the last read are OR'd together to set the PORTB Change Interrupt flag bit (RBIF) in the INTCON register.

This interrupt can wake the device from Sleep. The user, in the Interrupt Service Routine, clears the interrupt by:

- a) Any read or write of PORTB. This will end the mismatch condition.
- b) Clear the flag bit RBIF.

A mismatch condition will continue to set flag bit RBIF. Reading or writing PORTB will end the mismatch condition and allow flag bit RBIF to be cleared. The latch holding the last read value is not affected by a MCLR nor Brown-out Reset. After these Resets, the RBIF flag will continue to be set if a mismatch is present.

Note: When a pin change occurs at the same time as a read operation on PORTB, the RBIF flag will always be set. If multiple PORTB pins are configured for the interrupt-on-change, the user may not be able to identify which pin changed state.

6.5 PORTE and TRISE Registers

PORTE⁽¹⁾ is an 1-bit wide, input-only port. RE3 is inputonly and its TRIS bit will always read as '1'.

Reading the PORTE register (Register 6-12) reads the status of the pins. RE3 reads '0' when MCLRE = 1.

REGISTER 6-12: PORTE: PORTE REGISTER

U-0	U-0	U-0	U-0	R-x	U-0	U-0	U-0
—	—	—	—	RE3	—	—	_
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

	0 = Port pin is < VIL
	1 = Port pin is > VIH
bit 3	RE3: PORTE I/O Pin bits ⁽¹⁾
bit 7-4	Unimplemented: Read as '0'

REGISTER 6-13: TRISE: PORTE TRI-STATE REGISTER

U-0	U-0	U-0	U-0	R-1	U-0	U-0	U-0
_	—	_	—	TRISE3	_	—	—
bit 7							bit 0

Legend:						
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	ented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			

bit 7-4	Unimplemented: Read as '0'
bit 3	TRISE3: RE3 Port Tri-state Control bit
	This bit is always '1' as RE3 is an input-only
bit 2-0	Unimplemented: Read as '0'

TABLE 6-5: SUMMARY OF REGISTERS ASSOCIATED WITH PORTE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
PORTE	—	—	-	—	RE3	—	—	—	69
TRISE	—	—		—	TRISE3 ⁽¹⁾	—	—	—	69

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTE

Note 1: This bit is always '1' as RE3 is input-only.

7.0 OSCILLATOR MODULE

7.1 Overview

The oscillator module has a wide variety of clock sources and selection features that allow it to be used in a wide range of applications while maximizing performance and minimizing power consumption. Figure 7-1 illustrates a block diagram of the oscillator module.

Clock sources can be configured from external oscillators, quartz crystal resonators, ceramic resonators and Resistor-Capacitor (RC) circuits. In addition, the system can be configured to use an internal calibrated high-frequency oscillator as clock source, with a choice of selectable speeds via software.

Clock source modes are configured by the FOSC bits in Configuration Word 1 (CONFIG1). The oscillator module can be configured for one of eight modes of operation.

- 1. RC External Resistor-Capacitor (RC) with Fosc/4 output on OSC2/CLKOUT.
- 2. RCIO External Resistor-Capacitor (RC) with I/O on OSC2/CLKOUT.
- 3. INTOSC Internal oscillator with Fosc/4 output on OSC2 and I/O on OSC1/CLKIN.
- 4. INTOSCIO Internal oscillator with I/O on OSC1/CLKIN and OSC2/CLKOUT.
- 5. EC External clock with I/O on OSC2/CLKOUT.
- HS High Gain Crystal or Ceramic Resonator mode.
- 7. XT Medium Gain Crystal or Ceramic Resonator Oscillator mode.
- 8. LP Low-Power Crystal mode.



FIGURE 7-1: SIMPLIFIED PIC[®] MCU CLOCK SOURCE BLOCK DIAGRAM

FIGURE 12-6:	TIMER1 GATE SINGLE-PULSE MODE	
TMR1GE		
T1GPOL		
T1GSPM		
T1GGO <u>/</u> DONE	← Set by software ←	Cleared by hardware on falling edge of T1GVAL
T1G_IN	rising edge of T1G	
T1CKI		
T1GVAL		
TIMER1	N N + 1	N + 2
TMR1GIF	Cleared by software	- Set by hardware on falling edge of T1GVAL

15.2 Compare Mode

In Compare mode, the 16-bit CCPRx register value is constantly compared against the TMR1 register pair value. When a match occurs, the CCPx module may:

- Toggle the CCPx output
- Set the CCPx output
- · Clear the CCPx output
- Generate a Special Event Trigger
- Generate a Software Interrupt

The action on the pin is based on the value of the CCPxM<3:0> control bits of the CCPxCON register.

All Compare modes can generate an interrupt.

FIGURE 15-2: COMPARE MODE OPERATION BLOCK DIAGRAM



- Special Event Trigger will:
- Clear TMR1H and TMR1L registers.
- NOT set interrupt flag bit TMR1IF of the PIR1 register.
 Set the GO/DONE bit to start the ADC conversion

(CCP2 only).

15.2.1 CCPx PIN CONFIGURATION

The user must configure the CCPx pin as an output by clearing the associated TRIS bit.

Either RC1 or RB3 can be selected as the CCP2 pin. Refer to **Section 6.1** "Alternate Pin Function" for more information.

Note: Clearing the CCPxCON register will force the CCPx compare output latch to the default low level. This is not the PORT I/O data latch.

15.2.2 TIMER1 MODE SELECTION

In Compare mode, Timer1 must be running in either Timer mode or Synchronized Counter mode. The compare operation may not work in Asynchronous Counter mode.

Note:	Clocking Timer1 from the system clock						
	(Fosc) should not be used in Compare						
	mode. For the Compare operation of the						
	TMR1 register to the CCPRx register to						
	occur, Timer1 must be clocked from the						
	instruction clock (Fosc/4) or from an						
	external clock source.						

15.2.3 SOFTWARE INTERRUPT MODE

When Software Interrupt mode is chosen (CCPxM<3:0> = 1010), the CCPxIF bit in the PIRx register is set and the CCPx module does not assert control of the CCPx pin (refer to the CCPxCON register).

15.2.4 SPECIAL EVENT TRIGGER

When Special Event Trigger mode is chosen (CCPxM<3:0> = 1011), the CCPx module does the following:

- Resets Timer1
- Starts an ADC conversion if ADC is enabled (CCP2 only)

The CCPx module does not assert control of the CCPx pin in this mode (refer to the CCPxCON register).

The Special Event Trigger output of the CCP occurs immediately upon a match between the TMR1H, TMR1L register pair and the CCPRxH, CCPRxL register pair. The TMR1H, TMR1L register pair is not reset until the next rising edge of the Timer1 clock. This allows the CCPRxH, CCPRxL register pair to effectively provide a 16-bit programmable period register for Timer1.

- **Note 1:** The Special Event Trigger from the CCP module does not set interrupt flag bit TMR1IF of the PIR1 register.
 - 2: Removing the match condition by changing the contents of the CCPRxH and CCPRxL register pair, between the clock edge that generates the Special Event Trigger and the clock edge that generates the Timer1 Reset, will preclude the Reset from occurring.

15.2.5 COMPARE DURING SLEEP

The Compare mode is dependent upon the system clock (Fosc) for proper operation. Since Fosc is shut down during Sleep mode, the Compare mode will not function properly during Sleep.

15.3.2 PWM PERIOD

The PWM period is specified by the PR2 register of Timer2. The PWM period can be calculated using the formula of Equation 15-1.

EQUATION 15-1: PWM PERIOD

$$PWM Period = [(PR2) + 1] \bullet 4 \bullet Tosc \bullet$$
$$(TMR2 Prescale Value)$$
Note: Tosc = 1/Fosc

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The CCPx pin is set. (Exception: If the PWM duty cycle = 0%, the pin will not be set.)
- The PWM duty cycle is latched from CCPRxL into CCPRxH.

Note:	The	Timer2	postscaler	(refer	to
	Secti	on 13.1 "	Timer2 Ope	r ation") is r	not
	used	in the d	etermination	of the PW	/M
	freque	ency.			

15.3.3 PWM DUTY CYCLE

The PWM duty cycle is specified by writing a 10-bit value to multiple registers: CCPRxL register and DCxB<1:0> bits of the CCPxCON register. The CCPRxL contains the eight MSbs and the DCxB<1:0> bits of the CCPxCON register contain the two LSbs. CCPRxL and DCxB<1:0> bits of the CCPxCON register can be written to at any time. The duty cycle value is not latched into CCPRxH until after the period completes (i.e., a match between PR2 and TMR2 registers occurs). While using the PWM, the CCPRxH register is read-only.

Equation 15-2 is used to calculate the PWM pulse width.

Equation 15-3 is used to calculate the PWM duty cycle ratio.

EQUATION 15-2: PULSE WIDTH

 $Pulse Width = (CCPRxL:CCPxCON < 5:4>) \bullet$

TOSC • (TMR2 Prescale Value)

Note: Tosc = 1/Fosc

EQUATION 15-3: DUTY CYCLE RATIO

 $Duty Cycle Ratio = \frac{(CCPRxL:CCPxCON < 5:4>)}{4(PR2 + 1)}$

The CCPRxH register and a 2-bit internal latch are used to double buffer the PWM duty cycle. This double buffering is essential for glitchless PWM operation.

The 8-bit timer TMR2 register is concatenated with either the 2-bit internal system clock (Fosc), or 2 bits of the prescaler, to create the 10-bit time base. The system clock is used if the Timer2 prescaler is set to 1:1.

When the 10-bit time base matches the CCPRxH and 2-bit latch, then the CCPx pin is cleared (refer to Figure 15-3).

	SYNC = 0, BRGH = 1												
BAUD	Fosc = 8.000 MHz			Fos	Fosc = 4.000 MHz			Fosc = 3.6864 MHz			Fosc = 1.000 MHz		
RATE	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	
300	_	_	—				_		_	300	0.16	207	
1200		—	—	1202	0.16	207	1200	0.00	191	1202	0.16	51	
2400	2404	0.16	207	2404	0.16	103	2400	0.00	95	2404	0.16	25	
9600	9615	0.16	51	9615	0.16	25	9600	0.00	23	—	—	—	
10417	10417	0.00	47	10417	0.00	23	10473	0.53	21	10417	0.00	5	
19.2k	19231	0.16	25	19.23k	0.16	12	19.2k	0.00	11	—	_	_	
57.6k	55556	-3.55	8	—	—	—	57.60k	0.00	3	—	—	—	
115.2k	—	—	_	—	_	—	115.2k	0.00	1	_	_	—	

TABLE 16-5: BAUD RATES FOR ASYNCHRONOUS MODES

FIGURE 16-8:	SYNCHRONOUS RECEPTION (MASTER MODE, SREN)	
RX/DT pin	bit 0 bit 1 bit 2 bit 3 bit 4 bit 5 bit 6 bit 7	
TX/CK pin		
Write to bit SREN		
SREN bit	l	
CREN bit <u>'</u> 0'		ʻ0'
RCIF bit (Interrupt)		
Read RCREG		
Note: Timing d	iagram demonstrates Synchronous Master mode with bit SREN = 1 and bit BRGH = 0 .	

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
INTCON	GIE	PEIE	TOIE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
RCREG	AUSART R	eceive Data	a Register						0000 0000	0000 0000
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000X	0000 000X
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111
TXSTA	CSRC	TX9	TXEN	SYNC	_	BRGH	TRMT	TX9D	0000 -010	0000 -010

TABLE 16-7: REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER RECEPTION

Legend: x = unknown, - = unimplemented read as '0'. Shaded cells are not used for synchronous master reception.

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0
bit 7							bit 0
Legend:							
R = Readable bit		W = Writable bit		U = Unimplemented bit, read as '0'			
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unk	nown
 bit 7 WCOL: Write Collision Detect bit 1 = The SSPBUF register is written while it is still transmitting the previous word (must be cleared in software) 0 = No collision 							
 bit 6 SSPOV: Receive Overflow Indicator bit 1 = A new byte is received while the SSPBUF register is still holding the previous data. In case of overflow, the data in SSPSR is lost. Overflow can only occur in Slave mode. The user must read the SSPBUF, even if only transmitting data, to avoid setting overflow. In Master mode, the overflow bit is not set since each new reception (and transmission) is initiated by writing to the SSPBUF register. 0 = No overflow 							
bit 5 SSPEN : Synchronous Serial Port Enable bit 1 = Enables serial port and configures SCK, SDO and SDI as serial port pins ⁽¹⁾ 0 = Disables serial port and configures these pins as I/O port pins							
bit 4 CKP : Clock Polarity Select bit 1 = Idle state for clock is a high level 0 = Idle state for clock is a low level							
bit 3-0	t 3-0 SSPM<3:0>: Synchronous Serial Port Mode Select bits 0000 = SPI Master mode, clock = Fosc/4 0011 = SPI Master mode, clock = Fosc/16 0010 = SPI Master mode, clock = Fosc/64 0011 = SPI Master mode, clock = TMR2 output/2 0100 = SPI Slave mode, clock = SCK pin. SS pin control enabled. 0101 = SPI Slave mode, clock = SCK pin. SS pin control disabled. SS can be used as I/O pin.						
NI. 4		• • • •					

REGISTER 17-1: SSPCON: SYNC SERIAL PORT CONTROL REGISTER (SPI MODE)

Note 1: When enabled, these pins must be properly configured as input or output.

17.2.5 RECEPTION

When the R/\overline{W} bit of the received address byte is clear, the master will write data to the slave. If an address match occurs, the received address is loaded into the SSPBUF register. An address byte overflow will occur if that loaded address is not read from the SSPBUF before the next complete byte is received.

An SSP interrupt is generated for each data transfer byte. The BF, R/\overline{W} and D/\overline{A} bits of the SSPSTAT register are used to determine the status of the last received byte.

FIGURE 17-10: I²C WAVEFORMS FOR RECEPTION (7-BIT ADDRESS)

RÆ	V = 0	_
Receiving Address SDA T ATXA6XA5XA4XA3XA2XA1	ACK Receiving Data ACK Receiving Data ACI / D7\D6\D5\D4\D3\D2\D1\D0\ /D7\D6\D5\D4\D3\D2\D1\D0\ /D7\D6\D5\D4\D3\D2\D1\D0\ (₹ <u> </u>
	└ <u></u> 9 <u>+</u> _1 <u>_</u> 2 <u>_</u> 3 <u>_</u> 4 <u>_</u> 5 <u>_</u> 6 <u></u> _7 <u>_</u> 8 <u></u> _9 <u>+</u> 1 <u>_</u> 2 <u></u> 3 <u>_</u> 4 <u>_</u> 5 <u>_6</u> <u>7</u> _8 <u>+</u> 9	
SSPIF	Cleared in software	Bus Master sends Stop
BF	SSPBUF register is read	condition
SSPOV		
	Bit SSPOV is set because the SSPBUF register is still full.	
	ACK is not sent.——	_

RETFIE	Return from Interrupt	RET	
Syntax:	[label] RETFIE	Syn	
Operands:	None	Оре	
Operation:	$\begin{array}{l} TOS \to PC, \\ 1 \to GIE \end{array}$	Оре	
Status Affected:	None	Stat	
Description:	Return from Interrupt. Stack is POPed and Top-of-Stack (TOS) is loaded in the PC. Interrupts are enabled by setting Global Interrupt Enable bit, GIE (INTCON<7>). This is a 2-cycle instruction.	Des	
Words:	1	Сус	
Cycles:	2	<u>Exa</u>	
Example:	RETFIE		
	After Interrupt PC = TOS GIE = 1	TAB	

RETLW	Return with literal in W
Syntax:	[<i>label</i>] RETLW k
Operands:	$0 \le k \le 255$
Operation:	$k \rightarrow (W);$ TOS \rightarrow PC
Status Affected:	None
Description:	The W register is loaded with the 8-bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a 2-cycle instruction.
Words:	1
Cycles:	2
Example:	CALL TABLE;W contains table
TABLE	<pre>;offset value ;W now has table value ADDWF PC ;W = offset RETLW k1 ;Begin table RETLW k2 ; RETLW kn ; End of table Before Instruction W = 0x07 After Instruction W = value of k8</pre>
RETURN	Return from Subroutine
Syntax:	[label] RETURN
Operands:	None
Operation:	$TOS \rightarrow PC$
Status Affected:	None
Description:	Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a 2-cycle instruc- tion.

23.6 Timing Parameter Symbology

The timing parameter symbols have been created with one of the following formats:

- 1. TppS2ppS
- 2. TppS

Т				
F	Frequency	Т	Time	
Lowerc	Lowercase letters (pp) and their meanings:			
рр				
сс	CCP1	osc	OSC1	
ck	CLKOUT	rd	RD	
CS	CS	rw	RD or WR	
di	SDI	SC	SCK	
do	SDO	SS	SS	
dt	Data in	t0	ТОСКІ	
io	I/O PORT	t1	T1CKI	
mc	MCLR	wr	WR	
Upperc	Uppercase letters and their meanings:			
S				
F	Fall	Р	Period	
Н	High	R	Rise	
I	Invalid (High-impedance)	V	Valid	
L	Low	Z	High-impedance	

FIGURE 23-2: LOAD CONDITIONS





FIGURE 24-8: PIC16LF722A/723A TYPICAL IDD vs. VDD OVER Fosc, EXTRC MODE







FIGURE 24-24: PIC16LF722A/723A TYPICAL IDD vs. Fosc OVER VDD, INTOSC MODE







