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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CSIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	23
Program Memory Size	56KB (56K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 5x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-WFQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e1a11b0agn2b000

A/D Converter (Max: 8 channels)

- 12-bit A/D Converter
  - Successive approximation type
  - Conversion time: 0.8 µs @ 5 V (S6E1A1xC0A) / 2.0 µs (S6E1A1xB0A)
  - Priority conversion available (2 levels of priority)
  - Scan conversion mode
  - Built-in FIFO for conversion data storage (for scan conversion: 16 steps, for priority conversion: 4 steps)

Base Timer (Max: 4 channels)

The operation mode of each channel can be selected from one of the following.

- 16-bit PWM timer
- 16-bit PPG timer
- 16/32-bit reload timer
- 16/32-bit PWC timer

General-purpose I/O Port

This series can use its pin as a general-purpose I/O port when it is not used for an external bus or a peripheral function. All ports can be set to fast general-purpose I/O ports or slow general-purpose I/O ports. In addition, this series has a port relocate function that can set to which I/O port a peripheral function can be allocated.

- All ports are Fast GPIO which can be accessed by 1cycle
- Capable of controlling the pull-up of each pin
- Capable of reading pin level directly
- Port relocate function
- Up to 37 fast general-purpose I/O ports @48pin package
- Certain ports are 5 V tolerant.

  See "3. Pin Assignment" and "5. I/O Circuit Type" for details of such pins.

Dual Timer (32/16-bit Down Counter)

The Dual Timer consists of two programmable 32/16-bit down counters. The operation mode of each timer channel can be selected from one of the following.

- Free-running mode
- Periodic mode (= Reload mode)
- One-shot mode

Quadrature Position/Revolution Counter (QPRC)

The Quadrature Position/Revolution Counter (QPRC) is used to measure the position of the position encoder. In addition, it can be used as an up/down counter.

- The detection edge for the three external event input pins AIN, BIN and ZIN is configurable.
- 16-bit position counter
- 16-bit revolution counter
- Two 16-bit compare registers

Multi-function Timer

The Multi-function Timer consists of the following blocks.

- 16-bit free-run timer × 3 channels
- Input capture × 4 channels
- Output compare × 6 channels
- ADC start compare × 6 channel
- Waveform generator × 3 channels
- 16-bit PPG timer × 3 channels

  IGBT mode is contained.

The following function can be used to achieve the motor control.

- PWM signal output function
- DC chopper waveform output function
- Dead time function
- Input capture function
- ADC start function
- DTIF (motor emergency stop) interrupt function

Real-time Clock (RTC)

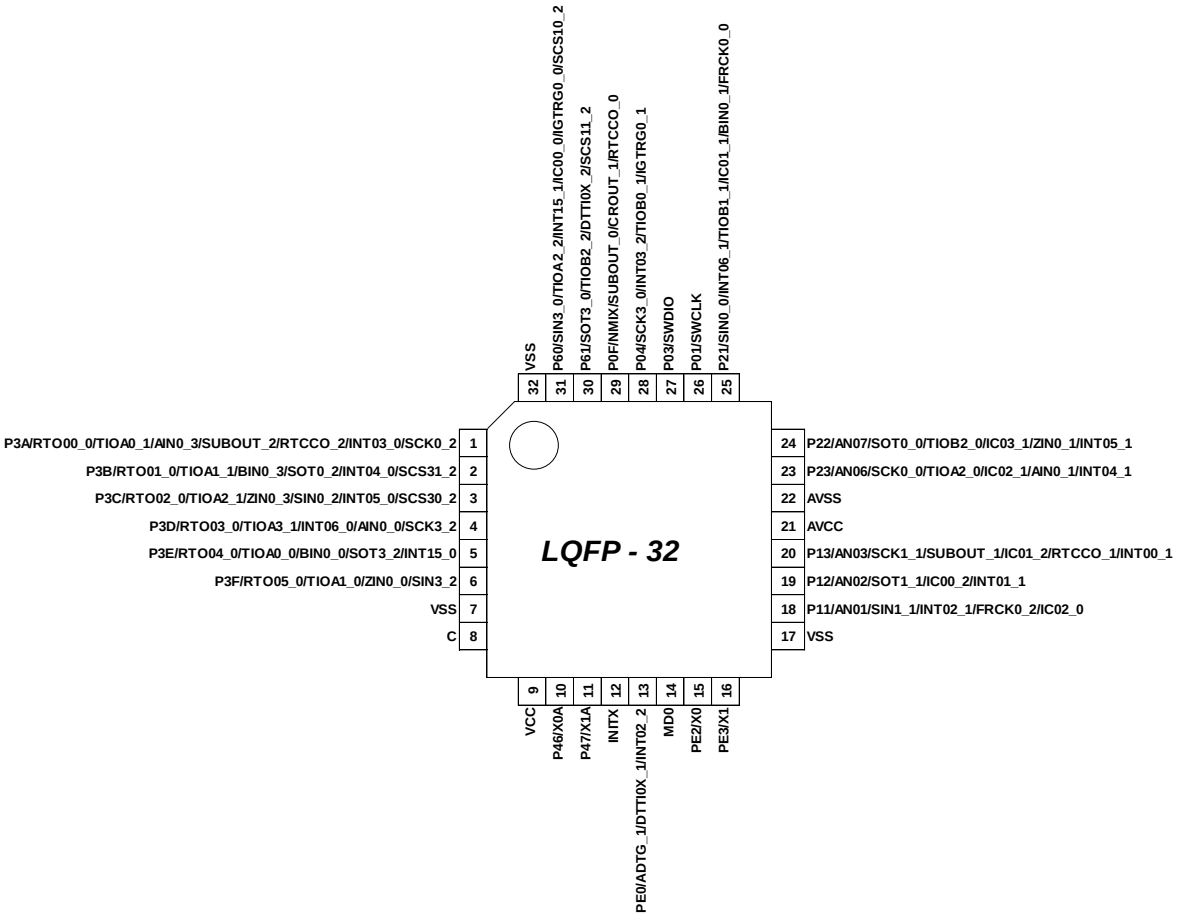
The Real-time Clock counts year/month/day/hour/minute/second/day of the week from year 01 to year 99.

- The RTC can generate an interrupt at a specific time (year/month/day/hour/minute/second/day of the week) and can also generate an interrupt in a specific year, in a specific month, on a specific day, at a specific hour or at a specific minute.
- It has a timer interrupt function generating an interrupt upon a specific time or at specific intervals.
- It can keep counting while rewriting the time.
- It can count leap years automatically.

3. Pin Assignment

FPT-32P-M30

(TOP VIEW)



Note:

- The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.
  Use the extended port function register (EPFR) to select the pin.

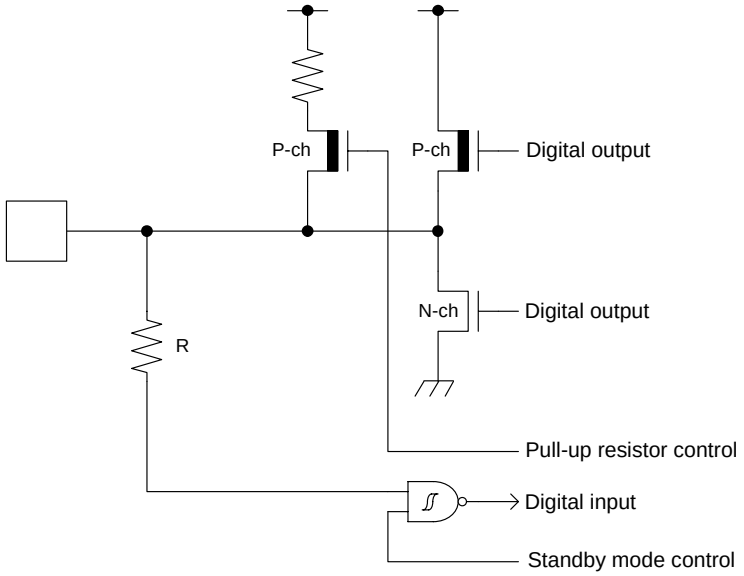
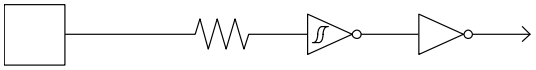
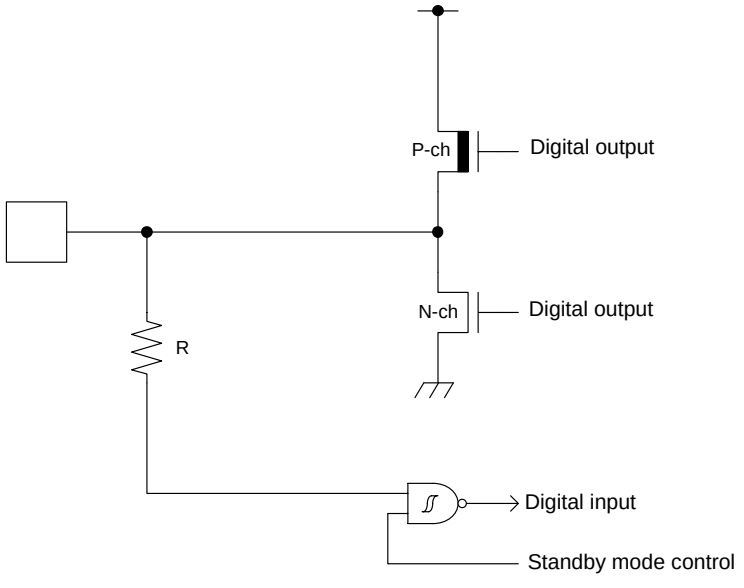
4. Pin Descriptions

List of Pin Functions

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.

Use the extended port function register (EPFR) to select the pin.

Pin no.			Pin name	I/O circuit type	Pin state type
LQFP-52	LQFP-48 QFN-48	LQFP-32 QFN-32			
1	1	-	VCC	-	
2	2	-	P50 INT00_0 AIN0_2 SIN3_1 IC01_0	I*	J
3	3	-	P51 INT01_0 BIN0_2 SOT3_1	I*	J
4	4	-	P52 INT02_0 ZIN0_2 SCK3_1	I*	J
6	5	-	P39 DTTI0X_0 ADTG_2	E	I
7	6	1	P3A RTO00_0 TIOA0_1 AIN0_3 SUBOUT_2 RTCCO_2 INT03_0 SCK0_2	F	J
8	7	2	P3B RTO01_0 TIOA1_1 BIN0_3 SOT0_2 INT04_0 SCS31_2	F	J

Type	Circuit	Remarks
I		• CMOS level output • CMOS level hysteresis input • 5V tolerant • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50kΩ • I_{OH}= -4mA, I_{OL}= 4mA • Available to control PZR registers • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off
J		CMOS level hysteresis input
K		• CMOS level output • CMOS level hysteresis input • With standby mode control • I_{OH}= -4mA, I_{OL}= 4mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off

Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

1. Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
2. Be sure that abnormal current flows do not occur during the power-on sequence.

Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

6.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

1. Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
   When you open Dry Package that recommends humidity 40% to 70% relative humidity.
3. When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
4. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
   Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

6.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity

   Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

2. Discharge of Static Electricity

   When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

3. Corrosive Gases, Dust, or Oil

   Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

4. Radiation, Including Cosmic Radiation

   Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

5. Smoke, Flame

   CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

Notes on Power-on

Turn power on/off in the following order or at the same time.

Turning on : VBAT → VCC
VCC → AVCC → AVRH
Turning off : VCC → VBAT
AVRH → AVCC → VCC

Serial Communication

There is a possibility to receive wrong data due to the noise or other causes on the serial communication.
Therefore, design a printed circuit board so as to avoid noise.

Consider the case of receiving wrong data due to noise, perform error detection such as by applying a checksum of data at the end.
If an error is detected, retransmit the data.

Differences in Features among the Products with Different Memory Sizes and between Flash Products and MASK Products

The electric characteristics including power consumption, ESD, latch-up, noise characteristics, and oscillation characteristics among the products with different memory sizes and between Flash products and MASK products are different because chip layout and memory structures are different.

If you are switching to use a different product of the same series, please make sure to evaluate the electric characteristics.

Pull-Up Function of 5V Tolerant I/O

Please do not input the signal more than VCC voltage at the time of Pull-Up function use of 5V tolerant I/O.

*1 : Ta=+25℃,V_{CC}=3.0V
*2 : Ta=+105℃,V_{CC}=5.5V
*3 : All ports are fixed
*4 : PCLK0=HCLK/8
*5 : The frequency is set to 4MHz by trimming
*6 : Flash sync down is set to FRWTR.RWT = 11 and FSYNDN.SD = 1111
*7 : V_{CC}=2.7V
*8 : When HCLK=4MHz, PLL OFF

Symbol (Pin name)	Conditions		Value		Unit	Remarks
			Typ	Max		
I_{CCH} (VCC)	STOP mode	Ta=25℃ Vcc=3.0V LVD off	5.6	28	µA	*1
		Ta=25℃ Vcc=5.0V LVD off	6.7	30	µA	*1
		Ta=105℃ Vcc=5.5V LVD off	-	540	µA	*1
I_{CCT} (VCC)	Sub timer mode	Ta=25℃ Vcc=3.0V 32kHz crystal oscillation LVD off	12	42	µA	*1
		Ta=25℃ Vcc=5.0V 32kHz crystal oscillation LVD off	13	44	µA	*1
		Ta=105℃ Vcc=5.5V 32kHz crystal oscillation LVD off	-	730	µA	*1
I_{CCR} (VCC)	RTC mode	Ta=25℃ Vcc=3.0V 32kHz crystal oscillation LVD off	9	36	µA	*1
		Ta=25℃ Vcc=5.0V 32kHz crystal oscillation LVD off	10	38	µA	*1
		Ta=105℃ Vcc=5.5V 32kHz crystal oscillation LVD off	-	570	µA	*1

*1:All ports are fixed.

LVD current

(V_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Low-Voltage detection circuit (LVD) power supply current	I_{CCLVD}	VCC	At operation	0.13	0.3	µA	For occurrence of reset
				0.13	0.3	µA	For occurrence of interrupt

Flash memory current

(V_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Flash memory write/erase current	$I_{CCFLASH}$	VCC	At Write/Erase	9.5	11.2	mA	

A/D convertor current (S6E1A1xC0A)

(V_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Power supply current	I_{CCAD}	AVCC	At operation	0.7	0.9	mA	
			At stop	0.13	13	µA	
Reference power supply current (AVRH)	I_{CCAVRH}	AVRH	At operation	1.1	1.97	mA	AVRH=5.5V
			At stop	0.1	1.7	µA	

A/D convertor current (S6E1A1xB0A)

(V_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Power supply current	I_{CCAD}	AVCC	At operation	1.8	2.87	mA	
			At stop	0.23	14.7	µA	

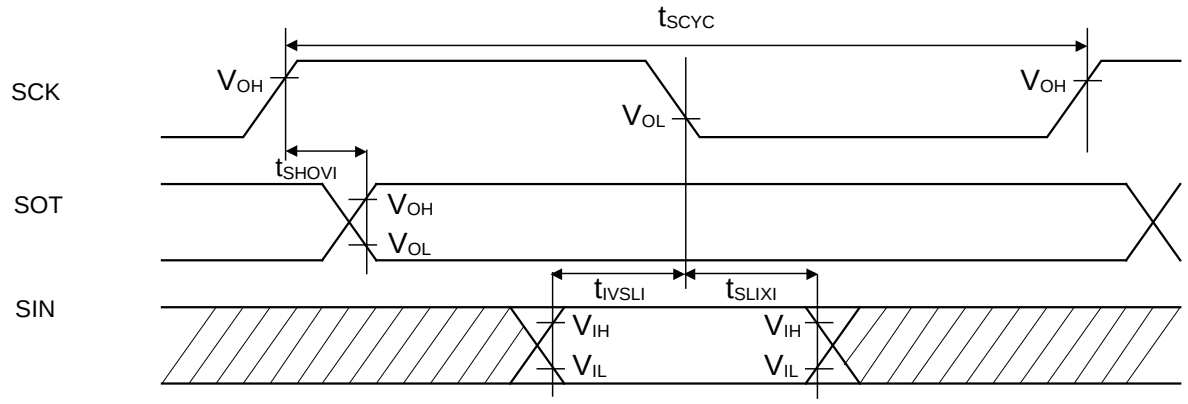
Peripheral current dissipation

Clock system	Peripheral	Conditions	Frequency (MHz)				Unit	Remarks
			4	8	20	40		
HCLK	GPIO	At all ports operation	0.11	0.22	0.55	1.10	mA	
	DMAC	At 2ch operation	0.05	0.11	0.25	0.51		
PCLK1	Base timer	At 4ch operation	0.03	0.05	0.15	0.30	mA	
	Multi-functional timer/PPG	At 1unit/4ch operation	0.14	0.28	0.68	1.38		
	Quadrature position/Revolution counter	At 1unit operation	0.02	0.04	0.11	0.22		
	ADC	At 1unit operation	0.07	0.14	0.37	0.73		
	Multi-function serial	At 1ch operation	0.15	0.31	0.77	1.54		

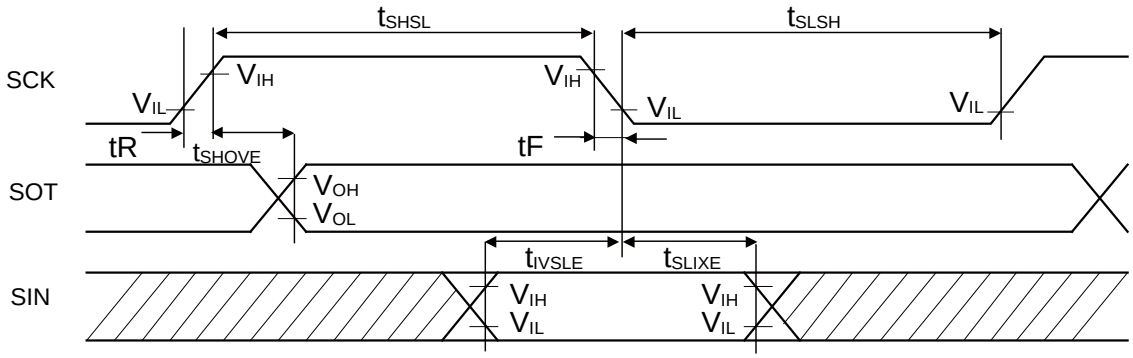
12.3.2 Pin Characteristics

(V_{CC} =AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage (hysteresis input)	V_{IHS}	CMOS hysteresis input pin, MD0, PE0	-	V_{CC} × 0.8	-	V_{CC} + 0.3	V	
		5V tolerant input pin	-	V_{CC} × 0.8	-	V_{SS} + 5.5	V	
"L" level input voltage (hysteresis input)	V_{ILS}	CMOS hysteresis input pin, MD0, PE0	-	V_{SS} - 0.3	-	V_{CC} × 0.2	V	
		5V tolerant input pin	-	V_{SS} - 0.3	-	V_{CC} × 0.2	V	
"H" level output voltage	V_{OH}	4 mA type	V_{CC} ≥ 4.5 V, I_{OH} = - 4 mA	V_{CC} - 0.5	-	V_{CC}	V	
			V_{CC} < 4.5 V, I_{OH} = - 2 mA					
		12 mA type	V_{CC} ≥ 4.5 V, I_{OH} = - 12 mA	V_{CC} - 0.5	-	V_{CC}	V	
			V_{CC} < 4.5 V, I_{OH} = - 8 mA					
"L" level output voltage	V_{OL}	4 mA type	V_{CC} ≥ 4.5 V, I_{OL} = 4 mA	V_{SS}	-	0.4	V	
			V_{CC} < 4.5 V, I_{OL} = 2 mA					
		12 mA type	V_{CC} ≥ 4.5 V, I_{OL} = 12 mA	V_{SS}	-	0.4	V	
			V_{CC} < 4.5 V, I_{OL} = 8 mA					
Input leak current	I_{IL}	-	-	- 5	-	+ 5	µA	
Pull-up resistance value	R_{PU}	Pull-up pin	V_{CC} ≥ 4.5 V	33	50	90	kΩ	
			V_{CC} < 4.5 V	-	-	180		
Input capacitance	C_{IN}	Other than VCC, VSS, AVCC, AVSS, AVRH	-	-	5	15	pF	



MS bit = 0



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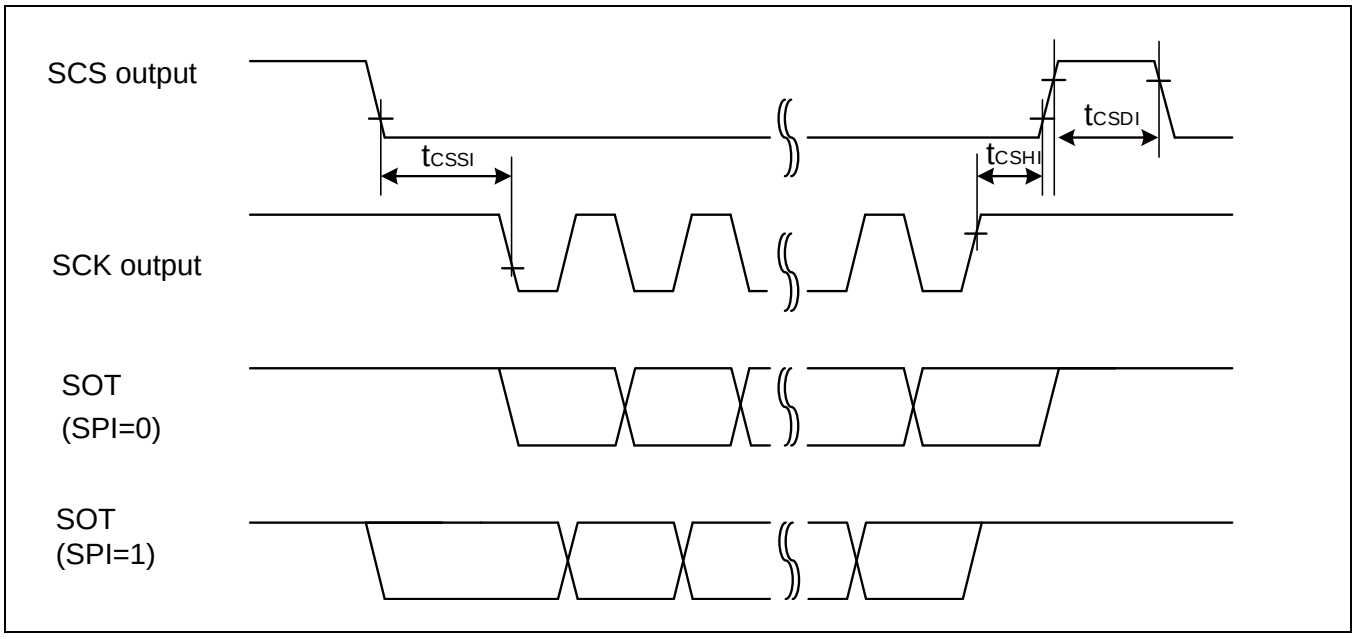
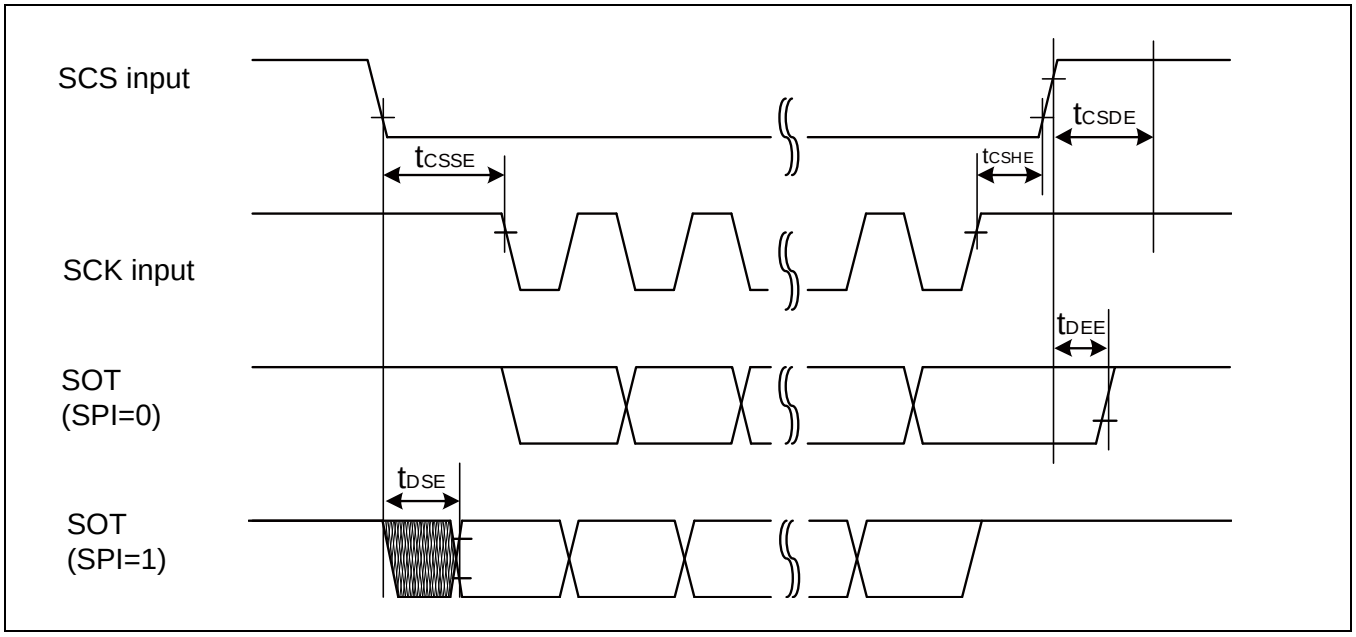
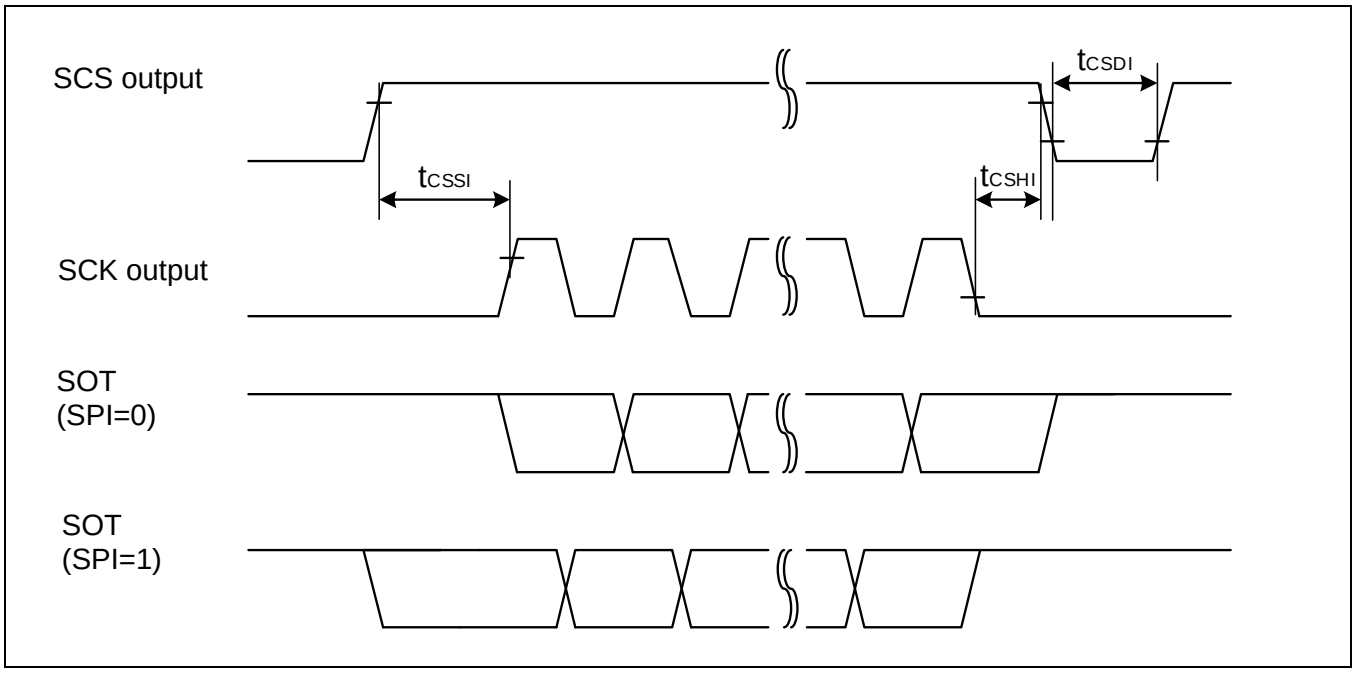
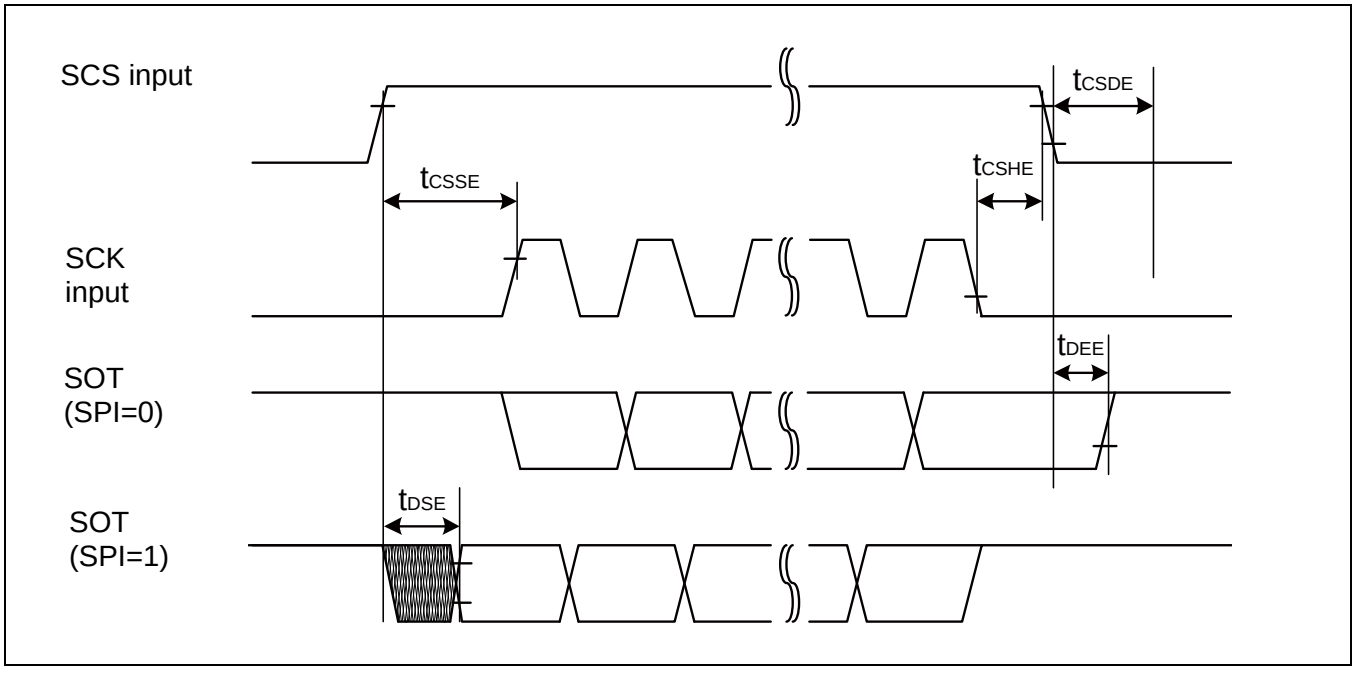

SCS output
tCSSI
tCSHI
tCSDI
SCK output
SOT
(SPI=0)
SOT
(SPI=1)


SCS input
tCSSE
tCSHE
tCSDE
SCK input
tDEE
SOT
(SPI=0)
tDSE
SOT
(SPI=1)

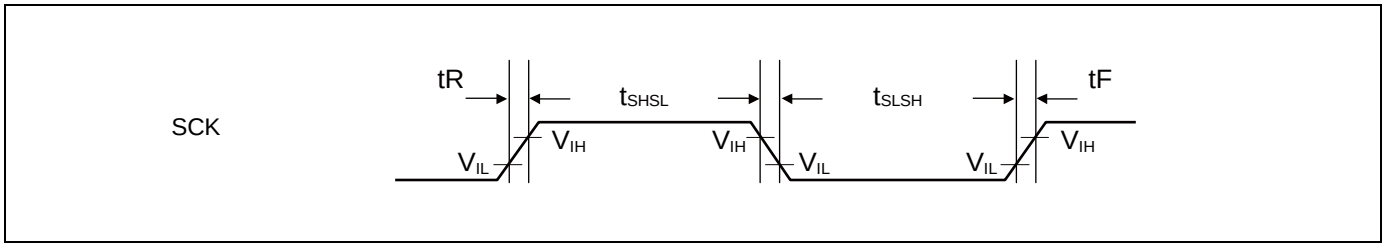

SCS output
SCK output
SOT
(SPI=0)
SOT
(SPI=1)
tCSSI
tCSHI
tCSDI

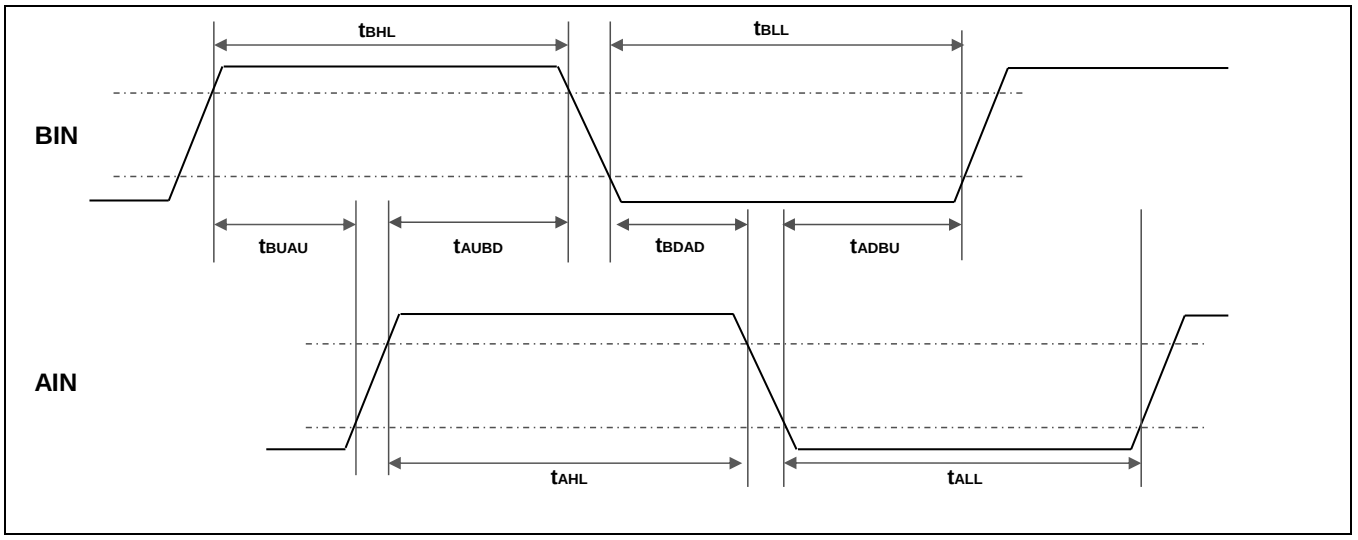

SCS input
SCK
input
SOT
(SPI=0)
SOT
(SPI=1)
tCSSE
tCSHE
tCSDE
tDEE
tDSE

External clock (EXT = 1): asynchronous only

(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Serial clock "L" pulse width	t_{SLSH}	C_L = 30 pF	t_{CYCP} + 10	-	ns	
Serial clock "H" pulse width	t_{SHSL}		t_{CYCP} + 10	-	ns	
SCK falling time	tF		-	5	ns	
SCK rising time	tR		-	5	ns	

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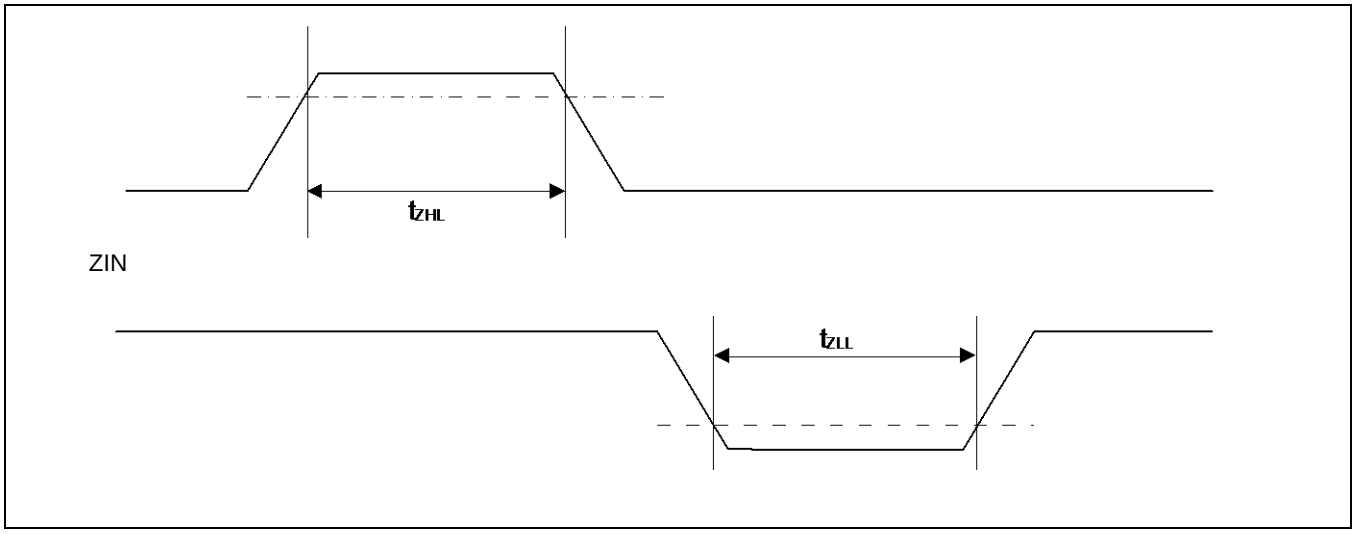
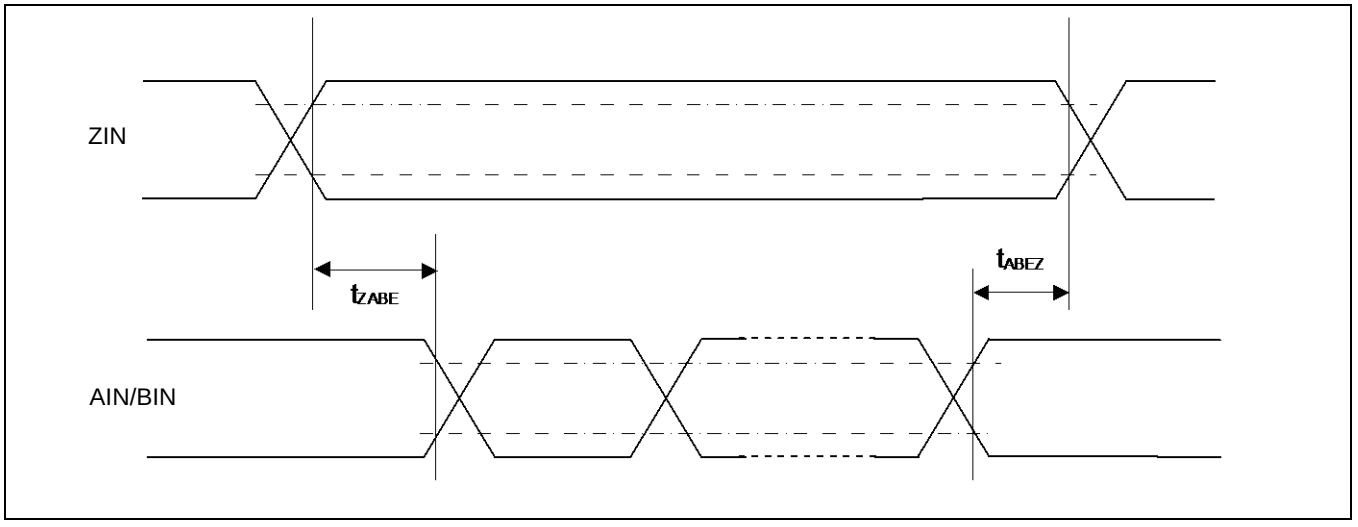
tBLL
BIN
tBUAU
tAUBD
tBDAD
tADBU
AIN
tAHL
tALL


tZHL
ZIN
tZLL


ZIN
tZABE
tABEZ
AIN/BIN

12.7 Flash Memory Write/Erase Characteristics

(V_{CC} = 2.7 V to 5.5 V, Ta = - 40°C to + 105°C)

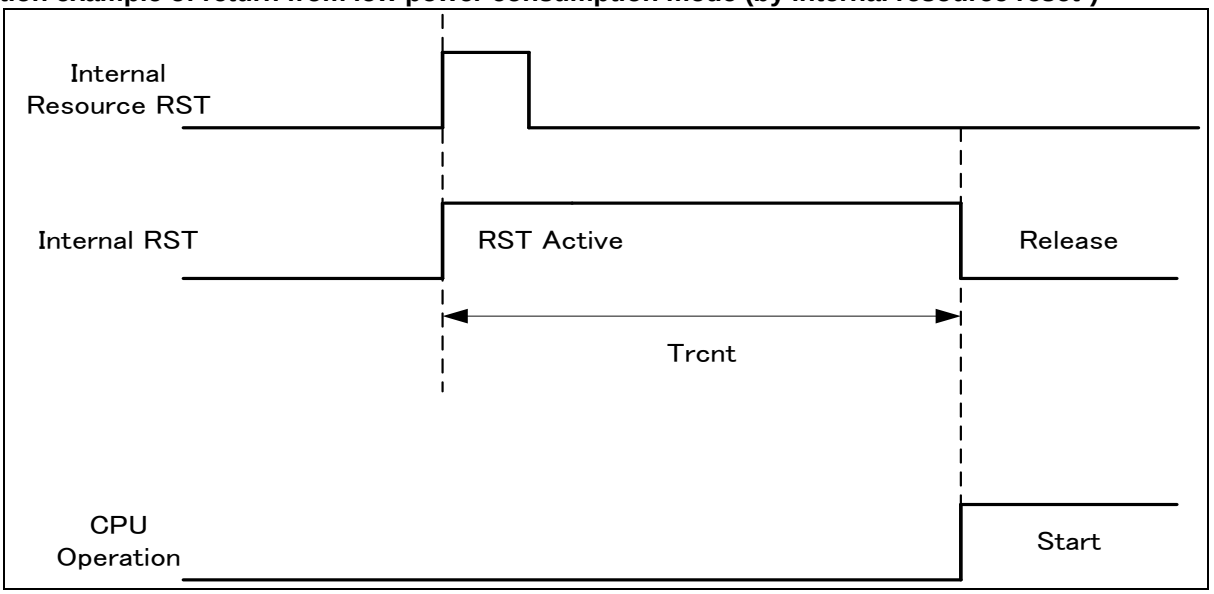
Parameter		Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	Large sector	-	0.7	2.2	s	The sector erase time includes the time of writing prior to internal erase.
	Small sector		0.3	0.9		
Halfword (16-bit) write time		-	30	528	µs	The halfword (16-bit) write time excludes the system-level overhead.
Chip erase time		-	2.6	8	s	The chip erase time includes the time of writing prior to internal erase.

Write/erase cycle and data hold time

Write/erase cycle	Data hold time (year)	Remarks
1,000	20*	
10,000	10*	

*: This value was converted from the result of a technology reliability assessment. (This value was converted from the result of a high temperature accelerated test using the Arrhenius equation with the average temperature value being + 85°C).

Operation example of return from low power consumption mode (by internal resource reset*)

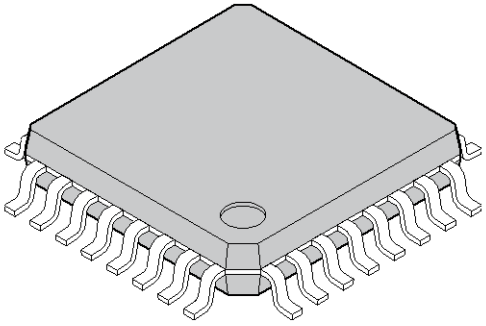


*: Internal resource reset is not included in return factor by the kind of Low-Power consumption mode.

Notes:

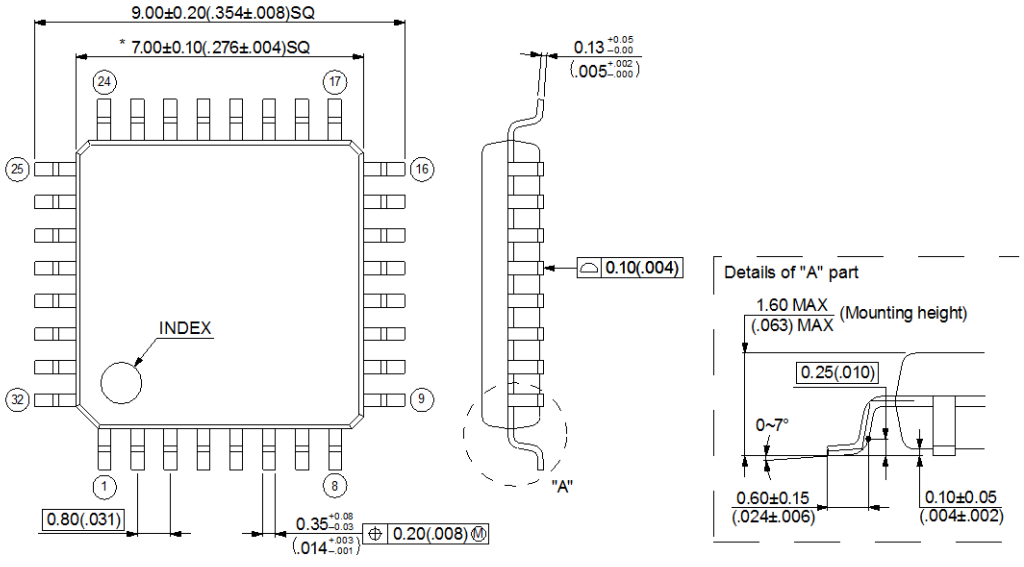
- The return factor is different in each Low-Power consumption modes.
  See "Chapter: Low Power Consumption Mode" and "Operations of Standby Modes" in FM0+ Family PERIPHERAL MANUAL.
- When interrupt recoveries, the operation mode that CPU recoveries depends on the state before the Low-Power consumption mode transition. See "CHAPTER: Low Power Consumption Mode" in "FM0+ Family PERIPHERAL MANUAL".
- The time during the power-on reset/low-voltage detection reset is excluded. See "12.4.7 Power-on Reset Timing " for the detail on the time during the power-on reset/low -voltage detection reset.
- When in recovery from reset, CPU changes to the high-speed CR run mode. When using the main clock or the PLL clock, it is necessary to add the main clock oscillation stabilization wait time or the main PLL clock stabilization wait time.
- The internal resource reset means the watchdog reset and the CSV reset.

14. Package Dimensions

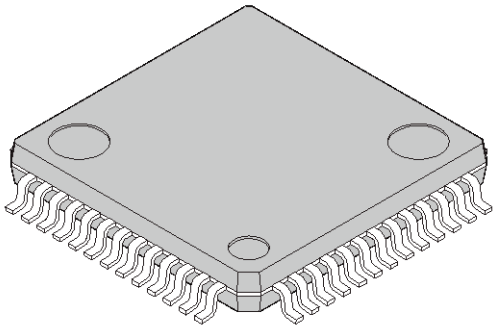
32-pin plastic LQFP		
 (FPT-32P-M30)	Lead pitch	0.80 mm
	Package width × package length	7.00 mm × 7.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.60 mm MAX

32-pin plastic LQFP
(FPT-32P-M30)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.

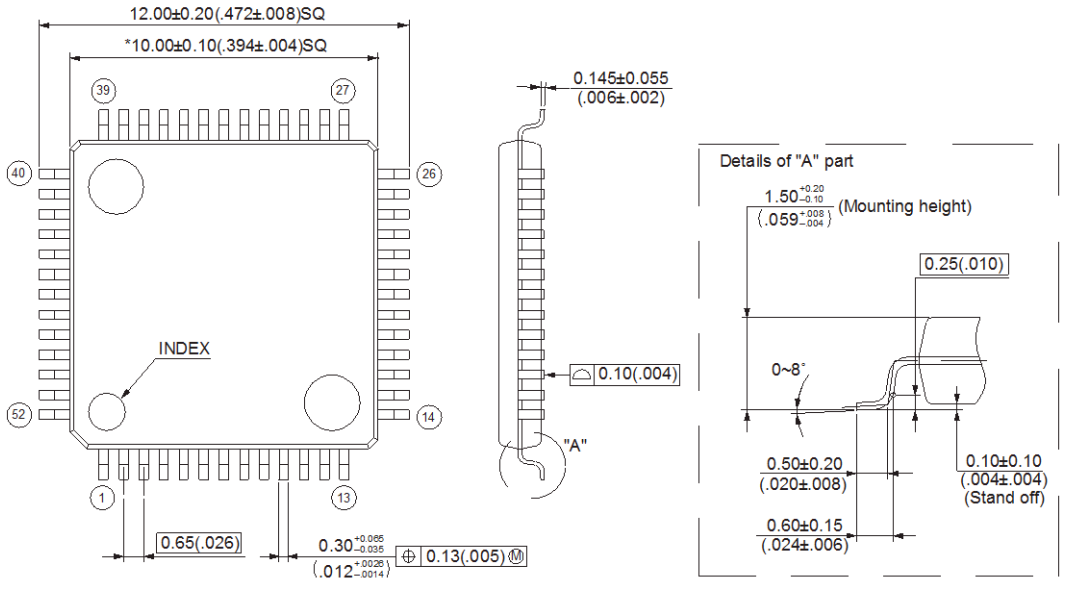


Dimensions in mm (inches).
Note: The values in parentheses are reference **values.**

52-pin plastic LQFP		
	Lead pitch	0.65 mm
	Package width × package length	10.00 × 10.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.32 g
(FPT-52P-M02)	Code (Reference)	P-LFQFP52-10 × 10-0.65

52-pin plastic LQFP
(FPT-52P-M02)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values