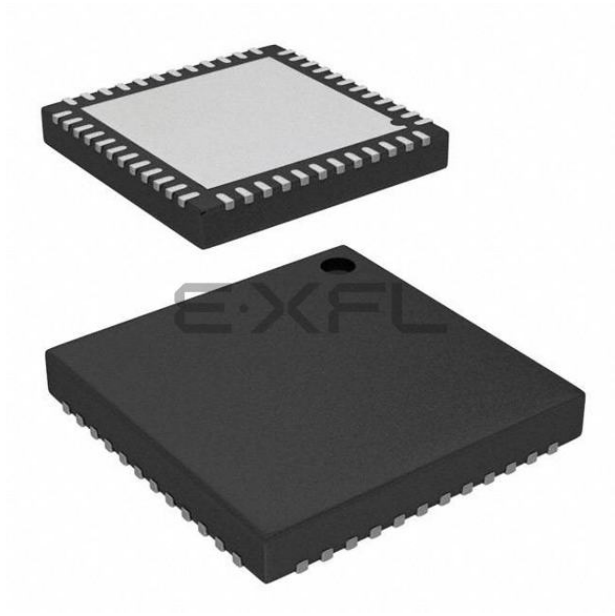
Infineon Technologies - S6E1A11C0AGN2B000 Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CSIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	56KB (56K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-WFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e1a11c0agn2b000

Watch Counter
The Watch Counter wakes up the microcontroller from the low power consumption mode. The clock source can be selected from the main clock, the sub clock, the built-in high-speed CR clock or the built-in low-speed CR clock.

Interval timer: up to 64 s (sub clock: 32.768 kHz)

External Interrupt Controller Unit

- Up to 8 external interrupt input pins
- Non-maskable interrupt (NMI) input pin: 1

Watchdog Timer (2 channels)
The watchdog timer generates an interrupt or a reset when the counter reaches a time-out value.

This series consists of two different watchdogs, "hardware" watchdog and "software" watchdog.

The "hardware" watchdog timer is clocked by the built-in low-speed CR oscillator. Therefore, the "hardware" watchdog is active in any low-power consumption modes except RTC mode and STOP mode.

Clock and Reset

- Clocks

A clock can be selected from five clock sources (two external oscillators, two built-in CR oscillator, and main PLL).

  - Main clock : 4 MHz to 40MHz
  - Sub clock : 32.768 kHz
  - Built-in high-speed CR clock : 4 MHz
  - Built-in low-speed CR clock : 100 kHz
  - Main PLL clock

- Resets
  - Reset request from the INITX pin
  - Power on reset
  - Software reset
  - Watchdog timer reset
  - Low-voltage detection reset
  - Clock supervisor reset

Clock Supervisor (CSV)
The Clock Supervisor monitors the failure of external clocks with a clock generated by a built-in CR oscillator.

- If an external clock failure (clock stop) is detected, a reset is asserted.
- If an external frequency anomaly is detected, an interrupt or a reset is asserted.

Low-voltage Detector (LVD)
This series monitors the voltage on the VCC pin with a 2-stage mechanism. When the voltage falls below a designated voltage, the Low-voltage Detector generates an interrupt or a reset.

- LVD1: error reporting via an interrupt
- LVD2: auto-reset operation

Low Power Consumption Mode
This series has four low power consumption modes.

- SLEEP
- TIMER
- RTC
- STOP

Peripheral Clock Gating
The system can reduce the current consumption of the total system with gating the operation clocks of peripheral functions not used.

Debug

- Serial Wire Debug Port (SW-DP)
- Micro Trace Buffer (MTB)

Unique ID
A 41-bit unique value of the device has been set.

Power Supply
Wide voltage range: VCC = 2.7 V to 5.5 V

2. Packages

Product name / Package	S6E1A11B0A S6E1A12B0A	S6E1A11C0A S6E1A12C0A
LQFP: FPT-32P-M30 (0.80 mm pitch)	❍	-
QFN: LCC-32P-M73 (0.50 mm pitch)	❍	-
LQFP: FPT-48P-M49 (0.50 mm pitch)	-	❍
QFN: LCC-48P-M74 (0.50 mm pitch)	-	❍
LQFP: FPT-52P-M02 (0.65 mm pitch)	-	❍

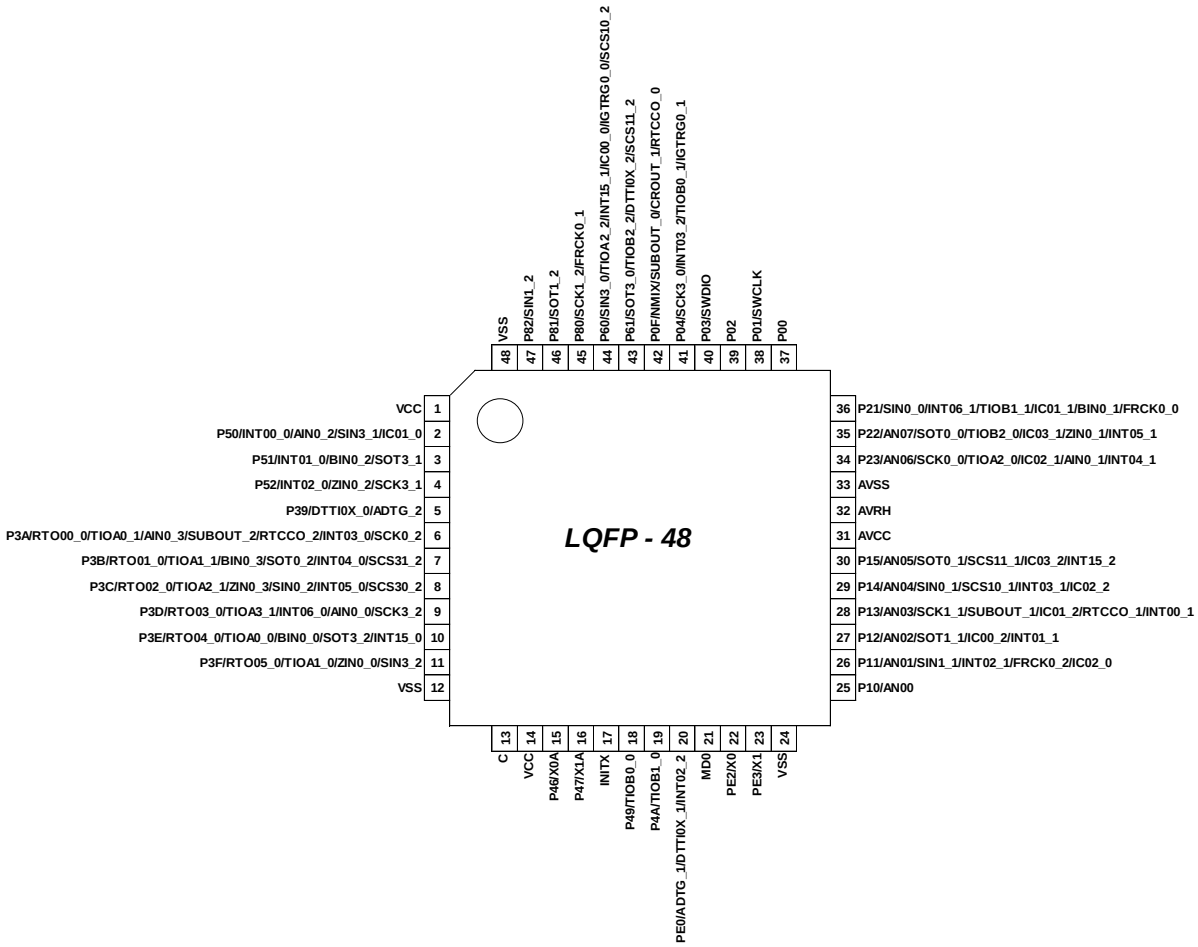
❍: Supported

Note:

- See "14. Package Dimensions" for detailed information on each package.

FPT-48P-M49

(TOP VIEW)



Note:

- The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.
  Use the extended port function register (EPFR) to select the pin.

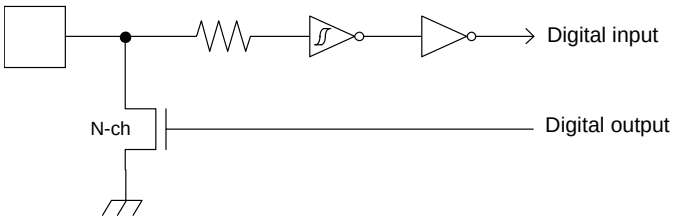
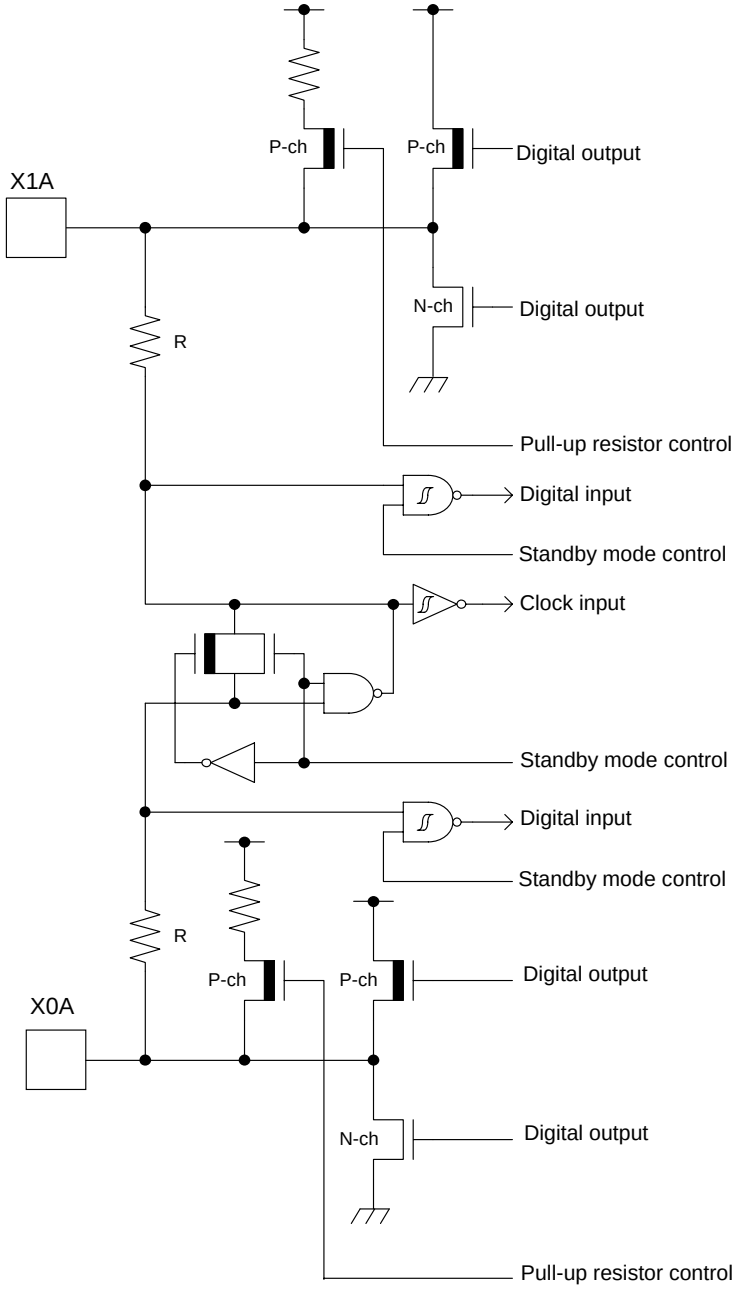
4. Pin Descriptions

List of Pin Functions

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.

Use the extended port function register (EPFR) to select the pin.

Pin no.			Pin name	I/O circuit type	Pin state type
LQFP-52	LQFP-48 QFN-48	LQFP-32 QFN-32			
1	1	-	VCC	-	
2	2	-	P50 INT00_0 AIN0_2 SIN3_1 IC01_0	I*	J
3	3	-	P51 INT01_0 BIN0_2 SOT3_1	I*	J
4	4	-	P52 INT02_0 ZIN0_2 SCK3_1	I*	J
6	5	-	P39 DTTI0X_0 ADTG_2	E	I
7	6	1	P3A RTO00_0 TIOA0_1 AIN0_3 SUBOUT_2 RTCCO_2 INT03_0 SCK0_2	F	J
8	7	2	P3B RTO01_0 TIOA1_1 BIN0_3 SOT0_2 INT04_0 SCS31_2	F	J

Type	Circuit	Remarks
C		• Open drain output • CMOS level hysteresis input
D		It is possible to select the sub oscillation / GPIO function When the sub oscillation is selected. • Oscillation feedback resistor : Approximately 5MΩ • With standby mode control When the GPIO is selected. • CMOS level output. • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50kΩ • I_{OH}= -4mA, I_{OL}= 4mA

7. Handling Devices

Power Supply Pins

In products with multiple VCC and VSS pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. However, all of these pins should be connected externally to the power supply or ground lines in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with each POWER pins and GND pins of this device at low impedance. It is also advisable that a ceramic capacitor of approximately 0.1 µF be connected as a bypass capacitor between VCC and VSS, between AVCC and AVSS and between AVRH and AVRL near this device.

A malfunction may occur when the power supply voltage fluctuates rapidly even though the fluctuation is within the guaranteed operating range of the VCC power supply voltage. As a rule of voltage stabilization, suppress voltage fluctuation so that the fluctuation in VCC ripple (peak-to-peak value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the standard VCC value, and the transient fluctuation rate does not exceed 0.1 V/µs at a momentary fluctuation such as switching the power supply.

Crystal Oscillator Circuit

Noise near the X0/X1 and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1, X0A/X1A pins, the crystal oscillator (or ceramic oscillator), and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended that the PC board artwork be designed such that the X0/X1 and X0A/X1A pins are surrounded by ground plane as this is expected to produce stable operation.

Evaluate oscillation of your using crystal oscillator by your mount board.

Sub Crystal Oscillator

This series sub oscillator circuit is low gain to keep the low current consumption.
The crystal oscillator to fill the following conditions is recommended for sub crystal oscillator to stabilize the oscillation.

■Surface mount type

Size:	More than 3.2 mm × 1.5 mm
Load capacitance:	Approximately 6 pF to 7 pF When the Standard setting (CCS/CCB=11001110)
Load capacitance:	Approximately 4 pF to 7 pF When the low power setting (CCS/CCB=00000100)

■Lead type

Load capacitance:	Approximately 6 pF to 7 pF When the Standard setting (CCS/CCB=11001110)
Load capacitance:	Approximately 4 pF to 7 pF When the low power setting (CCS/CCB=00000100)

Notes on Power-on

Turn power on/off in the following order or at the same time.

Turning on : VBAT → VCC
VCC → AVCC → AVRH
Turning off : VCC → VBAT
AVRH → AVCC → VCC

Serial Communication

There is a possibility to receive wrong data due to the noise or other causes on the serial communication.
Therefore, design a printed circuit board so as to avoid noise.

Consider the case of receiving wrong data due to noise, perform error detection such as by applying a checksum of data at the end.
If an error is detected, retransmit the data.

Differences in Features among the Products with Different Memory Sizes and between Flash Products and MASK Products

The electric characteristics including power consumption, ESD, latch-up, noise characteristics, and oscillation characteristics among the products with different memory sizes and between Flash products and MASK products are different because chip layout and memory structures are different.

If you are switching to use a different product of the same series, please make sure to evaluate the electric characteristics.

Pull-Up Function of 5V Tolerant I/O

Please do not input the signal more than VCC voltage at the time of Pull-Up function use of 5V tolerant I/O.

Pin status type	Function group	State upon power-on reset or low-voltage detection	State at INITX input	State upon device internal reset	State in Run mode or SLEEP mode	State in TIMER mode, RTC mode, or STOP mode	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable	
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1	
		-	-	-	-	SPL = 0	SPL = 1
	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state
	Resource other than the above selected						Hi-Z / Internal input fixed at "0"
	GPIO selected						

*1:Oscillation stops in Sub timer mode, Low-speed CR timer mode, STOP mode, RTC mode.

*2:Oscillation stops in STOP mode.

12.3 DC Characteristics

12.3.1 Current Rating

Symbol (Pin name)	Conditions		HCLK Frequency *4	Value Typ*1	Value Max*2	Unit	Remarks
Icc (VCC)	Run mode, code executed from Flash	4MHz external clock input, PLL ON*8 NOP code executed Built-in high speed CR stopped All peripheral clock stopped by CKENx	4MHz	0.7	1.5	mA	*3
			8MHz	1.3	2.3		
			20MHz	2.8	4.0		
			40MHz	5.7	7.3		
		4MHz external clock input, PLL ON*8 Benchmark code executed Built-in high speed CR stopped PCLK1 stopped	4MHz	0.6	1.4	mA	*3
			8MHz	1.2	2.1		
			20MHz	2.6	3.7		
			40MHz	4.8	6.3		
		4MHz crystal oscillation, PLL ON*8 NOP code executed Built-in high speed CR stopped All peripheral clock stopped by CKENx	4MHz	1.0	2.9	mA	*3
			8MHz	1.7	3.6		
			20MHz	3.4	5.6		
			40MHz	5.7	8.2		
	Run mode, code executed from RAM	4MHz external clock input, PLL ON*8 NOP code executed Built-in high speed CR stopped All peripheral clock stopped by CKENx	4MHz	0.5	1.2	mA	*3
			8MHz	0.9	1.8		
			20MHz	2.0	2.9		
			40MHz	3.7	4.8		
	Run mode, code executed from Flash	4MHz external clock input, PLL ON NOP code executed Built-in high speed CR stopped PCLK1 stopped	40MHz	2.8	3.7	mA	*3,*6,*7
	Run mode, code executed from Flash	Built-in high speed CR*5 NOP code executed All peripheral clock stopped by CKENx	4MHz	0.8	1.5	mA	*3
		32kHz crystal oscillation NOP code executed All peripheral clock stopped by CKENx	32kHz	65	900	µA	*3
		Built-in low speed CR NOP code executed All peripheral clock stopped by CKENx	100kHz	73	920	µA	*3
Iccs (VCC)	SLEEP operation	4MHz external clock input, PLL ON*8 All peripheral clock stopped by CKENx	4MHz	0.4	1.2	mA	*3
			8MHz	0.7	1.6		
			20MHz	1.5	2.4		
			40MHz	2.7	3.7		
		Built-in high speed CR*5 All peripheral clock stopped by CKENx	4MHz	0.5	1.2	mA	*3
		32kHz crystal oscillation All peripheral clock stopped by CKENx	32kHz	63	880	µA	*3
		Built-in low speed CR All peripheral clock stopped by CKENx	100kHz	66	890	µA	*3

12.4.9 CSIO Timing

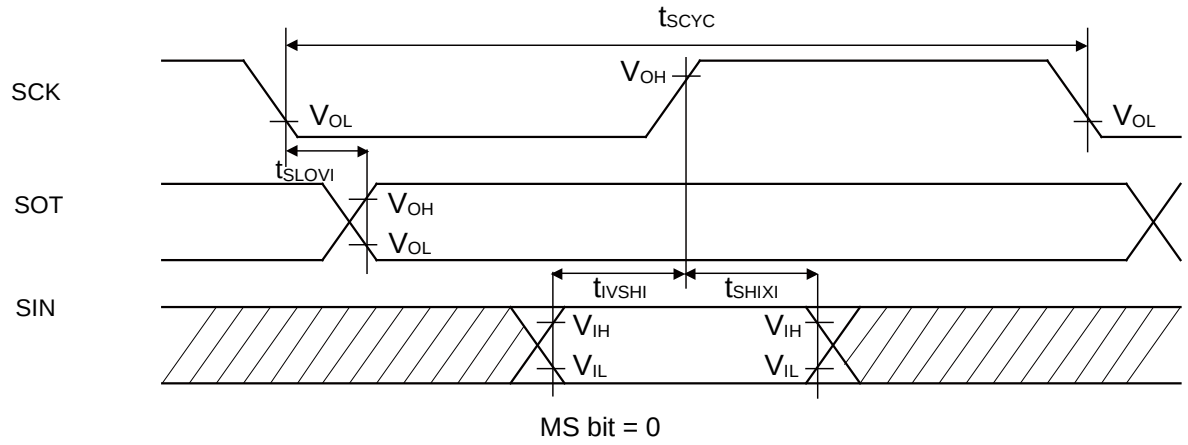
Synchronous serial (SPI = 0, SCINV = 0)

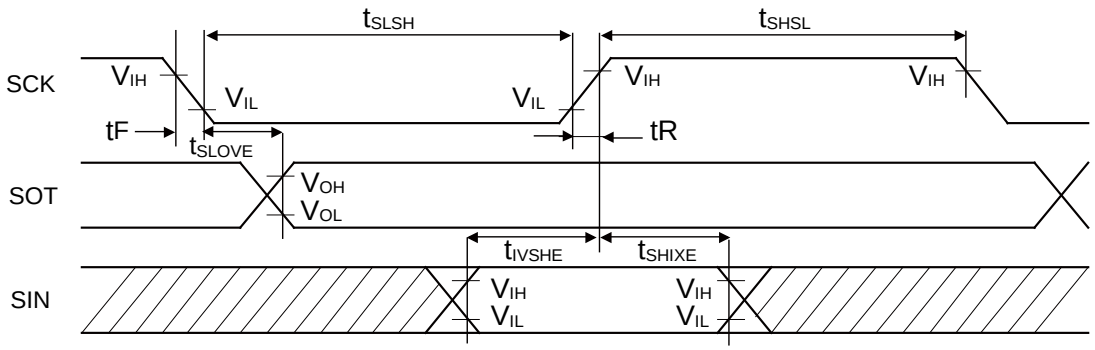
(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	4 t_{CYCP}	-	4 t_{CYCP}	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	30	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	External shift clock operation	2 t_{CYCP} - 10	-	2 t_{CYCP} - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	-	30	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- The above AC characteristics are for CLK synchronous mode.
- t_{CYCP} represents the APB bus clock cycle time.
  For the number of the APB bus to which Multi-function Serial has been connected, see "8. Block Diagram ".
- The characteristics are only applicable when the relocate port numbers are the same.
  For instance, they are not applicable for the combination of SCLKx_0 and SOTx_1.
- External load capacitance C_L = 30 pF





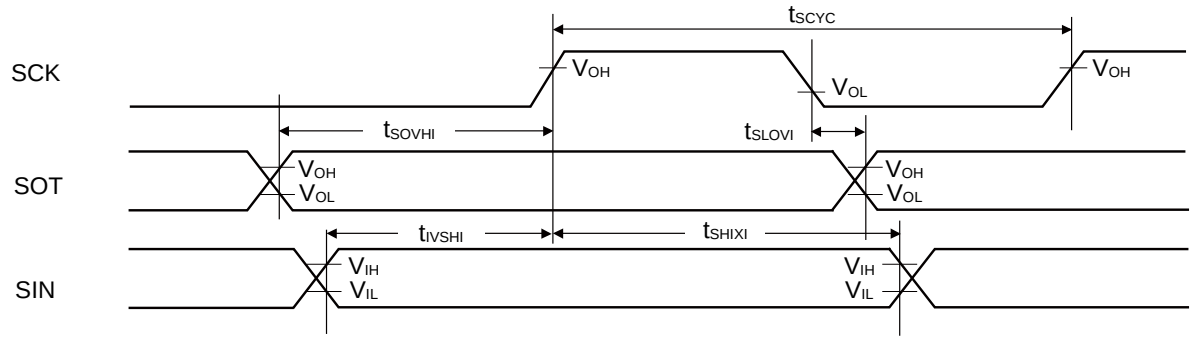
Synchronous serial (SPI = 0, SCINV = 1)

(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

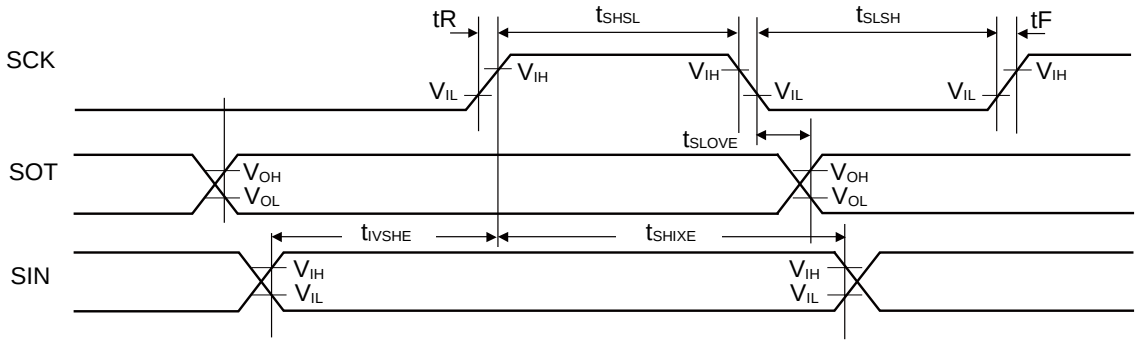
Parameter	Symbol	Pin name	Conditions	V_{CC} < 4.5V		V_{CC} ≥ 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	4 t_{CYCP}	-	4 t_{CYCP}	-	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKx, SINx		50	-	30	-	ns
SCK ↓ → SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	External shift clock operation	2 t_{CYCP} - 10	-	2 t_{CYCP} - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx, SOTx		-	50	-	30	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK ↓ → SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- The above AC characteristics are for CLK synchronous mode.
- t_{CYCP} represents the APB bus clock cycle time.
  For the number of the APB bus to which Multi-function Serial has been connected, see "8. Block Diagram ".
- The characteristics are only applicable when the relocate port numbers are the same.
  For instance, they are not applicable for the combination of SCLKx_0 and SOTx_1.
- External load capacitance C_L = 30 pF



MS bit = 0



MS bit = 1

When using synchronous serial chip select (SPI = 1, SCINV = 1, MS=0, CSLVL=0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5V		V_{CC} ≥ 4.5V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↑ setup time	t_{CSSI}	Internal shift clock operation	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↓→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	ns
SCS↑→SCK↑ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCK↓→SCS↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCS↑→SOT delay time	t_{DSE}		-	40	-	40	ns
SCS↓→SOT delay time	t_{DEE}		0	-	0	-	ns

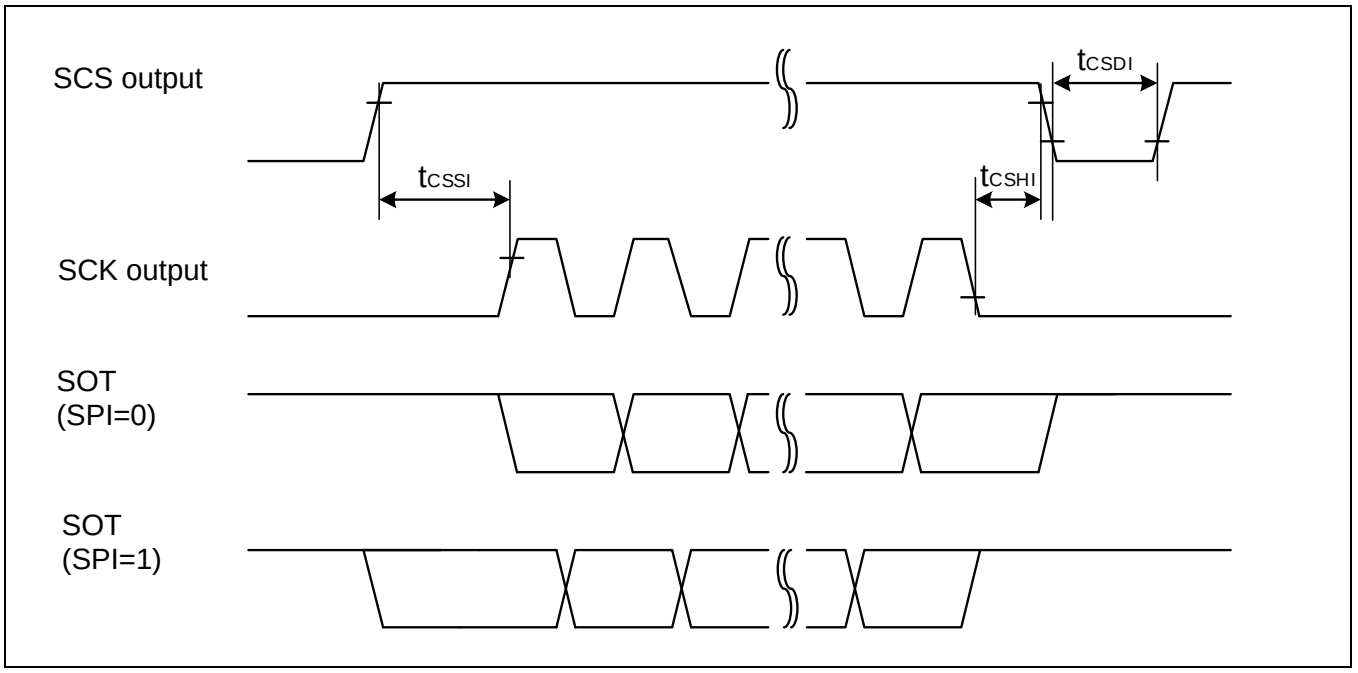
(*1): CSSU bit value × serial chip select timing operating clock cycle [ns]

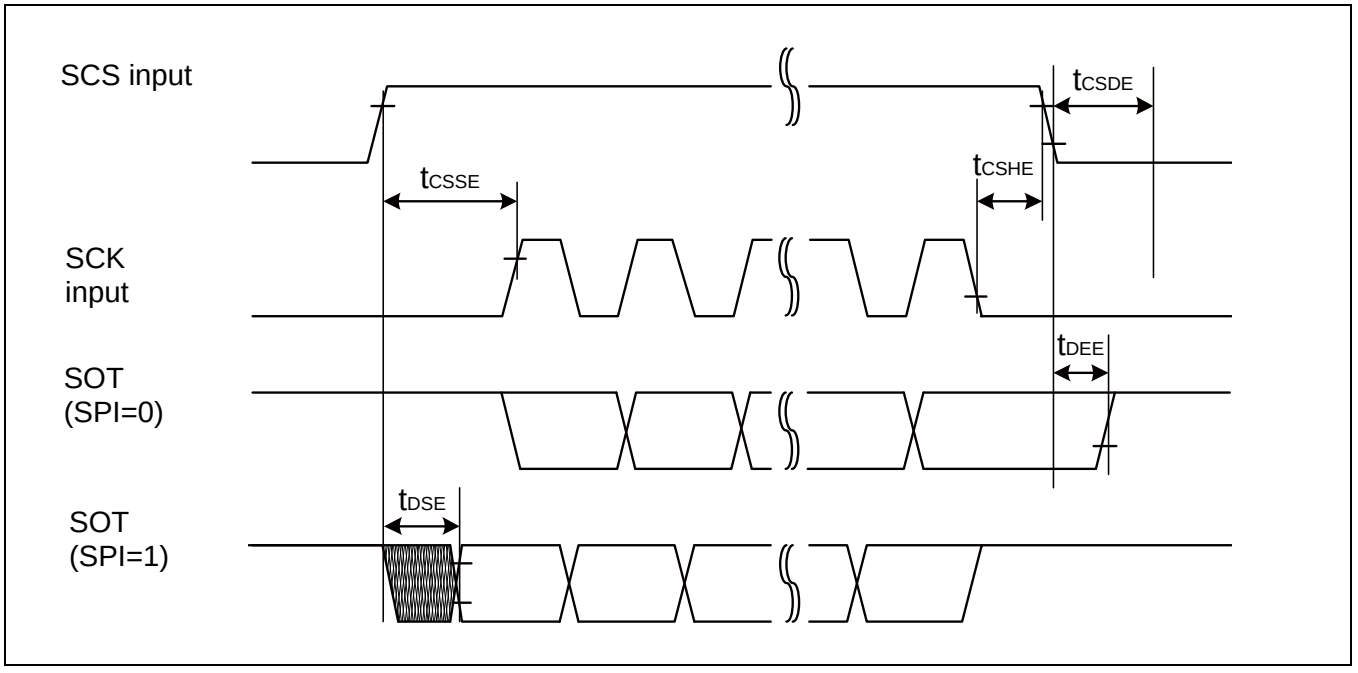
(*2): CSHD bit value × serial chip select timing operating clock cycle [ns]

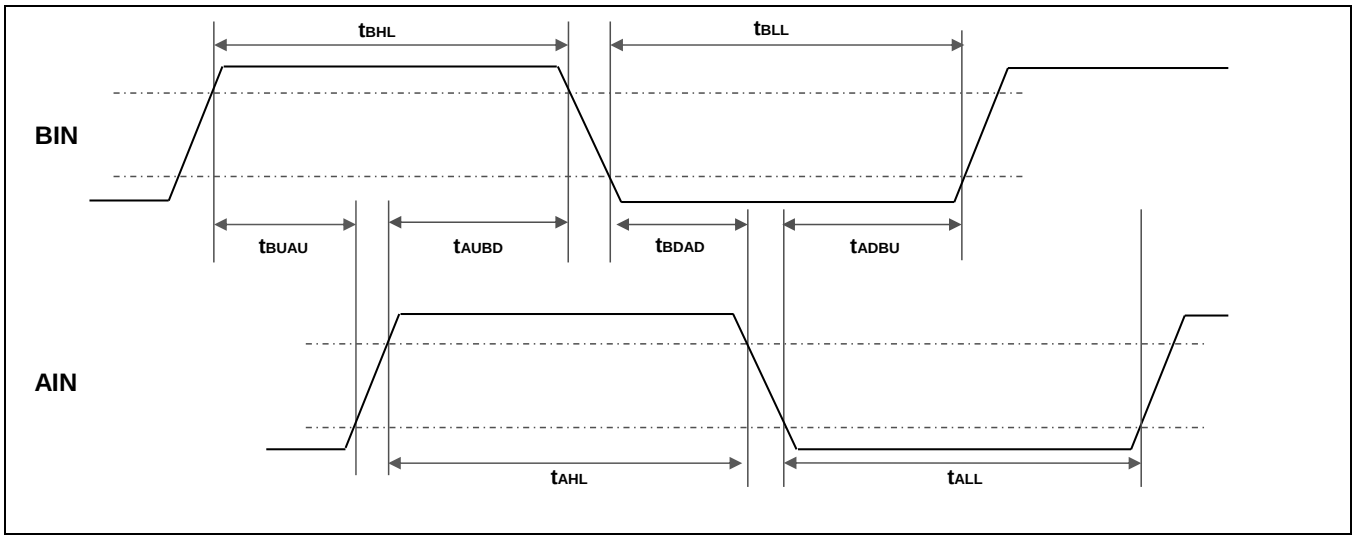
(*3): CSDS bit value × serial chip select timing operating clock cycle [ns]

Notes:

- t_{CYCP} indicates the APB bus clock cycle time.
  About the APB bus number which Multi-function Serial is connected to, see "8. Block Diagram ".
- About CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM0+ Family PERIPHERAL MANUAL".
- When the external load capacitance C_L = 30pF.


SCS output
SCK output
SOT
(SPI=0)
SOT
(SPI=1)
tCSSI
tCSHI
tCSDI


SCS input
SCK
input
SOT
(SPI=0)
SOT
(SPI=1)
tCSSE
tCSHE
tCSDE
tDEE
tDSE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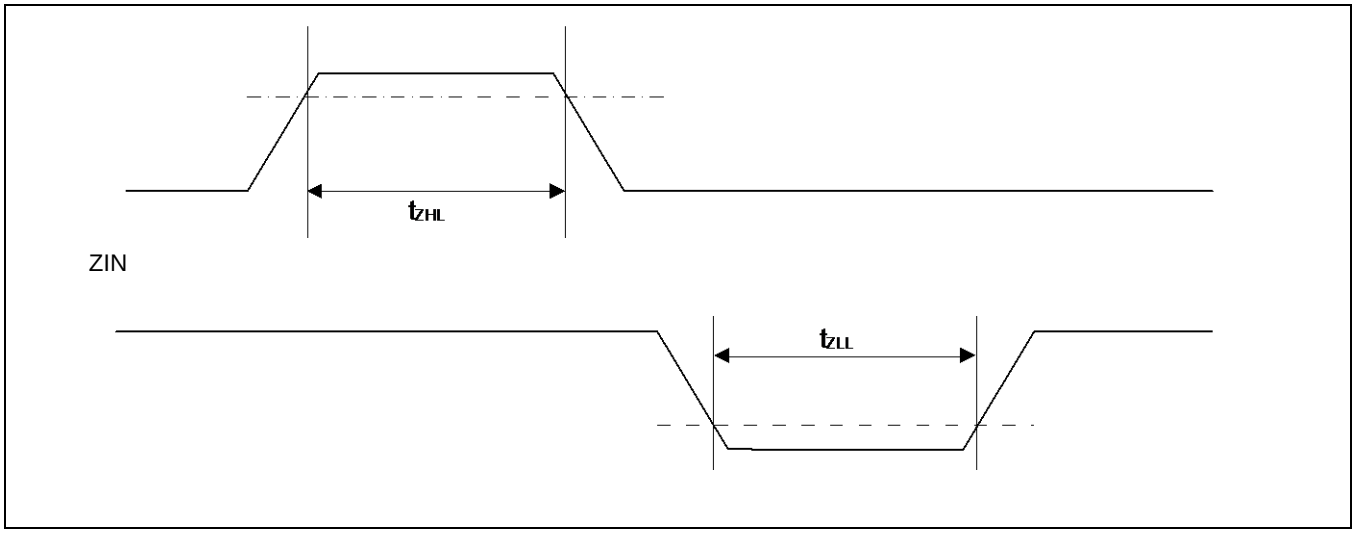
tBLL
BIN
tBUAU
tAUBD
tBDAD
tADBU
AIN
tAHL
tALL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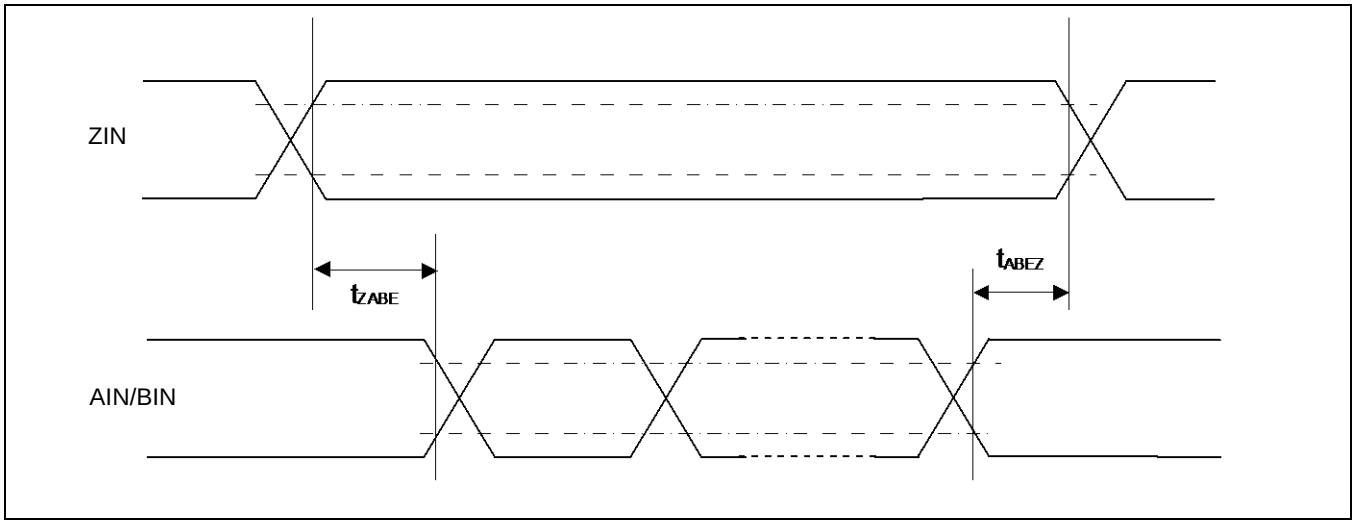
ZIN
tZLL


ZIN
tZABE
tABEZ
AIN/BIN

12.4.12 I^2C Timing

(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

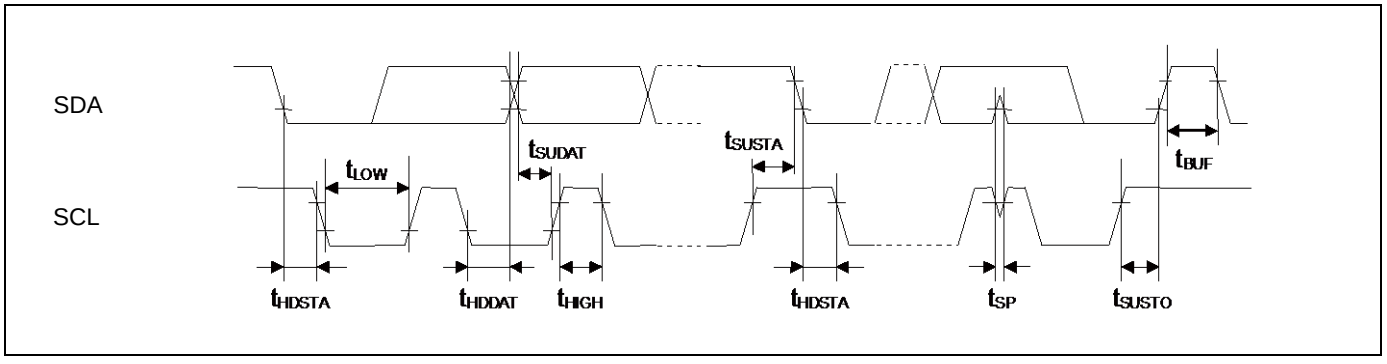
Parameter	Symbol	Conditions	Standard-mode		Fast-mode		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	F_{SCL}	C_L = 30 pF, R = (Vp/I_{OL})*1	0	100	0	400	kHz	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		4.0	-	0.6	-	µs	
SCL clock "L" width	t_{LOW}		4.7	-	1.3	-	µs	
SCL clock "H" width	t_{HIGH}		4.0	-	0.6	-	µs	
(Repeated) START setup time SCL ↑ → SDA ↓	t_{SUSTA}		4.7	-	0.6	-	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45*2	0	0.9*3	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		250	-	100	-	ns	
STOP condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		4.0	-	0.6	-	µs	
Bus free time between "STOP condition" and "START condition"	t_{BUF}		4.7	-	1.3	-	µs	
Noise filter	t_{SP}	-	2 t_{CYCP}*4	-	2 t_{CYCP}*4	-	ns	

*1: R represents the pull-up resistance of the SCL and SDA lines, and C_L the load capacitance of the SCL and SDA lines. Vp represents the power supply voltage of the pull-up resistance, and I_{OL} the V_{OL} guaranteed current.

*2: The maximum t_{HDDAT} must satisfy at least the condition that the period during which the device is holding the SCL signal at "L" (t_{LOW}) does not extend.

*3: A Fast-mode I^2C bus device can be used in a Standard-mode I^2C bus system, provided that the condition of "t_{SUDAT} ≥ 250 ns" is fulfilled.

*4: t_{CYCP} represents the APB bus clock cycle time.
For the number of the APB bus to which the I^2C is connected, see "8. Block Diagram".
To use Standard-mode, set the APB bus clock at 2MHz or more.
To use Fast-mode, set the APB bus clock at 8 MHz or more.



12.6 Low-voltage Detection Characteristics

12.6.1 Low-voltage Detection Reset

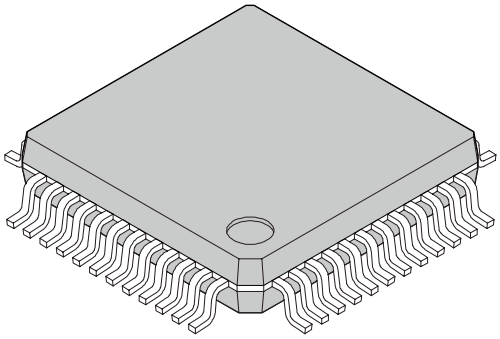
(Ta = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHR[*1] = 00000	2.25	2.45	2.65	V	When voltage drops
Released voltage	VDH		2.30	2.50	2.70	V	When voltage rises
Detected voltage	VDL	SVHR[*1] = 00001	2.39	2.60	2.81	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR[*1] = 00010	2.48	2.70	2.92	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR[*1] = 00011	2.58	2.80	3.02	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR[*1] = 00100	2.76	3.00	3.24	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR[*1] = 00101	2.94	3.20	3.46	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR[*1] = 00110	3.31	3.60	3.89	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR[*1] = 00111	3.40	3.70	4.00	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR[*1] = 01000	3.68	4.00	4.32	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR[*1] = 01001	3.77	4.10	4.43	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR[*1] = 01010	3.86	4.20	4.54	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
LVD stabilization wait time	T_{LVDW}	-	-	-	8160× t_{CYCP}[*2]	µs	
LVD detection delay time	T_{LVDDL}	-	-	-	200	µs	

*1: SVHR bit of Low-Voltage Detection Voltage Control Register (LVD_CTL) is reset to SVHR = 00000 by low voltage detection reset.

*2: t_{CYCP} indicates the APB1 bus clock cycle time.

48-pin plastic LQFP

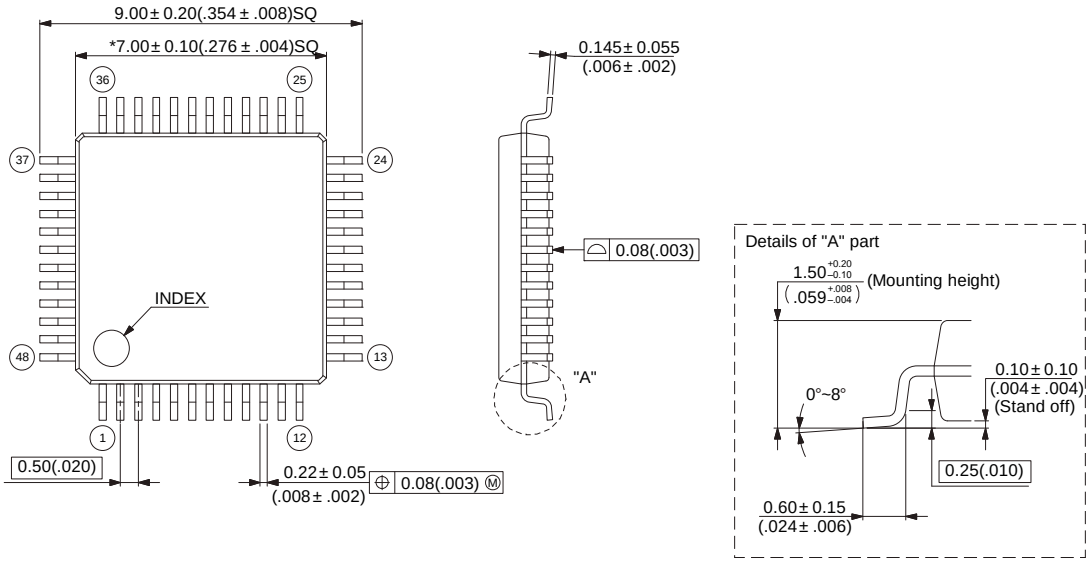


(FPT-48P-M49)

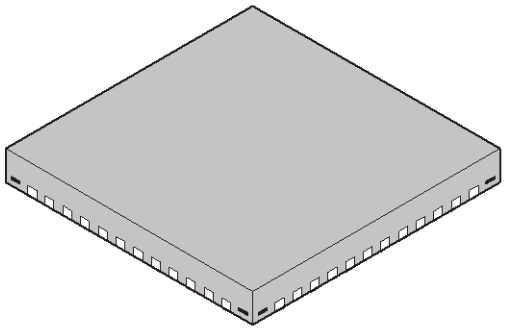
Lead pitch	0.50 mm
Package width × package length	7.00 mm × 7.00 mm
Lead shape	Gullwing
Lead bend direction	Normal bend
Sealing method	Plastic mold
Mounting height	1.70 mm MAX
Weight	0.17 g

48-pin plastic LQFP
(FPT-48P-M49)

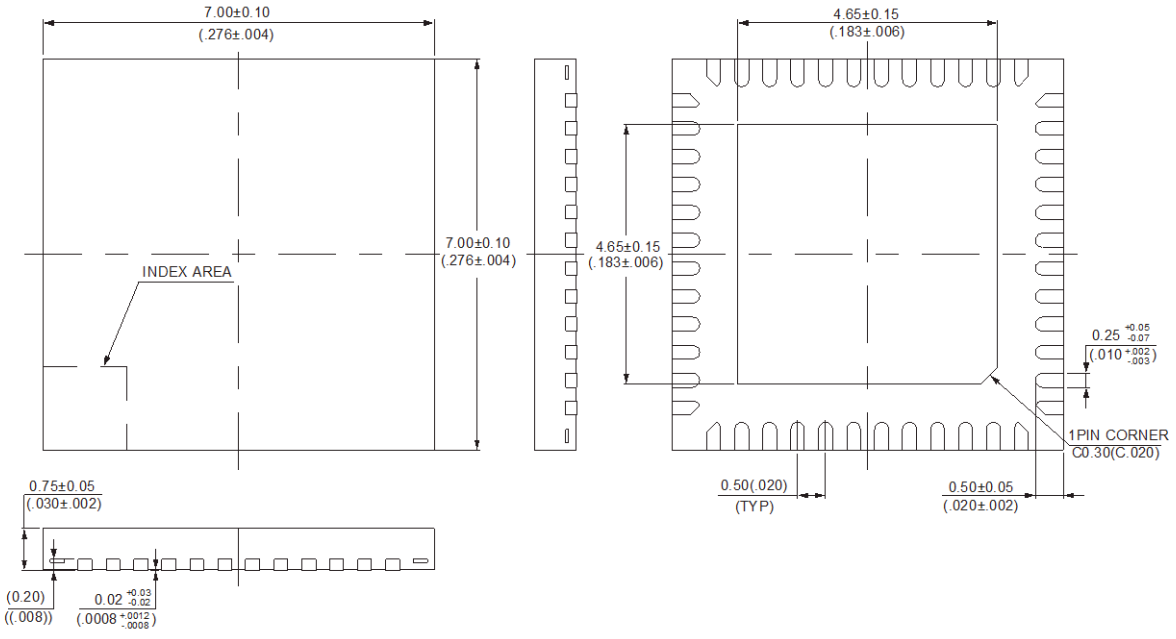
Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

48-pin plastic QFN		
 (LCC-48P-M74)	Lead pitch	0.50 mm
	Package width× package length	7.00 mm × 7.00 mm
	Sealing method	Plastic mold
	Mounting height	0.80 mm MAX
	Weight	0.12 g

48-pin plastic QFN
(LCC-48P-M74)



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

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