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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CSIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	23
Program Memory Size	88KB (88K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 5x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-WFQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e1a12b0agn20000

2. Packages

Product name / Package	S6E1A11B0A S6E1A12B0A	S6E1A11C0A S6E1A12C0A
LQFP: FPT-32P-M30 (0.80 mm pitch)	❍	-
QFN: LCC-32P-M73 (0.50 mm pitch)	❍	-
LQFP: FPT-48P-M49 (0.50 mm pitch)	-	❍
QFN: LCC-48P-M74 (0.50 mm pitch)	-	❍
LQFP: FPT-52P-M02 (0.65 mm pitch)	-	❍

❍: Supported

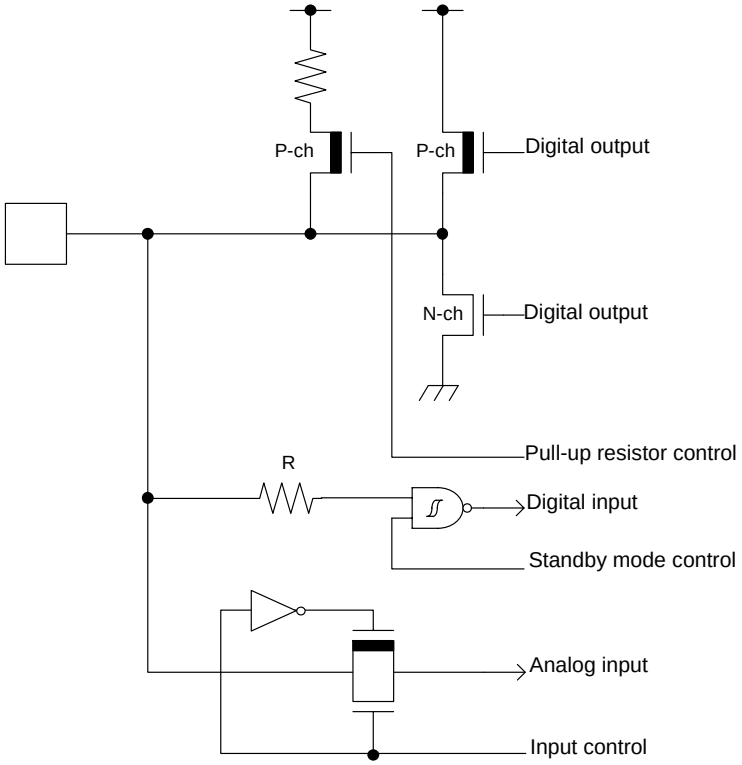
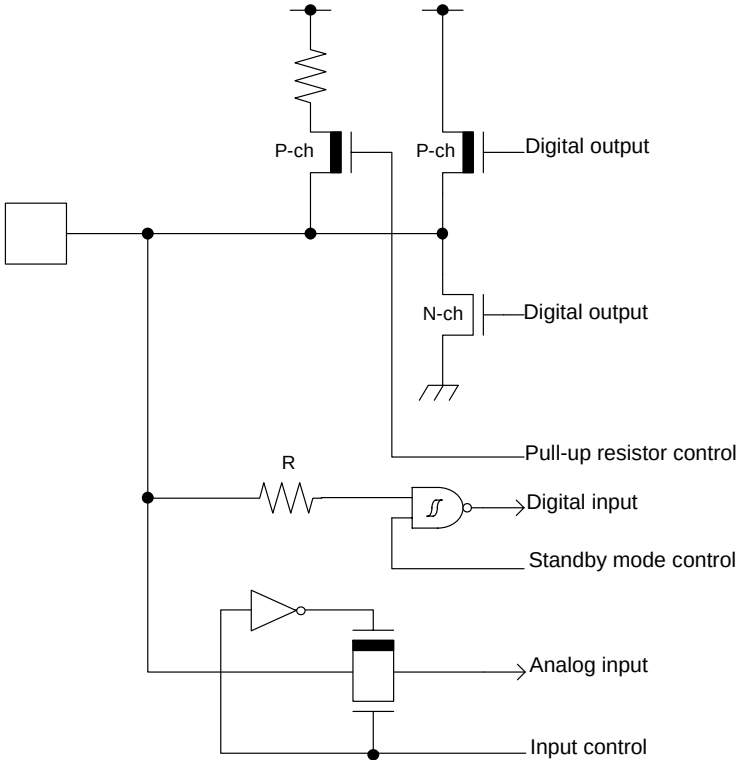
Note:

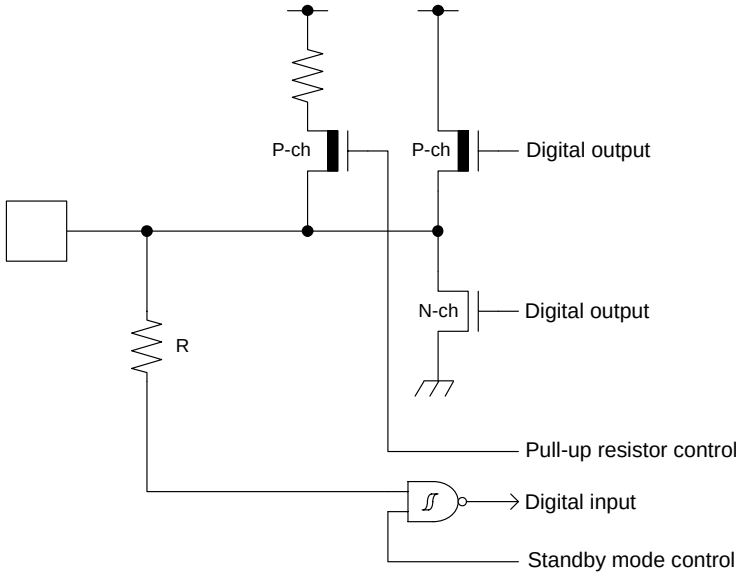
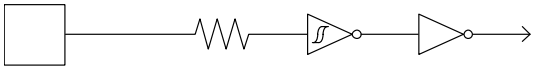
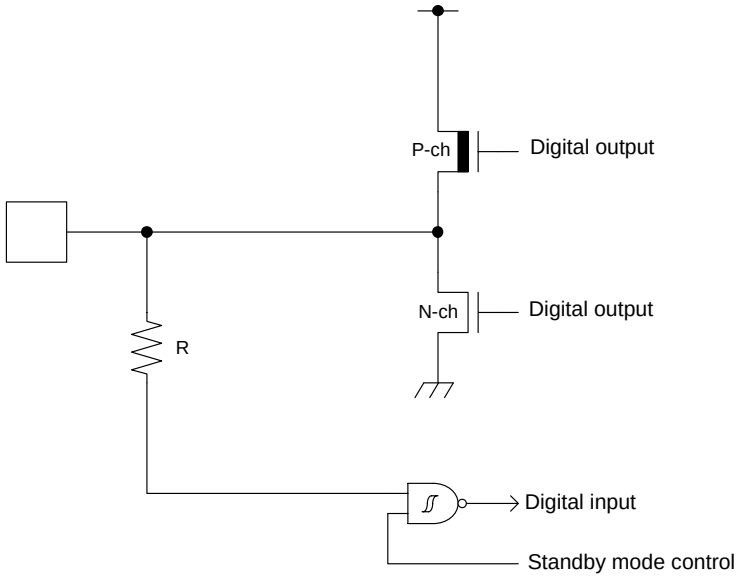
- See "14. Package Dimensions" for detailed information on each package.

List of pin functions

The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.

Pin function	Pin name	Function description	Pin no.		
			LQFP-52	LQFP-48 QFN-48	LQFP-32 QFN-32
ADC	ADTG_1	A/D converter external trigger input pin	22	20	13
	ADTG_2		6	5	-
	AN00	A/D converter analog input pin. ANxx describes ADC ch.xx.	27	25	-
	AN01		28	26	18
	AN02		29	27	19
	AN03		30	28	20
	AN04		31	29	-
	AN05		32	30	-
	AN06		37	34	23
	AN07		38	35	24
Base Timer 0	TIOA0_0	Base timer ch.0 TIOA pin	11	10	5
	TIOA0_1		7	6	1
	TIOB0_0	Base timer ch.0 TIOB pin	19	18	-
	TIOB0_1		45	41	28
Base Timer 1	TIOA1_0	Base timer ch.1 TIOA pin	12	11	6
	TIOA1_1		8	7	2
	TIOB1_0	Base timer ch.1 TIOB pin	20	19	-
	TIOB1_1		39	36	25
Base Timer 2	TIOA2_0	Base timer ch.2 TIOA pin	37	34	23
	TIOA2_1		9	8	3
	TIOA2_2		48	44	31
	TIOB2_0	Base timer ch.2 TIOB pin	38	35	24
	TIOB2_2		47	43	30
Base Timer 3	TIOA3_1	Base timer ch.3 TIOA pin	10	9	4
Debugger	SWCLK	Serial wire debug interface clock input pin	42	38	26
	SWDIO	Serial wire debug interface data input / output pin	44	40	27

Type	Circuit	Remarks
G		• CMOS level output • CMOS level hysteresis input • With input control • Analog input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50kΩ • I_{OH}= -4mA, I_{OL}= 4mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off
H		• CMOS level output • CMOS level hysteresis input • With input control • Analog input • 5V tolerant • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50kΩ • I_{OH}= -4mA, I_{OL}= 4mA • Available to control of PZR registers. • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off

Type	Circuit	Remarks
I		• CMOS level output • CMOS level hysteresis input • 5V tolerant • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50kΩ • I_{OH}= -4mA, I_{OL}= 4mA • Available to control PZR registers • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off
J		CMOS level hysteresis input
K		• CMOS level output • CMOS level hysteresis input • With standby mode control • I_{OH}= -4mA, I_{OL}= 4mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off

6.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity

   Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

2. Discharge of Static Electricity

   When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

3. Corrosive Gases, Dust, or Oil

   Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

4. Radiation, Including Cosmic Radiation

   Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

5. Smoke, Flame

   CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

Notes on Power-on

Turn power on/off in the following order or at the same time.

Turning on : VBAT → VCC
VCC → AVCC → AVRH
Turning off : VCC → VBAT
AVRH → AVCC → VCC

Serial Communication

There is a possibility to receive wrong data due to the noise or other causes on the serial communication.
Therefore, design a printed circuit board so as to avoid noise.

Consider the case of receiving wrong data due to noise, perform error detection such as by applying a checksum of data at the end.
If an error is detected, retransmit the data.

Differences in Features among the Products with Different Memory Sizes and between Flash Products and MASK Products

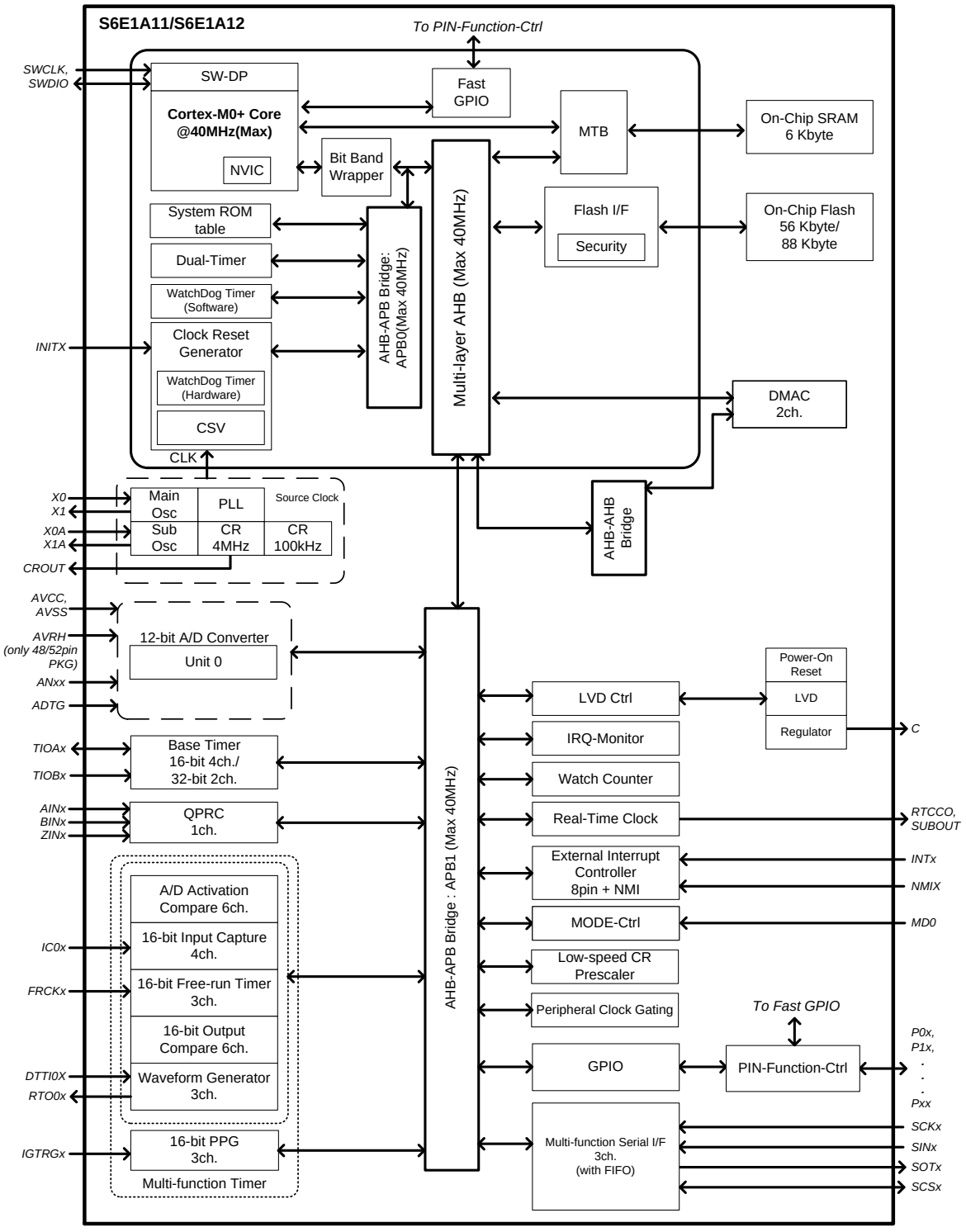
The electric characteristics including power consumption, ESD, latch-up, noise characteristics, and oscillation characteristics among the products with different memory sizes and between Flash products and MASK products are different because chip layout and memory structures are different.

If you are switching to use a different product of the same series, please make sure to evaluate the electric characteristics.

Pull-Up Function of 5V Tolerant I/O

Please do not input the signal more than VCC voltage at the time of Pull-Up function use of 5V tolerant I/O.

8. Block Diagram



List of Pin Status

Pin status type	Function group	State upon power-on reset or low-voltage detection	State at INITX input	State upon device internal reset	State in Run mode or SLEEP mode	State in TIMER mode, RTC mode, or STOP mode	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable	
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1	
		-	-	-	-	SPL = 0	SPL = 1
A	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"
	Main crystal oscillator input pin/ External main clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
B	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"
	External main clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"
	Main crystal oscillator output pin	Hi-Z / Internal input fixed at "0"/ Input enabled	Hi-Z / Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	Maintain previous state/When oscillation stops*[1], Hi-Z / Internal input fixed at "0"	Maintain previous state/When oscillation stops*[1], Hi-Z / Internal input fixed at "0"	Maintain previous state/When oscillation stops*[1], Hi-Z / Internal input fixed at "0"
C	INITX input pin	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled
D	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
E	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"
	Sub crystal oscillator input pin / External sub clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
F	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"
	External sub clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"

LVD current

(V_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Low-Voltage detection circuit (LVD) power supply current	I_{CCLVD}	VCC	At operation	0.13	0.3	µA	For occurrence of reset
				0.13	0.3	µA	For occurrence of interrupt

Flash memory current

(V_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Flash memory write/erase current	$I_{CCFLASH}$	VCC	At Write/Erase	9.5	11.2	mA	

A/D convertor current (S6E1A1xC0A)

(V_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Power supply current	I_{CCAD}	AVCC	At operation	0.7	0.9	mA	
			At stop	0.13	13	µA	
Reference power supply current (AVRH)	I_{CCAVRH}	AVRH	At operation	1.1	1.97	mA	AVRH=5.5V
			At stop	0.1	1.7	µA	

A/D convertor current (S6E1A1xB0A)

(V_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Power supply current	I_{CCAD}	AVCC	At operation	1.8	2.87	mA	
			At stop	0.23	14.7	µA	

Peripheral current dissipation

Clock system	Peripheral	Conditions	Frequency (MHz)				Unit	Remarks
			4	8	20	40		
HCLK	GPIO	At all ports operation	0.11	0.22	0.55	1.10	mA	
	DMAC	At 2ch operation	0.05	0.11	0.25	0.51		
PCLK1	Base timer	At 4ch operation	0.03	0.05	0.15	0.30	mA	
	Multi-functional timer/PPG	At 1unit/4ch operation	0.14	0.28	0.68	1.38		
	Quadrature position/Revolution counter	At 1unit operation	0.02	0.04	0.11	0.22		
	ADC	At 1unit operation	0.07	0.14	0.37	0.73		
	Multi-function serial	At 1ch operation	0.15	0.31	0.77	1.54		

12.4 AC Characteristics

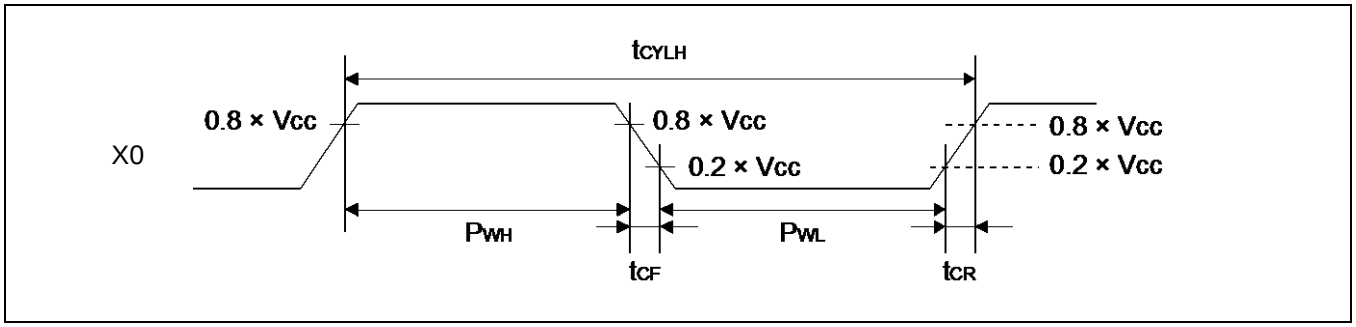
12.4.1 Main Clock Input Characteristics

(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	F_{CH}	X0, X1	V_{CC} ≥ 4.5V	4	40	MHz	When the crystal oscillator is connected
			V_{CC} < 4.5V	4	20		
			-	4	40	MHz	When the external clock is used
Input clock cycle	t_{CYLH}		-	25	250	ns	When the external clock is used
Input clock pulse width	-		P_{WH}/t_{CYLH}, P_{WL}/t_{CYLH}	45	55	%	When the external clock is used
Input clock rising time and falling time	t_{CF}, t_{CR}		-	-	5	ns	When the external clock is used
Internal operating clock*1 frequency	F_{CM}	-	-	-	41.2	MHz	Master clock
	F_{CC}	-	-	-	41.2	MHz	Base clock (HCLK/FCLK)
	F_{CP0}	-	-	-	41.2	MHz	APB0 bus clock*2
	F_{CP1}	-	-	-	41.2	MHz	APB1 bus clock*2
Internal operating clock*1 cycle time	t_{CYCC}	-	-	24.27	-	ns	Base clock (HCLK/FCLK)
	t_{CYCP0}	-	-	24.27	-	ns	APB0 bus clock*2
	t_{CYCP1}	-	-	24.27	-	ns	APB1 bus clock*2

*1: For details of each internal operating clock, refer to "CHAPTER: Clock" in "FM0+ Family PERIPHERAL MANUAL".

*2: For details of the APB bus to which a peripheral is connected, see "8. Block Diagram".

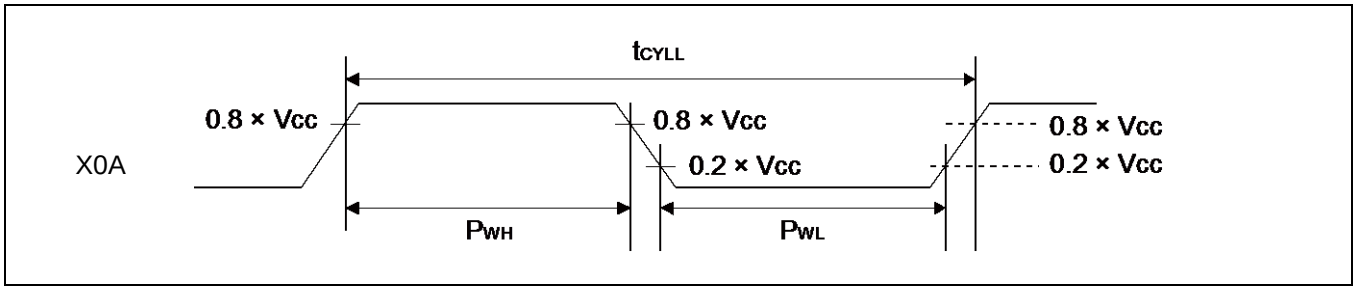


12.4.2 Sub Clock Input Characteristics

(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	$1/t_{CYLL}$	X0A, X1A	-	-	32.768	-	kHz	When the crystal oscillator is connected
			-	32	-	100	kHz	When the external clock is used
Input clock cycle	t_{CYLL}		-	10	-	31.25	µs	When the external clock is used
Input clock pulse width	-		P_{WH}/t_{CYLL}, P_{WL}/t_{CYLL}	45	-	55	%	When the external clock is used

*: See "Sub crystal oscillator" in "7. Handling Devices" for the crystal oscillator used.



12.4.4 Operating Conditions of Main PLL (In the case of using the main clock as the input clock of the PLL)

(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	F_{PLLI}	4	-	16	MHz	
PLL multiple rate	-	5	-	37	multiple	
PLL macro oscillation clock frequency	F_{PLLO}	75	-	150	MHz	
Main PLL clock frequency*2	F_{CLKPLL}	-	-	40	MHz	

*1: The wait time is the time it takes for PLL oscillation to stabilize.

*2: For details of the main PLL clock (CLKPLL), refer to "CHAPTER: Clock" in "FM0+ Family PERIPHERAL MANUAL".

12.4.5 Operating Conditions of Main PLL (In the case of using the built-in high-speed CR clock as the input clock of the main PLL)

(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	F_{PLLI}	3.88	4	4.12	MHz	
PLL multiple rate	-	19	-	35	multiple	
PLL macro oscillation clock frequency	F_{PLLO}	72	-	150	MHz	
Main PLL clock frequency*2	F_{CLKPLL}	-	-	41.2	MHz	

*1: The wait time is the time it takes for PLL oscillation to stabilize.

*2: For details of the main PLL clock (CLKPLL), refer to "CHAPTER: Clock" in "FM0+ Family PERIPHERAL MANUAL".

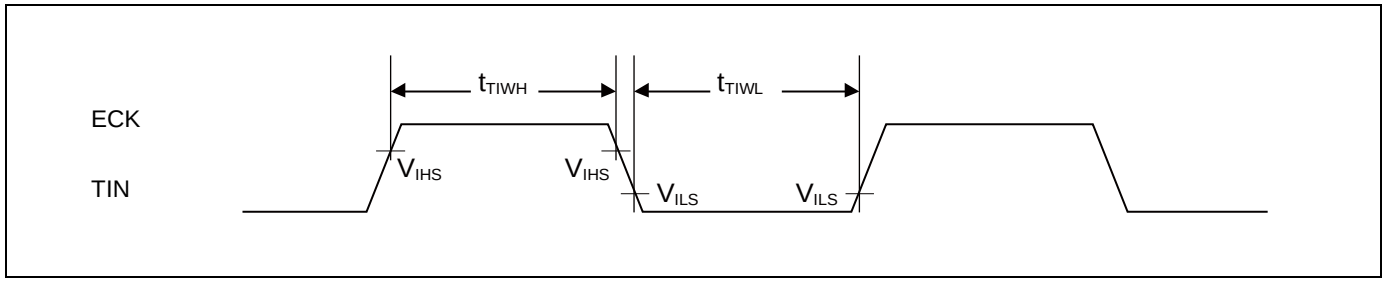
Note:
For the main PLL source clock, input the high-speed CR clock (CLKHC) whose frequency has been trimmed.

12.4.8 Base Timer Input Timing

Timer input timing

(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

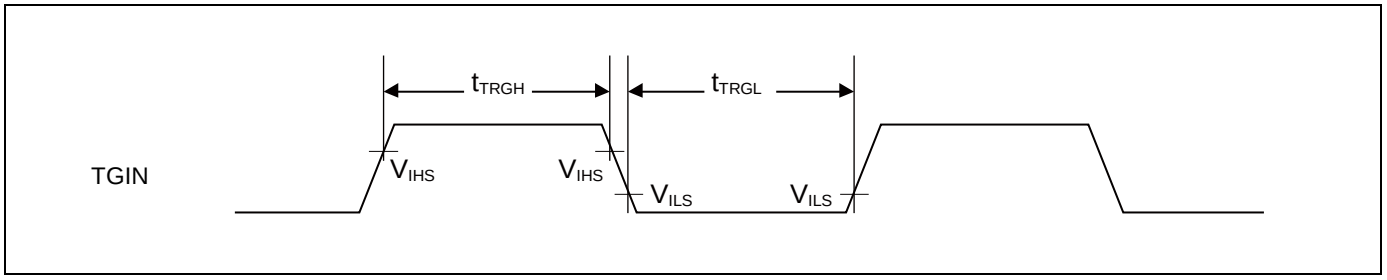
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}, t_{TIWL}	TIOAn/TIOBn (when using as ECK, TIN)	-	2 t_{CYCP}	-	ns	



Trigger input timing

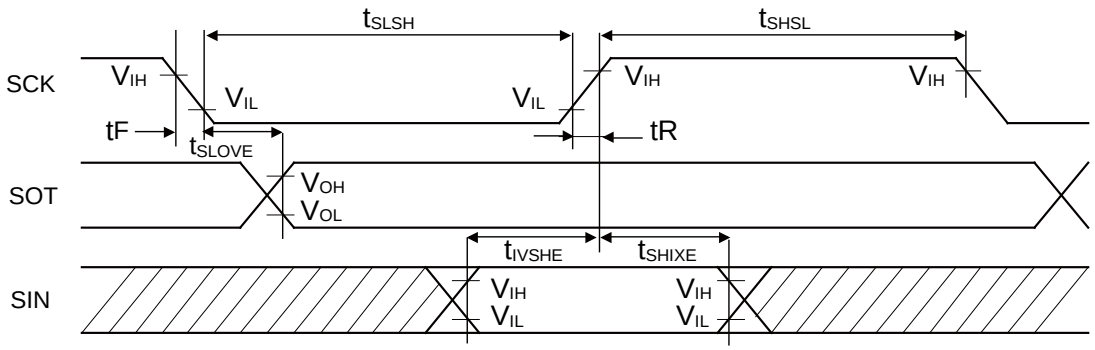
(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	TIOAn/TIOBn (when using as TGIN)	-	2 t_{CYCP}	-	ns	



Note:

- t_{CYCP} indicates the APB bus clock cycle time.
  For the number of the APB bus to which the Base Timer has been connected, see "8. Block Diagram".



Synchronous serial (SPI = 0, SCINV = 1)

(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	V_{CC} < 4.5V		V_{CC} ≥ 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	4 t_{CYCP}	-	4 t_{CYCP}	-	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKx, SINx		50	-	30	-	ns
SCK ↓ → SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	External shift clock operation	2 t_{CYCP} - 10	-	2 t_{CYCP} - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx, SOTx		-	50	-	30	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK ↓ → SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- The above AC characteristics are for CLK synchronous mode.
- t_{CYCP} represents the APB bus clock cycle time.
  For the number of the APB bus to which Multi-function Serial has been connected, see "8. Block Diagram ".
- The characteristics are only applicable when the relocate port numbers are the same.
  For instance, they are not applicable for the combination of SCLKx_0 and SOTx_1.
- External load capacitance C_L = 30 pF

When using synchronous serial chip select (SPI = 1, SCINV = 0, MS=0, CSLVL=0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5V		V_{CC} ≥ 4.5V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↓ setup time	t_{CSSI}	Internal shift clock operation	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↑→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	ns
SCS↑→SCK↓ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCK↑→SCS↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCS↑→SOT delay time	t_{DSE}		-	40	-	40	ns
SCS↓→SOT delay time	t_{DEE}		0	-	0	-	ns

(*1): CSSU bit value × serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value × serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value × serial chip select timing operating clock cycle [ns]

Notes:

- t_{CYCP} indicates the APB bus clock cycle time.
  About the APB bus number which Multi-function Serial is connected to, see "8. Block Diagram ".
- About CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM0+ Family PERIPHERAL MANUAL".
- When the external load capacitance C_L = 30pF.

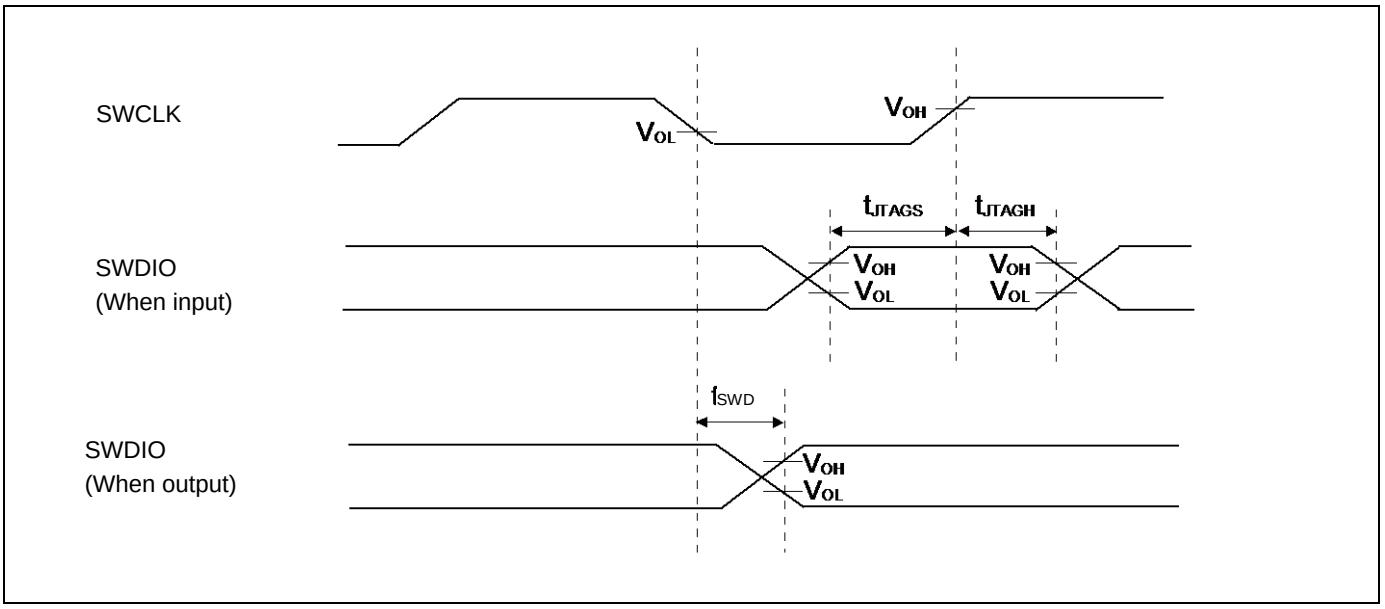
12.4.13 SW-DP Timing

(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SWDIO setup time	t_{SWS}	SWCLK, SWDIO	-	15	-	ns	
SWDIO hold time	t_{SWH}	SWCLK, SWDIO	-	15	-	ns	
SWDIO delay time	t_{SWD}	SWCLK, SWDIO	-	-	45	ns	

Note:

- External load capacitance C_L = 30 pF



12.6.2 Low-voltage Detection Interrupt

(Ta = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHI = 00011	2.58	2.80	3.02	V	When voltage drops
Released voltage	VDH		2.67	2.90	3.13	V	When voltage rises
Detected voltage	VDL	SVHI = 00100	2.76	3.00	3.24	V	When voltage drops
Released voltage	VDH		2.85	3.10	3.35	V	When voltage rises
Detected voltage	VDL	SVHI = 00101	2.94	3.20	3.46	V	When voltage drops
Released voltage	VDH		3.04	3.30	3.56	V	When voltage rises
Detected voltage	VDL	SVHI = 00110	3.31	3.60	3.89	V	When voltage drops
Released voltage	VDH		3.40	3.70	4.00	V	When voltage rises
Detected voltage	VDL	SVHI = 00111	3.40	3.70	4.00	V	When voltage drops
Released voltage	VDH		3.50	3.80	4.10	V	When voltage rises
Detected voltage	VDL	SVHI = 01000	3.68	4.00	4.32	V	When voltage drops
Released voltage	VDH		3.77	4.10	4.43	V	When voltage rises
Detected voltage	VDL	SVHI = 01001	3.77	4.10	4.43	V	When voltage drops
Released voltage	VDH		3.86	4.20	4.54	V	When voltage rises
Detected voltage	VDL	SVHI = 01010	3.86	4.20	4.54	V	When voltage drops
Released voltage	VDH		3.96	4.30	4.64	V	When voltage rises
LVD stabilization wait time	T_{LVDW}	-	-	-	8160 × t_{CYCP}*	µs	
LVD detection delay time	T_{LVDDL}	-	-	-	200	µs	

*:t_{CYCP} represents the APB1 bus clock cycle time.

12.8.2 Return Factor: Reset

The return time from Low-Power consumption mode is indicated as follows. It is from releasing reset to starting the program operation.

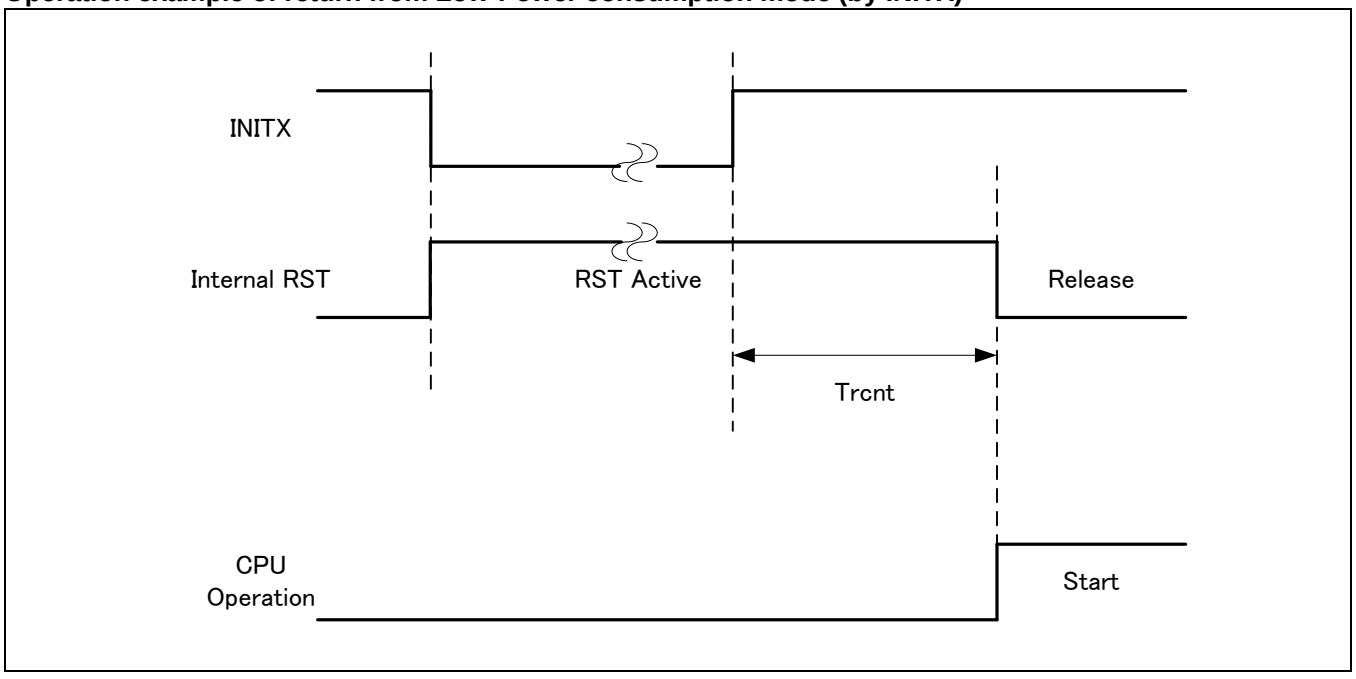
Return Count Time

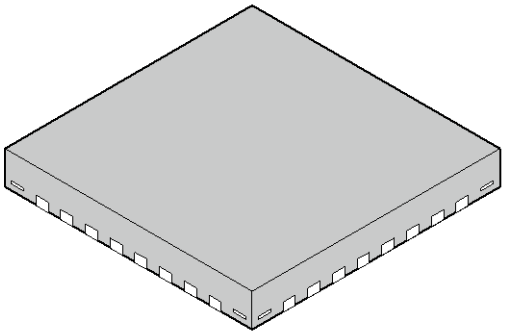
(V_{CC} = 2.7V to 5.5V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
SLEEP mode	Trcnt	208	378	µs	
High-speed CR TIMER mode, Main TIMER mode, PLL TIMER mode		208	378	µs	
Low-speed CR TIMER mode		398	758	µs	
Sub TIMER mode		490	849	µs	
RTC/STOP mode		288	538	µs	

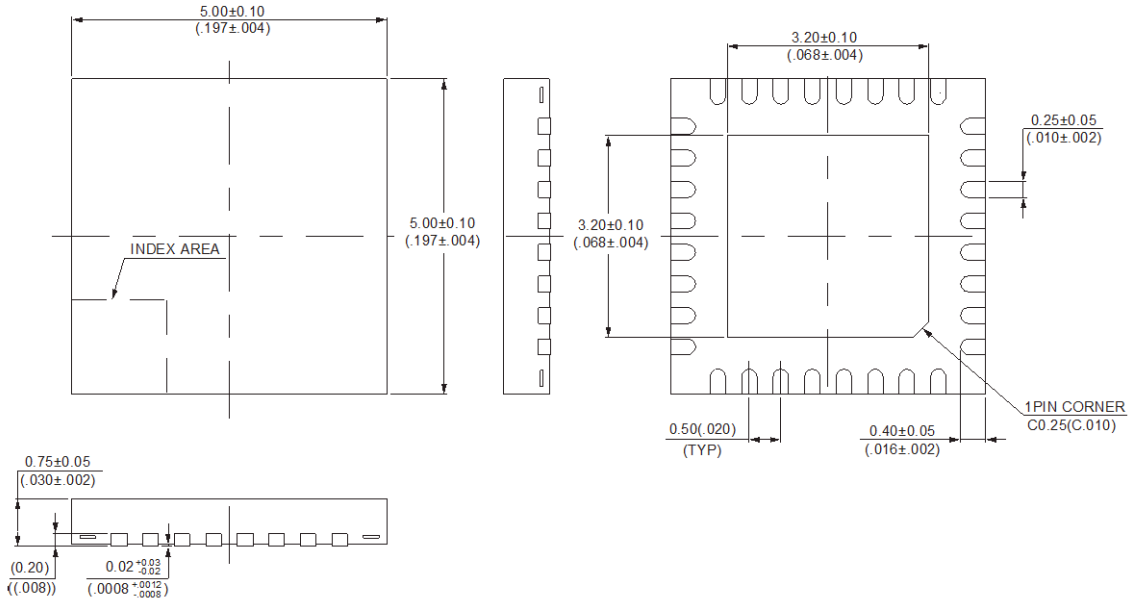
*: The maximum value depends on the accuracy of built-in CR.

Operation example of return from Low-Power consumption mode (by INITX)

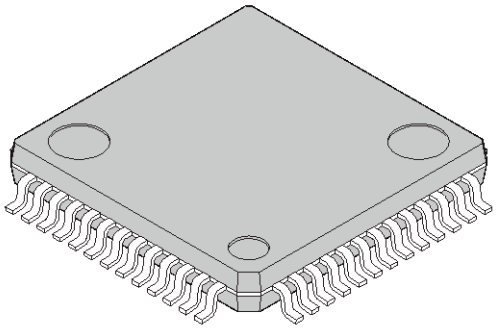


32-pin plastic QFN		
 (LCC-32P-M73)	Lead pitch	0.50 mm
	Package width × package length	5.00 mm × 5.00 mm
	Sealing method	Plastic mold
	Mounting height	0.80 mm MAX
	Weight	0.06 g

32-pin plastic QFN
(LCC-32P-M73)

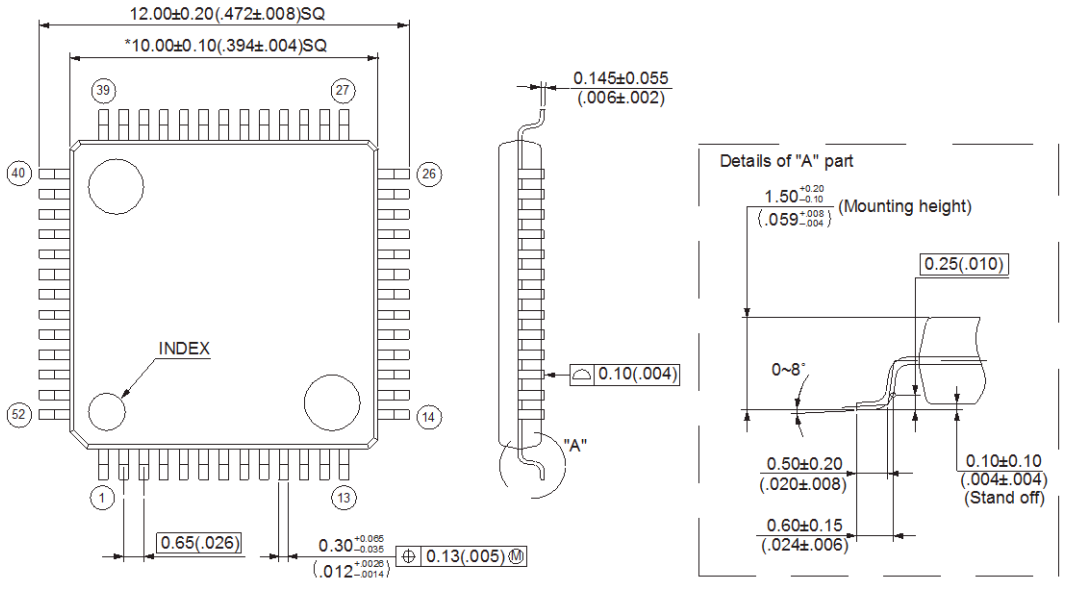


Dimensions in mm (inches).
Note: The values in parentheses are reference values.

52-pin plastic LQFP		
	Lead pitch	0.65 mm
	Package width × package length	10.00 × 10.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.32 g
(FPT-52P-M02)	Code (Reference)	P-LFQFP52-10 × 10-0.65

52-pin plastic LQFP
(FPT-52P-M02)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values