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What is "Embedded - Microcontrollers"?

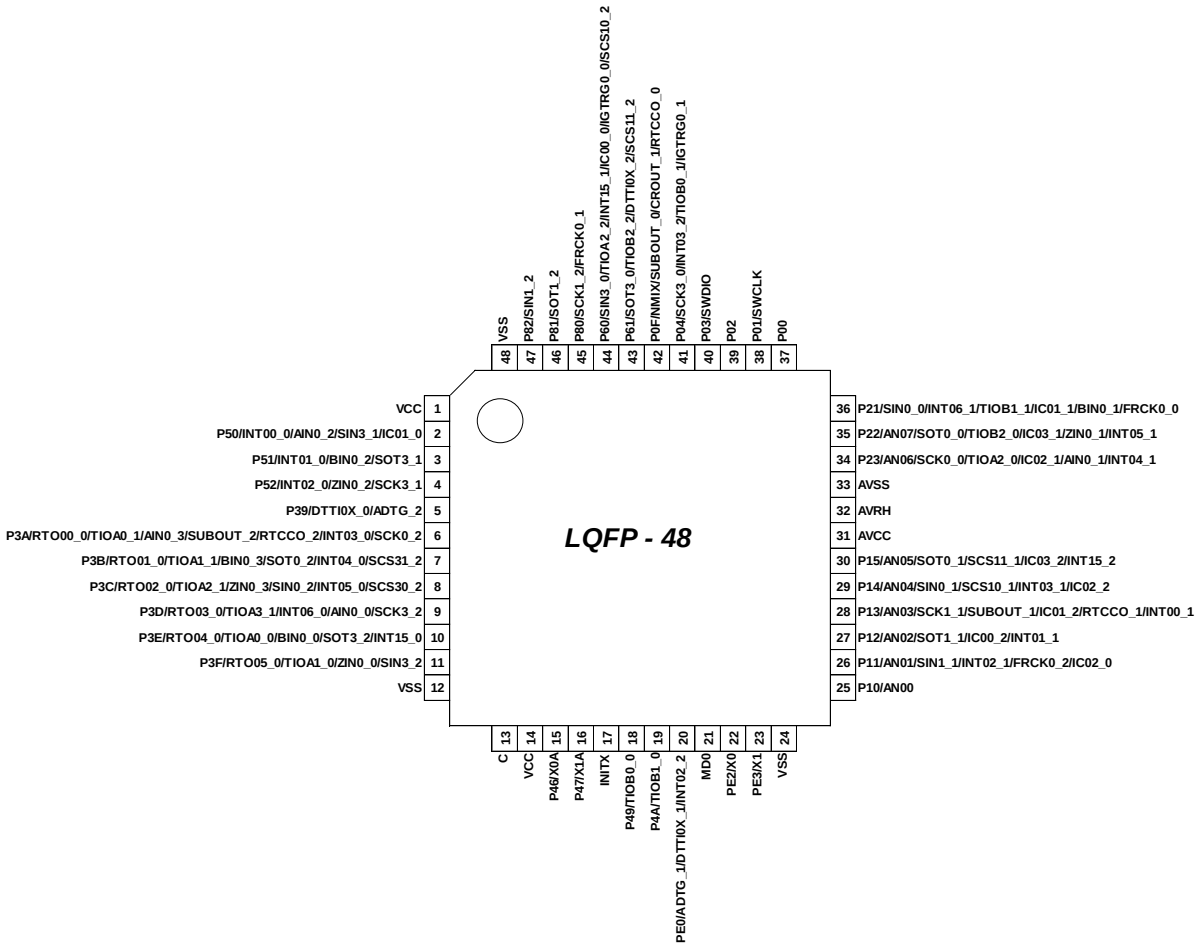
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CSIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	23
Program Memory Size	88KB (88K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 5x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-WFQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e1a12b0agn2b000

FPT-48P-M49

(TOP VIEW)

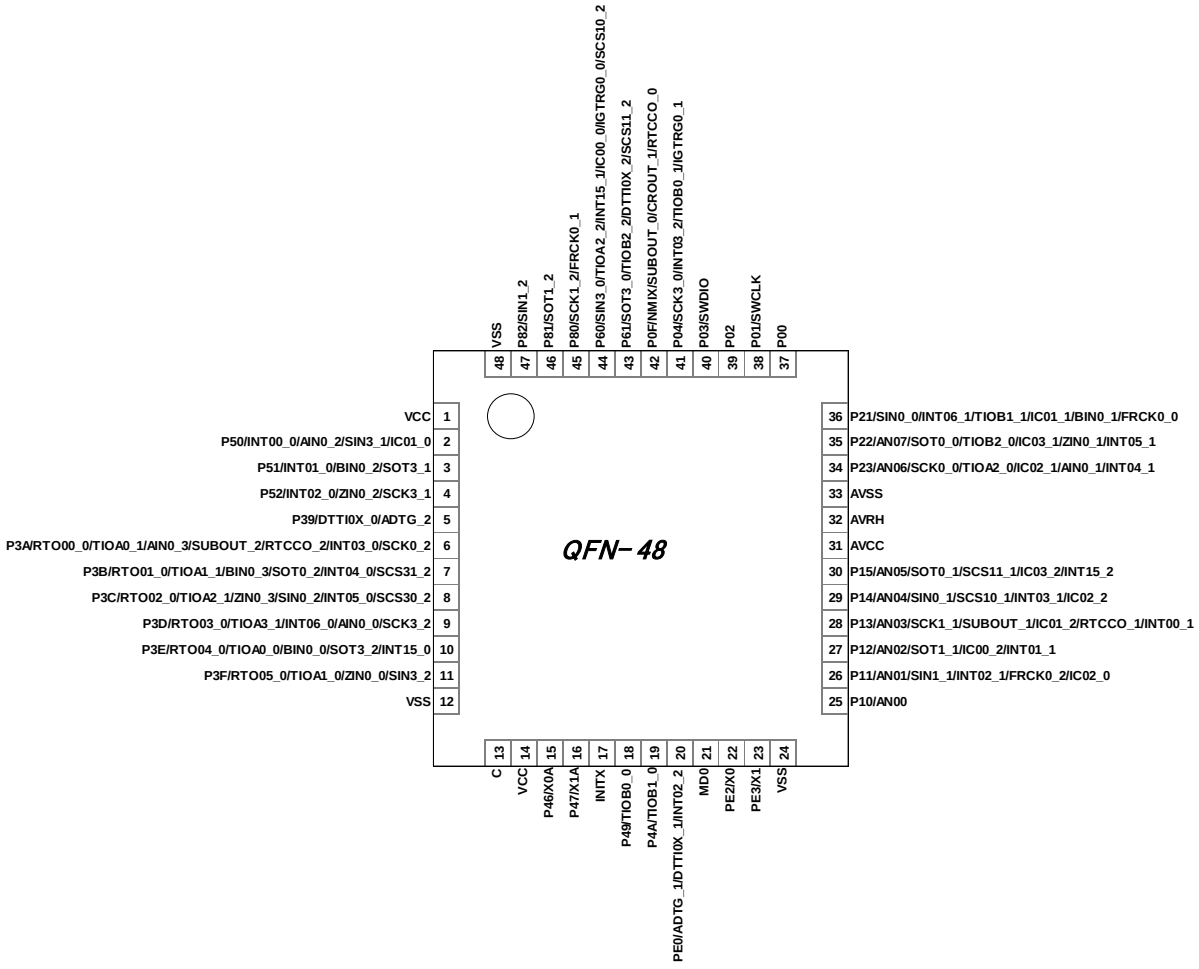


Note:

- The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.
  Use the extended port function register (EPFR) to select the pin.

LCC-48P-M74

(TOP VIEW)



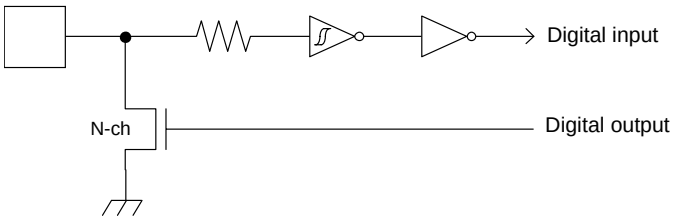
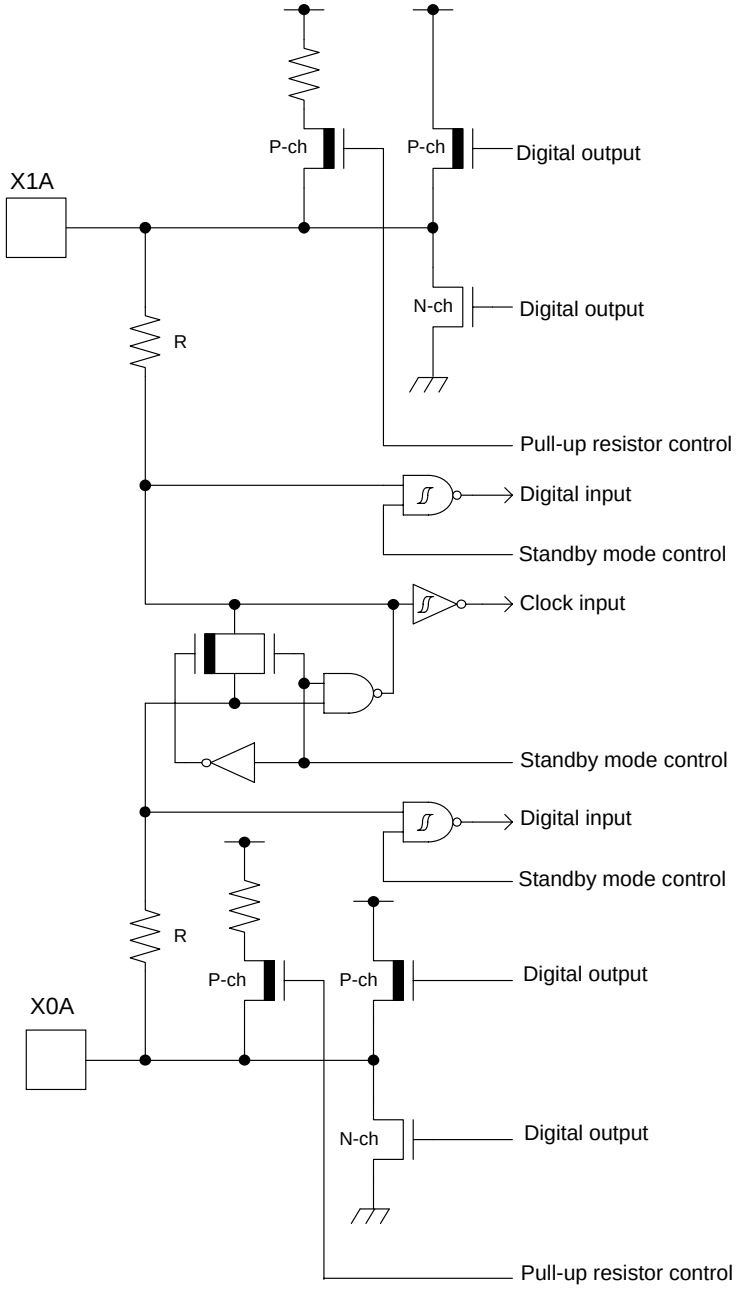
Note:

- The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.
  Use the extended port function register (EPFR) to select the pin.

Pin no.			Pin name	I/O circuit type	Pin state type
LQFP-52	LQFP-48 QFN-48	LQFP-32 QFN-32			
32	30	-	P15 AN05 SOT0_1 SCS11_1 IC03_2 INT15_2	H*	L
33	31	21	AVCC	-	
34	32	-	AVRH	-	
35	33	22	AVSS	-	
37	34	23	P23 AN06 SCK0_0 TIOA2_0 IC02_1 AIN0_1 INT04_1	G	L
38	35	24	P22 AN07 SOT0_0 TIOB2_0 IC03_1 ZIN0_1 INT05_1	G	L
39	36	25	P21 SIN0_0 INT06_1 TIOB1_1 IC01_1 BIN0_1 FRCK0_0	E	J
41	37	-	P00	E	I
42	38	26	P01 SWCLK	E	H
43	39	-	P02	E	I
44	40	27	P03 SWDIO	E	H

Pin no.			Pin name	I/O circuit type	Pin state type
LQFP-52	LQFP-48 QFN-48	LQFP-32 QFN-32			
45	41	28	P04 SCK3_0 INT03_2 TIOB0_1 IGTRG0_1	I*	J
46	42	29	P0F NMIX SUBOUT_0 CROUT_1 RTCCO_0	E	G
47	43	30	P61 SOT3_0 TIOB2_2 DTTI0X_2 SCS11_2	I*	I
48	44	31	P60 SIN3_0 TIOA2_2 INT15_1 IC00_0 IGTRG0_0 SCS10_2	I*	J
49	45	-	P80 SCK1_2 FRCK0_1	K	I
50	46	-	P81 SOT1_2	K	I
51	47	-	P82 SIN1_2	K	I
52	48	32	VSS	-	
5,21,36,40	-	-	NC	-	

*:5V tolerant I/O

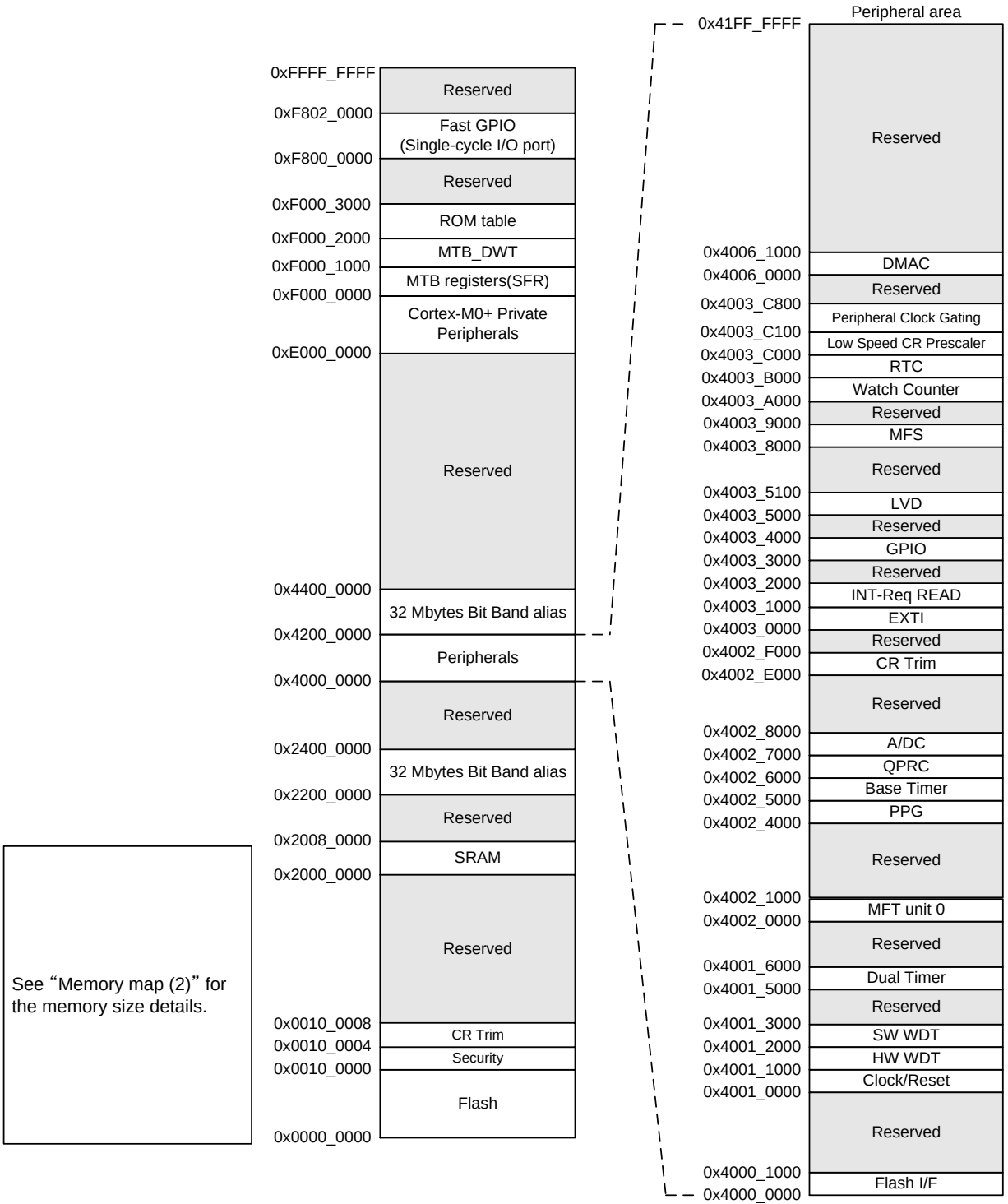
Type	Circuit	Remarks
C		• Open drain output • CMOS level hysteresis input
D		It is possible to select the sub oscillation / GPIO function When the sub oscillation is selected. • Oscillation feedback resistor : Approximately 5MΩ • With standby mode control When the GPIO is selected. • CMOS level output. • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50kΩ • I_{OH}= -4mA, I_{OL}= 4mA

9. Memory Size

See Memory size in 1. Product Lineup to confirm the memory size.

10. Memory Map

Memory Map (1)



Peripheral Address Map

Start address	End address	Bus	Peripheral
0x4000_0000	0x4000_0FFF	AHB	Flash memory I/F register
0x4000_1000	0x4000_FFFF		Reserved
0x4001_0000	0x4001_0FFF	APB0	Clock/Reset Control
0x4001_1000	0x4001_1FFF		Hardware Watchdog Timer
0x4001_2000	0x4001_2FFF		Software Watchdog Timer
0x4001_3000	0x4001_4FFF		Reserved
0x4001_5000	0x4001_5FFF		Dual-Timer
0x4001_6000	0x4001_FFFF		Reserved
0x4002_0000	0x4002_0FFF	APB1	Multi-function Timer unit0
0x4002_1000	0x4002_3FFF		Reserved
0x4002_4000	0x4002_4FFF		PPG
0x4002_5000	0x4002_5FFF		Base Timer
0x4002_6000	0x4002_6FFF		Quadrature Position/Revolution Counter
0x4002_7000	0x4002_7FFF		A/D Converter
0x4002_8000	0x4002_DFFF		Reserved
0x4002_E000	0x4002_EFFF		Built-in CR trimming
0x4002_F000	0x4002_FFFF		Reserved
0x4003_0000	0x4003_0FFF		External Interrupt Controller
0x4003_1000	0x4003_1FFF		Interrupt Request Batch-Read Function
0x4003_2000	0x4003_2FFF		Reserved
0x4003_3000	0x4003_3FFF		GPIO
0x4003_4000	0x4003_4FFF		Reserved
0x4003_5000	0x4003_57FF		Low-Voltage Detection
0x4003_5800	0x4003_7FFF		Reserved
0x4003_8000	0x4003_8FFF		Multi-function Serial Interface
0x4003_9000	0x4003_9FFF		Reserved
0x4003_A000	0x4003_AFFF		Watch Counter
0x4003_B000	0x4003_BFFF		Real-time clock
0x4003_C000	0x4003_C0FF		Low-speed CR Prescaler
0x4003_C100	0x4003_C7FF		Peripheral Clock Gating
0x4003_C800	0x4003_FFFF		Reserved
0x4004_0000	0x4005_FFFF	AHB	Reserved
0x4006_0000	0x4006_0FFF		DMAC register
0x4006_1000	0x41FF_FFFF		Reserved

12.4 AC Characteristics

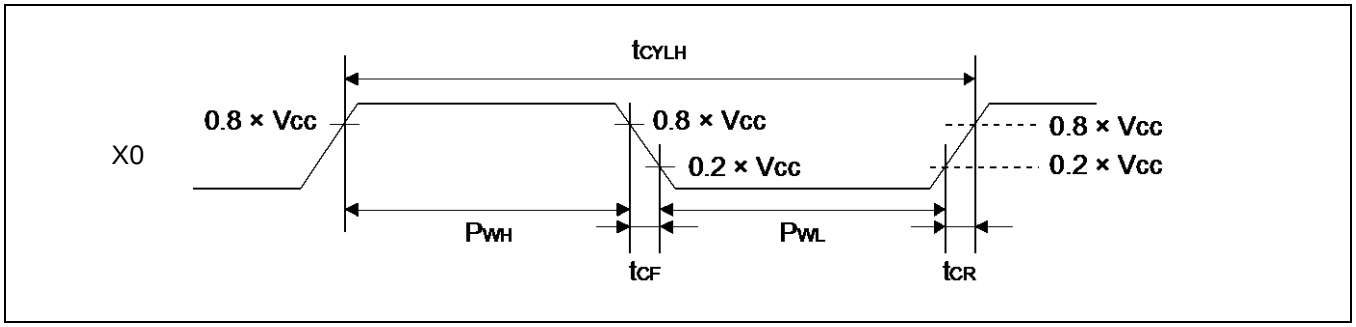
12.4.1 Main Clock Input Characteristics

(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	F_{CH}	X0, X1	V_{CC} ≥ 4.5V	4	40	MHz	When the crystal oscillator is connected
			V_{CC} < 4.5V	4	20		
			-	4	40	MHz	When the external clock is used
Input clock cycle	t_{CYLH}		-	25	250	ns	When the external clock is used
Input clock pulse width	-		P_{WH}/t_{CYLH}, P_{WL}/t_{CYLH}	45	55	%	When the external clock is used
Input clock rising time and falling time	t_{CF}, t_{CR}		-	-	5	ns	When the external clock is used
Internal operating clock*1 frequency	F_{CM}	-	-	-	41.2	MHz	Master clock
	F_{CC}	-	-	-	41.2	MHz	Base clock (HCLK/FCLK)
	F_{CP0}	-	-	-	41.2	MHz	APB0 bus clock*2
	F_{CP1}	-	-	-	41.2	MHz	APB1 bus clock*2
Internal operating clock*1 cycle time	t_{CYCC}	-	-	24.27	-	ns	Base clock (HCLK/FCLK)
	t_{CYCP0}	-	-	24.27	-	ns	APB0 bus clock*2
	t_{CYCP1}	-	-	24.27	-	ns	APB1 bus clock*2

*1: For details of each internal operating clock, refer to "CHAPTER: Clock" in "FM0+ Family PERIPHERAL MANUAL".

*2: For details of the APB bus to which a peripheral is connected, see "8. Block Diagram".



12.4.4 Operating Conditions of Main PLL (In the case of using the main clock as the input clock of the PLL)

(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	F_{PLLI}	4	-	16	MHz	
PLL multiple rate	-	5	-	37	multiple	
PLL macro oscillation clock frequency	F_{PLLO}	75	-	150	MHz	
Main PLL clock frequency*2	F_{CLKPLL}	-	-	40	MHz	

*1: The wait time is the time it takes for PLL oscillation to stabilize.

*2: For details of the main PLL clock (CLKPLL), refer to "CHAPTER: Clock" in "FM0+ Family PERIPHERAL MANUAL".

12.4.5 Operating Conditions of Main PLL (In the case of using the built-in high-speed CR clock as the input clock of the main PLL)

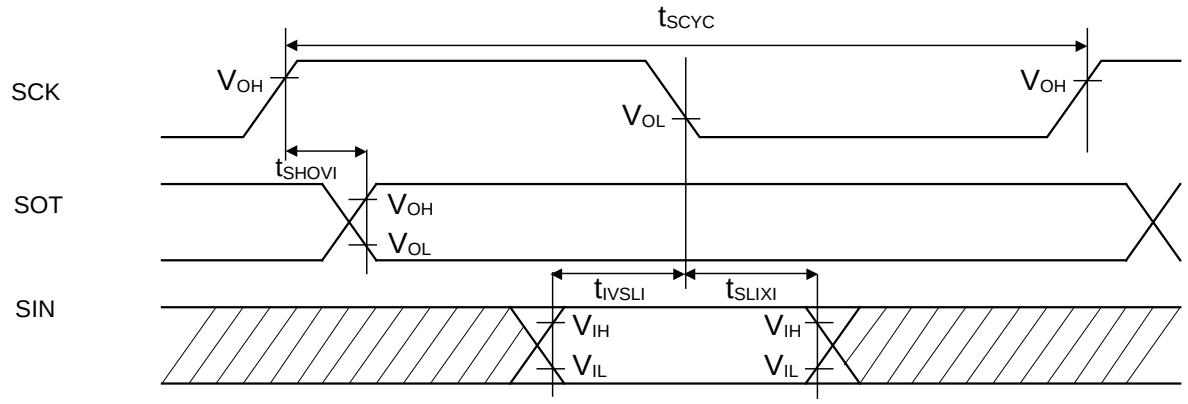
(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	F_{PLLI}	3.88	4	4.12	MHz	
PLL multiple rate	-	19	-	35	multiple	
PLL macro oscillation clock frequency	F_{PLLO}	72	-	150	MHz	
Main PLL clock frequency*2	F_{CLKPLL}	-	-	41.2	MHz	

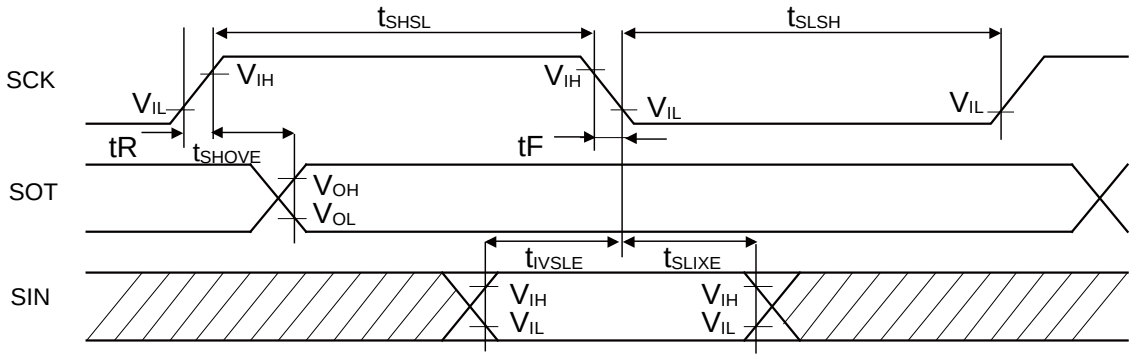
*1: The wait time is the time it takes for PLL oscillation to stabilize.

*2: For details of the main PLL clock (CLKPLL), refer to "CHAPTER: Clock" in "FM0+ Family PERIPHERAL MANUAL".

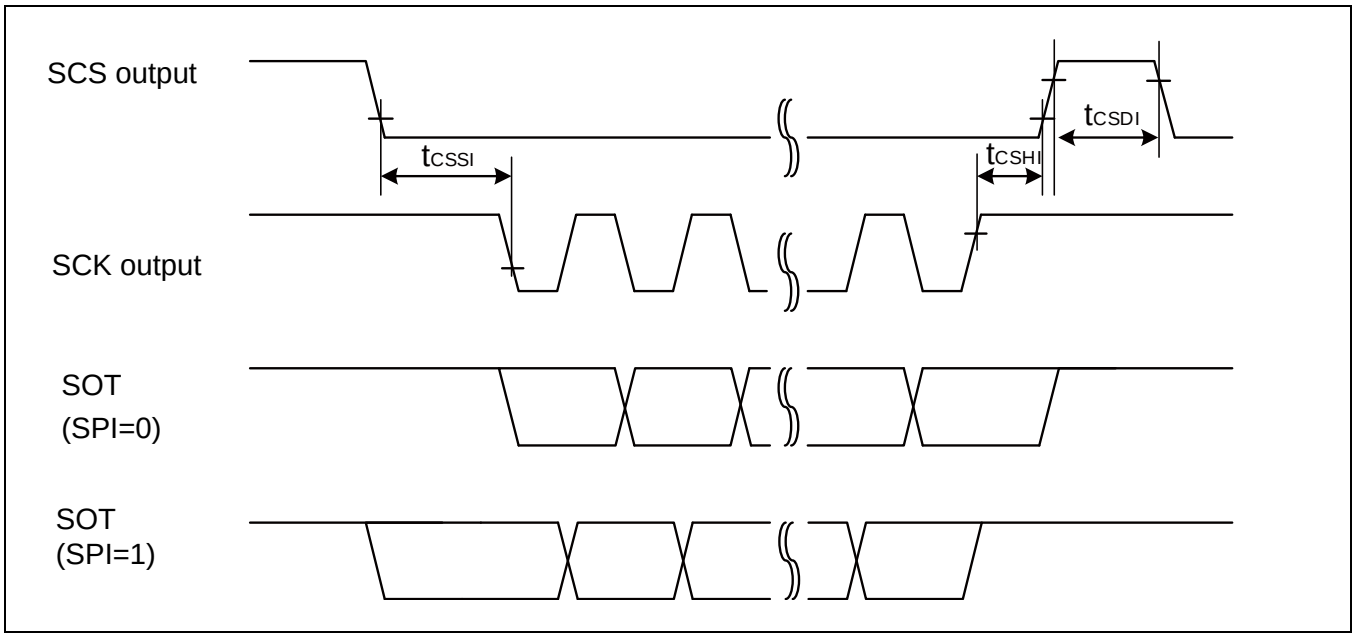
Note:
For the main PLL source clock, input the high-speed CR clock (CLKHC) whose frequency has been trimmed.

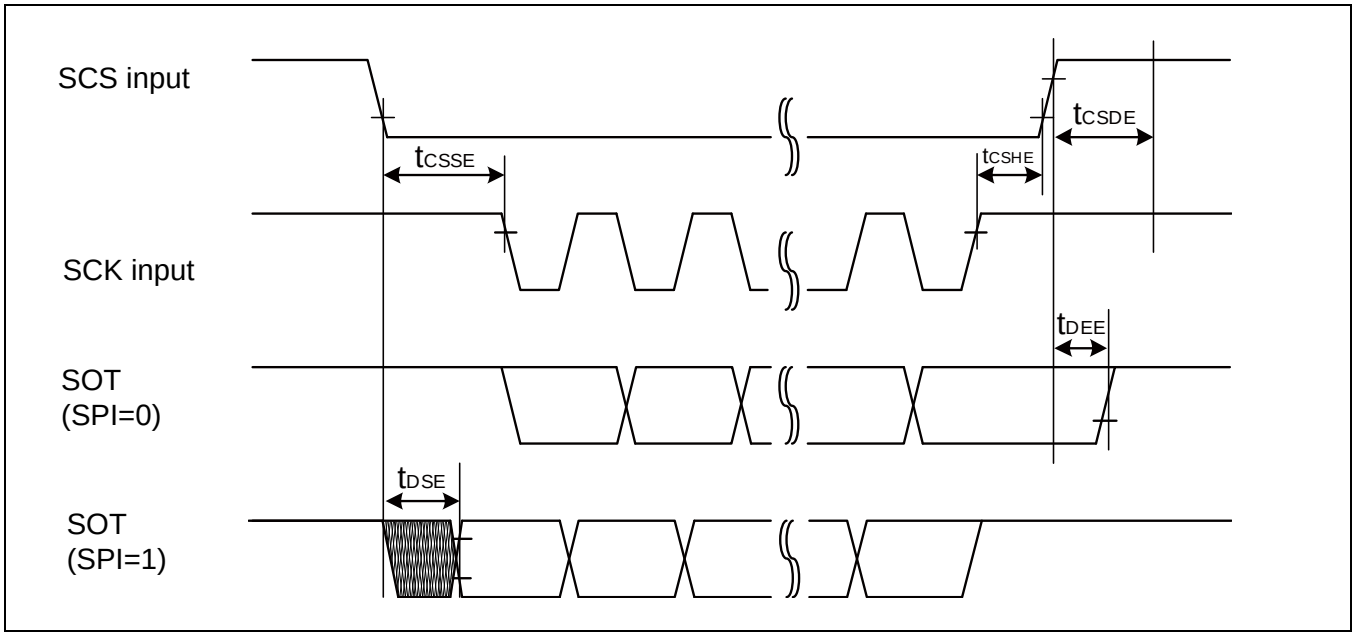


MS bit = 0



MS bit = 1


SCS output
tCSSI
tCSHI
tCSDI
SCK output
SOT
(SPI=0)
SOT
(SPI=1)


SCS input
tCSSE
tCSHE
tCSDE
SCK input
tDEE
SOT
(SPI=0)
tDSE
SOT
(SPI=1)

When using synchronous serial chip select (SPI = 1, SCINV = 0, MS=0, CSLVL=0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5V		V_{CC} ≥ 4.5V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↓ setup time	t_{CSSI}	Internal shift clock operation	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↑→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	ns
SCS↑→SCK↓ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCK↑→SCS↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCS↑→SOT delay time	t_{DSE}		-	40	-	40	ns
SCS↓→SOT delay time	t_{DEE}		0	-	0	-	ns

(*1): CSSU bit value × serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value × serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value × serial chip select timing operating clock cycle [ns]

Notes:

- t_{CYCP} indicates the APB bus clock cycle time.
  About the APB bus number which Multi-function Serial is connected to, see "8. Block Diagram ".
- About CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM0+ Family PERIPHERAL MANUAL".
- When the external load capacitance C_L = 30pF.

When using synchronous serial chip select (SPI = 1, SCINV = 1, MS=0, CSLVL=0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5V		V_{CC} ≥ 4.5V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↑ setup time	t_{CSSI}	Internal shift clock operation	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↓→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	ns
SCS↑→SCK↑ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCK↓→SCS↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCS↑→SOT delay time	t_{DSE}		-	40	-	40	ns
SCS↓→SOT delay time	t_{DEE}		0	-	0	-	ns

(*1): CSSU bit value × serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value × serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value × serial chip select timing operating clock cycle [ns]

Notes:

- t_{CYCP} indicates the APB bus clock cycle time.
  About the APB bus number which Multi-function Serial is connected to, see "8. Block Diagram ".
- About CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM0+ Family PERIPHERAL MANUAL".
- When the external load capacitance C_L = 30pF.

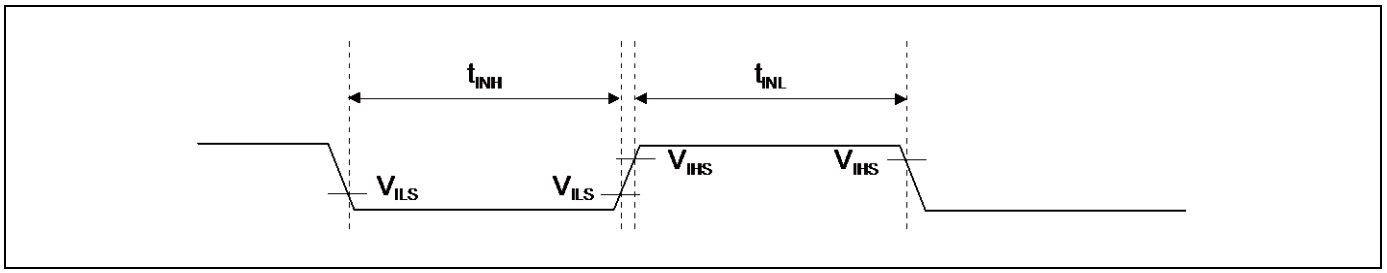
12.4.10 External Input Timing

(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{INH}, t_{INL}	ADTGx	-	2 t_{CYCP}*1	-	ns	A/D converter trigger input
		FRCKx					Free-run timer input clock
		ICxx					Input capture
		DTTIxX	-	2 t_{CYCP}*1	-	ns	Wave form generator
		INTxx, NMIX	-	2 t_{CYCP} + 100*1	-	ns	External interrupt, NMI
				500*2	-	ns	

*1: t_{CYCP} represents the APB bus clock cycle time except when the APB bus clock stops in STOP mode or in TIMER mode. For the number of the APB bus to which the Multi-function Timer is connected and that of the APB bus to which the External Interrupt Controller is connected, see "8. Block Diagram".

*2: In STOP mode and TIMER mode



12.6 Low-voltage Detection Characteristics

12.6.1 Low-voltage Detection Reset

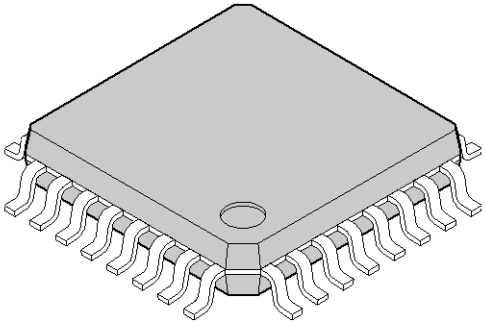
(Ta = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHR[*1] = 00000	2.25	2.45	2.65	V	When voltage drops
Released voltage	VDH		2.30	2.50	2.70	V	When voltage rises
Detected voltage	VDL	SVHR[*1] = 00001	2.39	2.60	2.81	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR[*1] = 00010	2.48	2.70	2.92	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR[*1] = 00011	2.58	2.80	3.02	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR[*1] = 00100	2.76	3.00	3.24	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR[*1] = 00101	2.94	3.20	3.46	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR[*1] = 00110	3.31	3.60	3.89	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR[*1] = 00111	3.40	3.70	4.00	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR[*1] = 01000	3.68	4.00	4.32	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR[*1] = 01001	3.77	4.10	4.43	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR[*1] = 01010	3.86	4.20	4.54	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
LVD stabilization wait time	T_{LVDW}	-	-	-	8160× t_{CYCP}[*2]	µs	
LVD detection delay time	T_{LVDDL}	-	-	-	200	µs	

*1: SVHR bit of Low-Voltage Detection Voltage Control Register (LVD_CTL) is reset to SVHR = 00000 by low voltage detection reset.

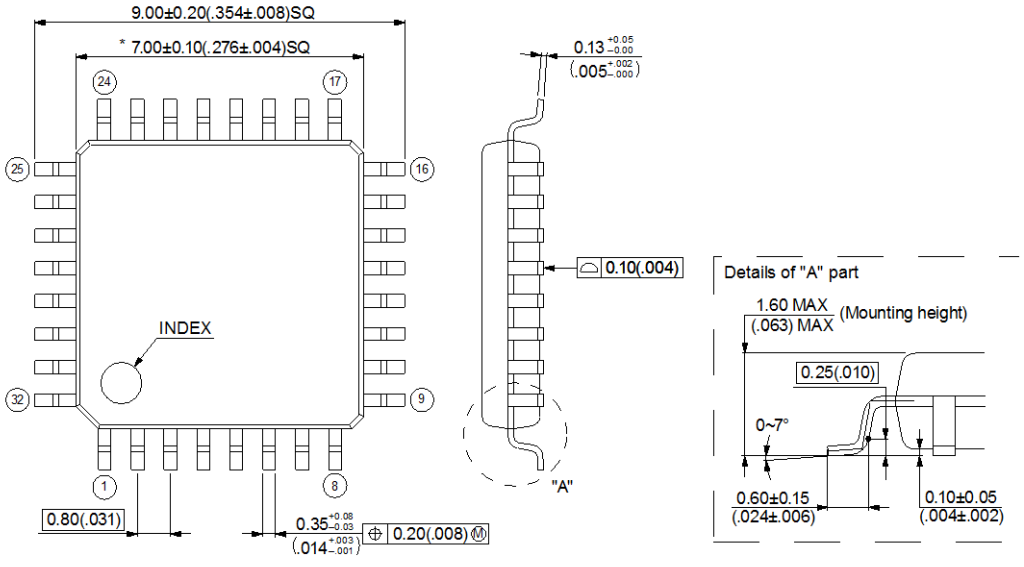
*2: t_{CYCP} indicates the APB1 bus clock cycle time.

14. Package Dimensions

32-pin plastic LQFP		
 (FPT-32P-M30)	Lead pitch	0.80 mm
	Package width × package length	7.00 mm × 7.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.60 mm MAX

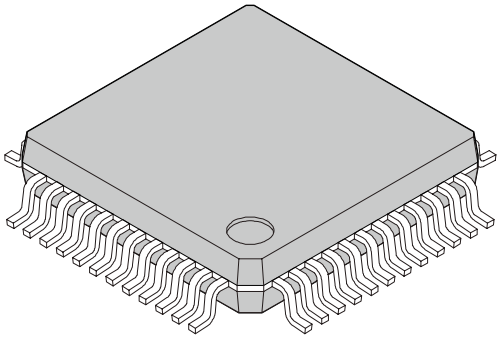
32-pin plastic LQFP
(FPT-32P-M30)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference **values.**

48-pin plastic LQFP

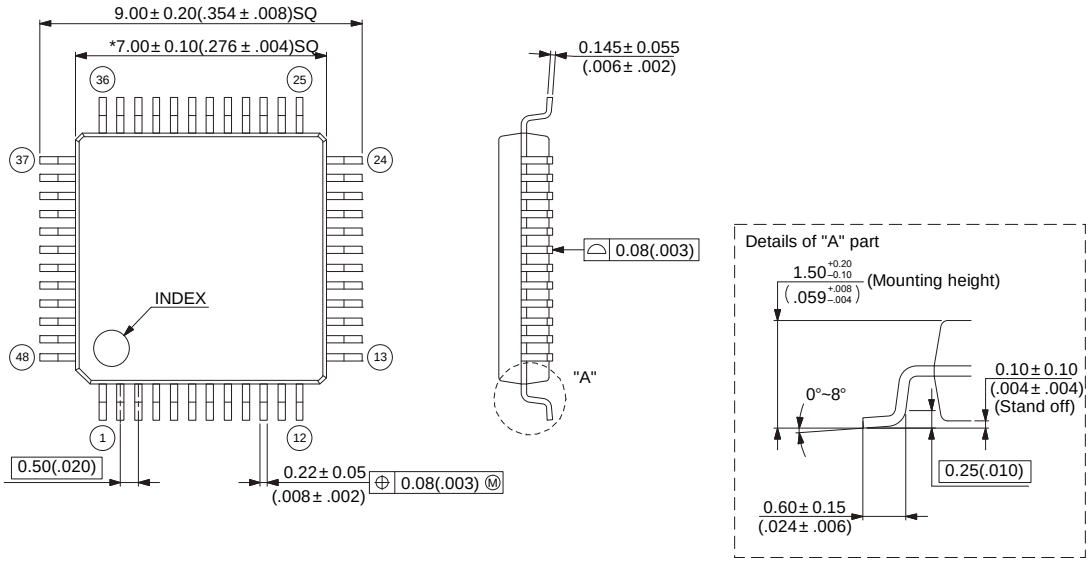


(FPT-48P-M49)

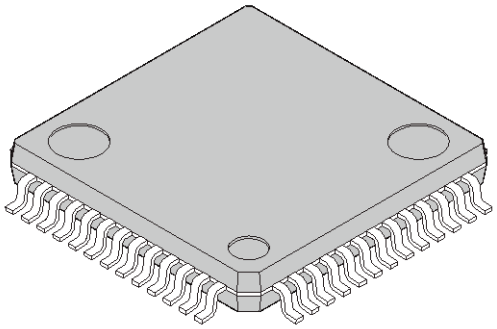
Lead pitch	0.50 mm
Package width × package length	7.00 mm × 7.00 mm
Lead shape	Gullwing
Lead bend direction	Normal bend
Sealing method	Plastic mold
Mounting height	1.70 mm MAX
Weight	0.17 g

48-pin plastic LQFP
(FPT-48P-M49)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.

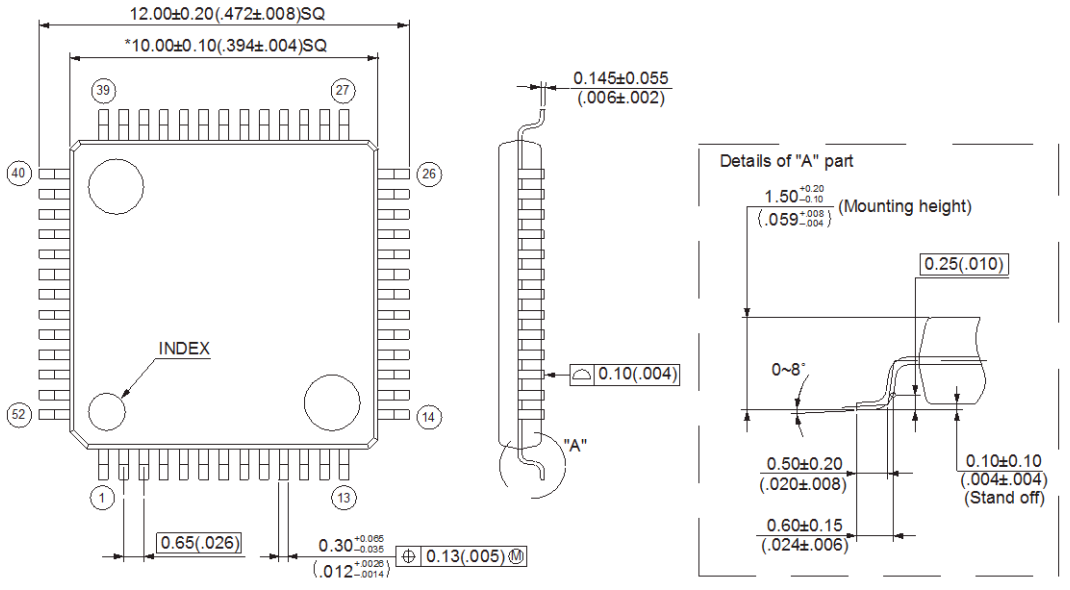


Dimensions in mm (inches).
Note: The values in parentheses are reference values.

52-pin plastic LQFP		
	Lead pitch	0.65 mm
	Package width × package length	10.00 × 10.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.32 g
(FPT-52P-M02)	Code (Reference)	P-LFQFP52-10 × 10-0.65

52-pin plastic LQFP
(FPT-52P-M02)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values

15. Major Changes

Spansion Publication Number: S6E1A1_DS710-00001

Page	Section	Change Results
Revision 0.1		
-	-	Initial release
Revision 1.0 [July 16,2014]		
-	-	Revised from "Preliminary" to "Full Production"
3	1. Description	Revised from "TYPE1" product to "TYPE1-M0+" product
5	2. Features	Revised "Processor version"
6	2. Features	Revised "Conversion time" of 12-bit A/D converter
9	3. Product Lineup	Added "Note" for accuracy of built-in CR
21,22,23, 24,25	6. List of Pin Functions List of pin functions	Revised Pin number 30 and 31 of LQFP-32 and QFN-32
23	6. List of Pin Functions List of pin functions	Revised Function description of SOT1_x(SDA1_x)
40	12. Memory Map Memory map (1)	Revised from "MTB resister" to "MTB resister(SFR)"
41	12. Memory Map Memory map (2)	Revised product name and RAM address
46	14. Electrical Characteristics 14.1 Absolute Maximum Ratings	Revised Analog pin input voltage
47	14. Electrical Characteristics 14.2 Recommended Operating Conditions	Added note "*2"
48,49,50	14. Electrical Characteristics 14.3 DC Characteristics 14.3.1 Current Rating	• Revised and added "Conditions" • Revised the value of "TBD"
52	14. Electrical Characteristics 14.4 AC Characteristics 14.4.1 Main Clock Input Characteristics	Revised the value of "Internal operating clock frequency" and "Internal operating clock cycle time"
54	14. Electrical Characteristics 14.4 AC Characteristics 14.4.3 Built-in CR Oscillation Characteristics	Revised the value of "TBD"
55	14. Electrical Characteristics 14.4 AC Characteristics 14.4.5 Operating Conditions of Main PLL(In the case of using the built-in high-speed CR clock as the input clock of the main PLL)	• Revised the value of "TBD" • Revised the maximum value of "Main PLL clock frequency"
56	14. Electrical Characteristics 14.4 AC Characteristics 14.4.7 Power-on Reset Timing	• Revised the value of "TBD" • Revised from "LVDL_minimum" to "VDH_minimum"
78	14. Electrical Characteristics 14.4 AC Characteristics 14.4.12 I2C Timing	• Revised the condition of "Noise filter" • Revised the note for noise filter
80	14. Electrical Characteristics 14.5 12-bit A/D Converter	• Revised the value of "Conversion time", "Sampling time" and "Compare clock cycle" • Revised the value of "State transition time to operation permission" • Revised the note
83,84	14. Electrical Characteristics 14.6 Low-voltage Detection Characteristics	Revised the value of SVHR and SVHI
85	14. Electrical Characteristics 14.7 Flash Memory Write/Erase Characteristics	• Revised the value of "TBD" • Revised the value of typical

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