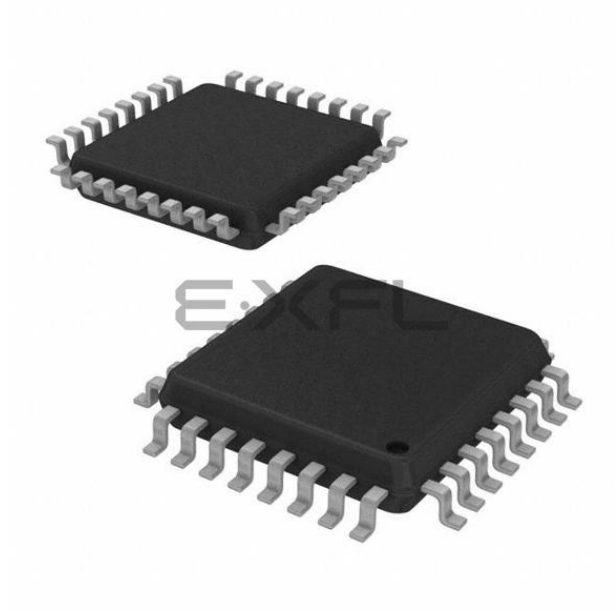


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CSIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	23
Program Memory Size	88KB (88K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 5x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e1a12b0agp20000

Watch Counter
The Watch Counter wakes up the microcontroller from the low power consumption mode. The clock source can be selected from the main clock, the sub clock, the built-in high-speed CR clock or the built-in low-speed CR clock.

Interval timer: up to 64 s (sub clock: 32.768 kHz)

External Interrupt Controller Unit

- Up to 8 external interrupt input pins
- Non-maskable interrupt (NMI) input pin: 1

Watchdog Timer (2 channels)
The watchdog timer generates an interrupt or a reset when the counter reaches a time-out value.

This series consists of two different watchdogs, "hardware" watchdog and "software" watchdog.

The "hardware" watchdog timer is clocked by the built-in low-speed CR oscillator. Therefore, the "hardware" watchdog is active in any low-power consumption modes except RTC mode and STOP mode.

Clock and Reset

- Clocks

A clock can be selected from five clock sources (two external oscillators, two built-in CR oscillator, and main PLL).

  - Main clock : 4 MHz to 40MHz
  - Sub clock : 32.768 kHz
  - Built-in high-speed CR clock : 4 MHz
  - Built-in low-speed CR clock : 100 kHz
  - Main PLL clock

- Resets
  - Reset request from the INITX pin
  - Power on reset
  - Software reset
  - Watchdog timer reset
  - Low-voltage detection reset
  - Clock supervisor reset

Clock Supervisor (CSV)
The Clock Supervisor monitors the failure of external clocks with a clock generated by a built-in CR oscillator.

- If an external clock failure (clock stop) is detected, a reset is asserted.
- If an external frequency anomaly is detected, an interrupt or a reset is asserted.

Low-voltage Detector (LVD)
This series monitors the voltage on the VCC pin with a 2-stage mechanism. When the voltage falls below a designated voltage, the Low-voltage Detector generates an interrupt or a reset.

- LVD1: error reporting via an interrupt
- LVD2: auto-reset operation

Low Power Consumption Mode
This series has four low power consumption modes.

- SLEEP
- TIMER
- RTC
- STOP

Peripheral Clock Gating
The system can reduce the current consumption of the total system with gating the operation clocks of peripheral functions not used.

Debug

- Serial Wire Debug Port (SW-DP)
- Micro Trace Buffer (MTB)

Unique ID
A 41-bit unique value of the device has been set.

Power Supply
Wide voltage range: VCC = 2.7 V to 5.5 V

2. Packages

Product name / Package	S6E1A11B0A S6E1A12B0A	S6E1A11C0A S6E1A12C0A
LQFP: FPT-32P-M30 (0.80 mm pitch)	❍	-
QFN: LCC-32P-M73 (0.50 mm pitch)	❍	-
LQFP: FPT-48P-M49 (0.50 mm pitch)	-	❍
QFN: LCC-48P-M74 (0.50 mm pitch)	-	❍
LQFP: FPT-52P-M02 (0.65 mm pitch)	-	❍

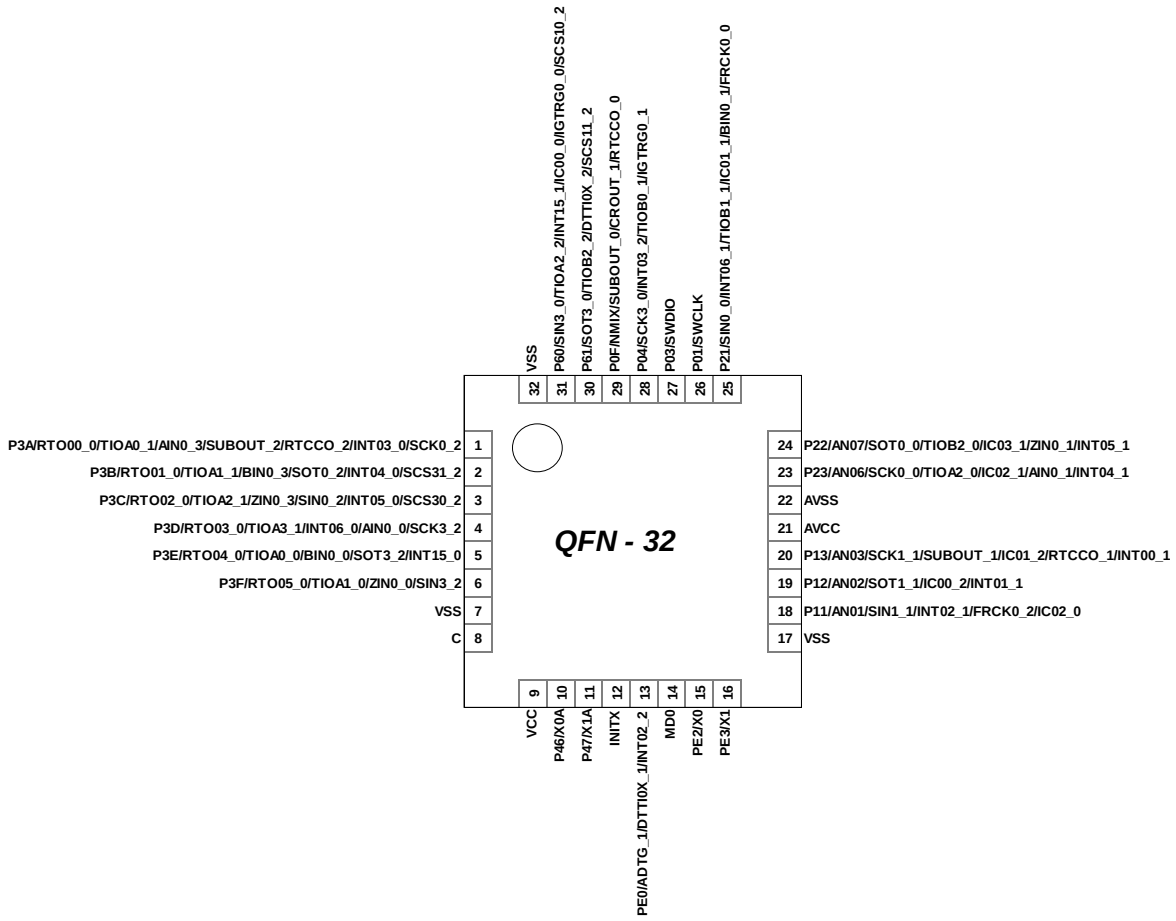
❍: Supported

Note:

- See "14. Package Dimensions" for detailed information on each package.

LCC-32P-M73

(TOP VIEW)



Note:

- The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.
  Use the extended port function register (EPFR) to select the pin.

4. Pin Descriptions

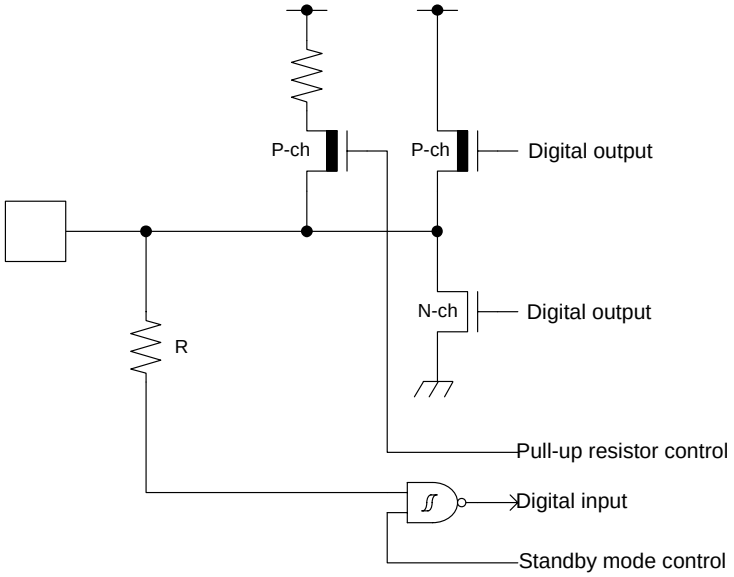
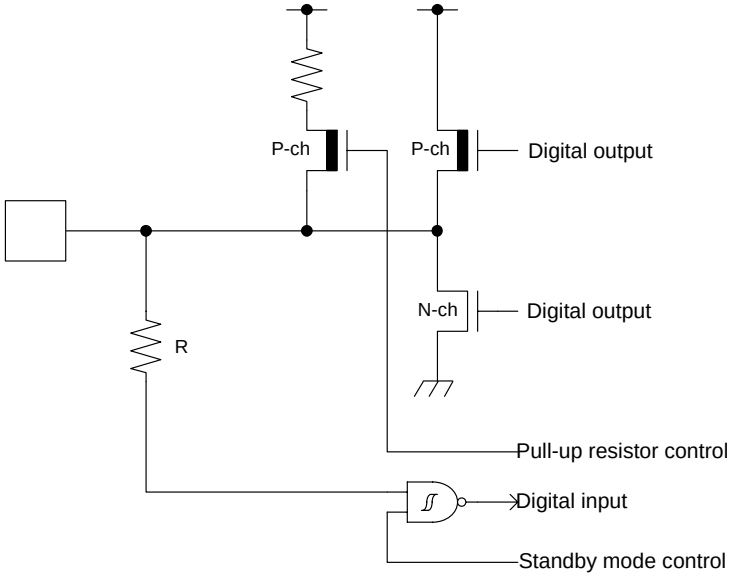
List of Pin Functions

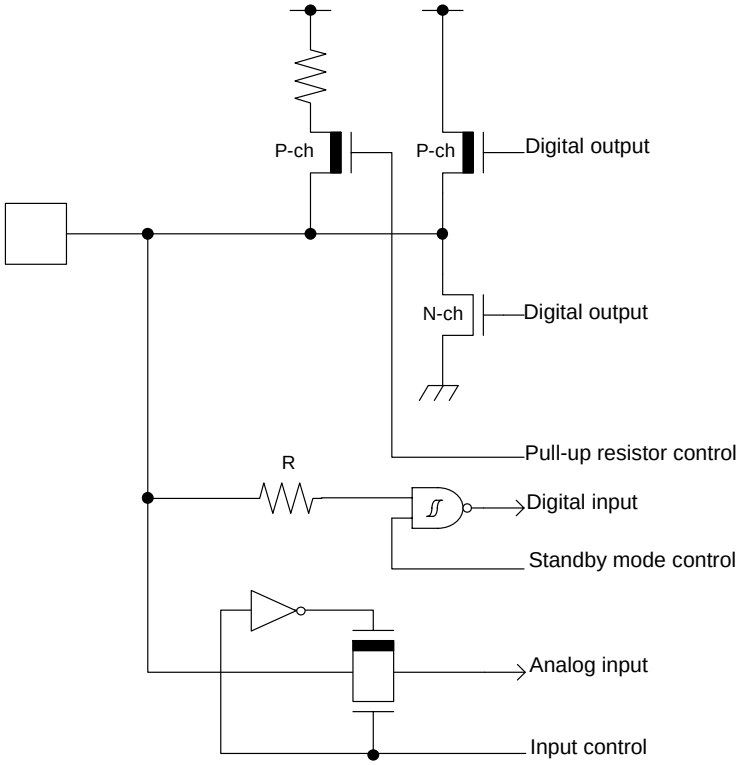
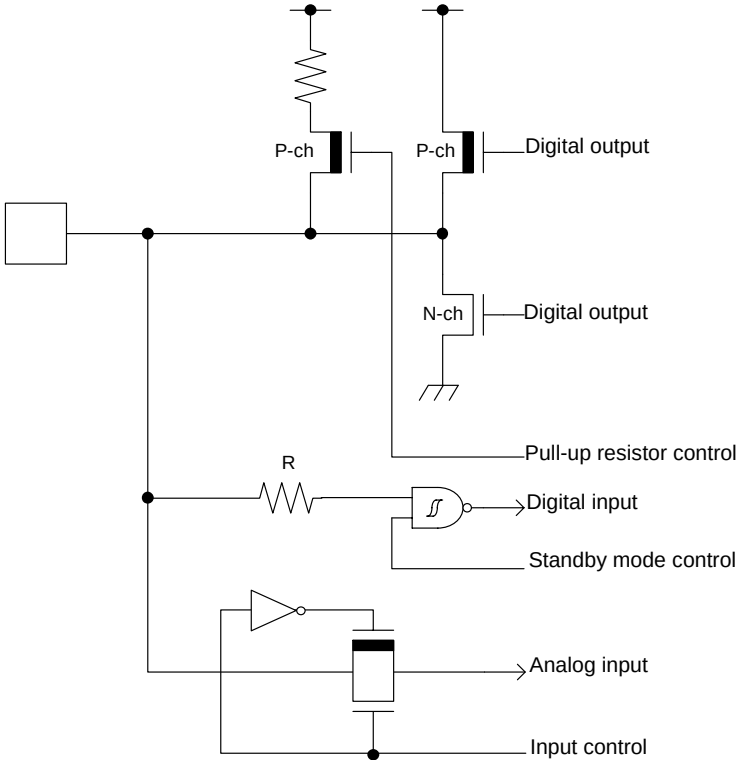
The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.

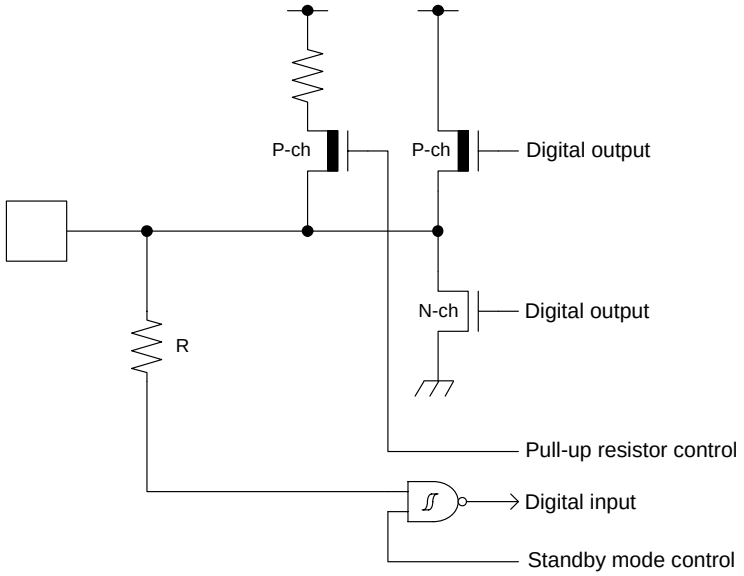
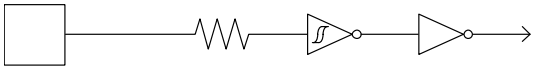
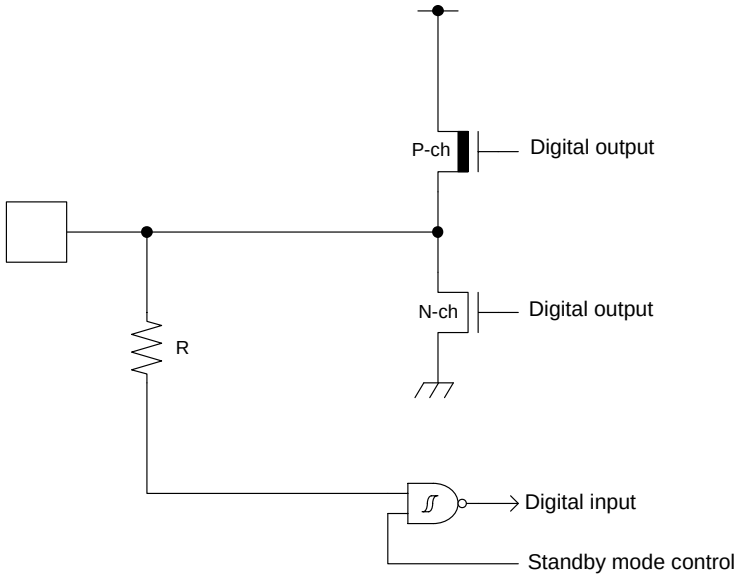
Use the extended port function register (EPFR) to select the pin.

Pin no.			Pin name	I/O circuit type	Pin state type
LQFP-52	LQFP-48 QFN-48	LQFP-32 QFN-32			
1	1	-	VCC	-	
2	2	-	P50 INT00_0 AIN0_2 SIN3_1 IC01_0	I*	J
3	3	-	P51 INT01_0 BIN0_2 SOT3_1	I*	J
4	4	-	P52 INT02_0 ZIN0_2 SCK3_1	I*	J
6	5	-	P39 DTTI0X_0 ADTG_2	E	I
7	6	1	P3A RTO00_0 TIOA0_1 AIN0_3 SUBOUT_2 RTCCO_2 INT03_0 SCK0_2	F	J
8	7	2	P3B RTO01_0 TIOA1_1 BIN0_3 SOT0_2 INT04_0 SCS31_2	F	J

Pin no.			Pin name	I/O circuit type	Pin state type
LQFP-52	LQFP-48 QFN-48	LQFP-32 QFN-32			
32	30	-	P15 AN05 SOT0_1 SCS11_1 IC03_2 INT15_2	H*	L
33	31	21	AVCC	-	
34	32	-	AVRH	-	
35	33	22	AVSS	-	
37	34	23	P23 AN06 SCK0_0 TIOA2_0 IC02_1 AIN0_1 INT04_1	G	L
38	35	24	P22 AN07 SOT0_0 TIOB2_0 IC03_1 ZIN0_1 INT05_1	G	L
39	36	25	P21 SIN0_0 INT06_1 TIOB1_1 IC01_1 BIN0_1 FRCK0_0	E	J
41	37	-	P00	E	I
42	38	26	P01 SWCLK	E	H
43	39	-	P02	E	I
44	40	27	P03 SWDIO	E	H

Type	Circuit	Remarks
E		• CMOS level output • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50kΩ • I_{OH}= -4mA, I_{OL}= 4mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off
F		• CMOS level output • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50kΩ • I_{OH}= -12mA, I_{OL}= 12mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off

Type	Circuit	Remarks
G		• CMOS level output • CMOS level hysteresis input • With input control • Analog input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50kΩ • I_{OH}= -4mA, I_{OL}= 4mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off
H		• CMOS level output • CMOS level hysteresis input • With input control • Analog input • 5V tolerant • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50kΩ • I_{OH}= -4mA, I_{OL}= 4mA • Available to control of PZR registers. • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off

Type	Circuit	Remarks
I		• CMOS level output • CMOS level hysteresis input • 5V tolerant • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50kΩ • I_{OH}= -4mA, I_{OL}= 4mA • Available to control PZR registers • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off
J		CMOS level hysteresis input
K		• CMOS level output • CMOS level hysteresis input • With standby mode control • I_{OH}= -4mA, I_{OL}= 4mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off

Notes on Power-on

Turn power on/off in the following order or at the same time.

Turning on : VBAT → VCC
VCC → AVCC → AVRH
Turning off : VCC → VBAT
AVRH → AVCC → VCC

Serial Communication

There is a possibility to receive wrong data due to the noise or other causes on the serial communication.
Therefore, design a printed circuit board so as to avoid noise.

Consider the case of receiving wrong data due to noise, perform error detection such as by applying a checksum of data at the end.
If an error is detected, retransmit the data.

Differences in Features among the Products with Different Memory Sizes and between Flash Products and MASK Products

The electric characteristics including power consumption, ESD, latch-up, noise characteristics, and oscillation characteristics among the products with different memory sizes and between Flash products and MASK products are different because chip layout and memory structures are different.

If you are switching to use a different product of the same series, please make sure to evaluate the electric characteristics.

Pull-Up Function of 5V Tolerant I/O

Please do not input the signal more than VCC voltage at the time of Pull-Up function use of 5V tolerant I/O.

List of Pin Status

Pin status type	Function group	State upon power-on reset or low-voltage detection	State at INITX input	State upon device internal reset	State in Run mode or SLEEP mode	State in TIMER mode, RTC mode, or STOP mode	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable	
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1	
		-	-	-	-	SPL = 0	SPL = 1
A	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"
	Main crystal oscillator input pin/ External main clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
B	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"
	External main clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"
	Main crystal oscillator output pin	Hi-Z / Internal input fixed at "0"/ Input enabled	Hi-Z / Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	Maintain previous state/When oscillation stops*[1], Hi-Z / Internal input fixed at "0"	Maintain previous state/When oscillation stops*[1], Hi-Z / Internal input fixed at "0"	Maintain previous state/When oscillation stops*[1], Hi-Z / Internal input fixed at "0"
C	INITX input pin	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled
D	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
E	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"
	Sub crystal oscillator input pin / External sub clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
F	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"
	External sub clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"

LVD current

(V_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Low-Voltage detection circuit (LVD) power supply current	I_{CCLVD}	VCC	At operation	0.13	0.3	µA	For occurrence of reset
				0.13	0.3	µA	For occurrence of interrupt

Flash memory current

(V_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Flash memory write/erase current	$I_{CCFLASH}$	VCC	At Write/Erase	9.5	11.2	mA	

A/D convertor current (S6E1A1xC0A)

(V_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Power supply current	I_{CCAD}	AVCC	At operation	0.7	0.9	mA	
			At stop	0.13	13	µA	
Reference power supply current (AVRH)	I_{CCAVRH}	AVRH	At operation	1.1	1.97	mA	AVRH=5.5V
			At stop	0.1	1.7	µA	

A/D convertor current (S6E1A1xB0A)

(V_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Power supply current	I_{CCAD}	AVCC	At operation	1.8	2.87	mA	
			At stop	0.23	14.7	µA	

Peripheral current dissipation

Clock system	Peripheral	Conditions	Frequency (MHz)				Unit	Remarks
			4	8	20	40		
HCLK	GPIO	At all ports operation	0.11	0.22	0.55	1.10	mA	
	DMAC	At 2ch operation	0.05	0.11	0.25	0.51		
PCLK1	Base timer	At 4ch operation	0.03	0.05	0.15	0.30	mA	
	Multi-functional timer/PPG	At 1unit/4ch operation	0.14	0.28	0.68	1.38		
	Quadrature position/Revolution counter	At 1unit operation	0.02	0.04	0.11	0.22		
	ADC	At 1unit operation	0.07	0.14	0.37	0.73		
	Multi-function serial	At 1ch operation	0.15	0.31	0.77	1.54		

12.4 AC Characteristics

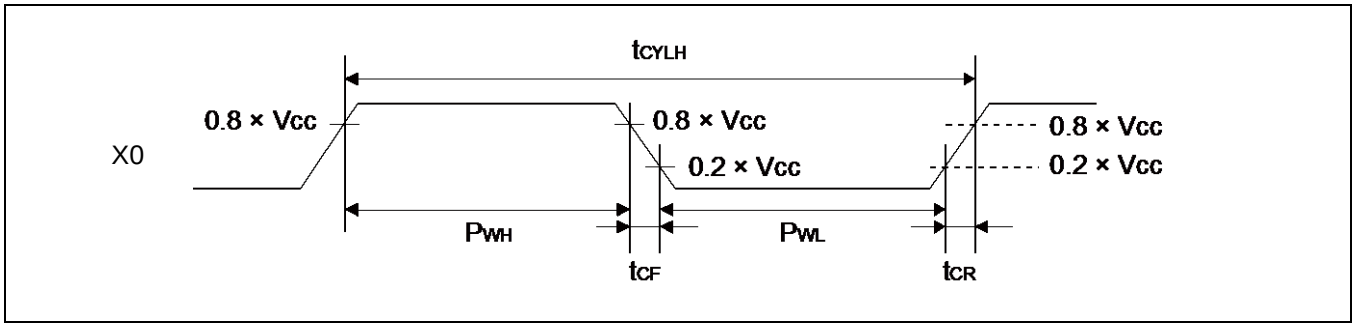
12.4.1 Main Clock Input Characteristics

(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	F_{CH}	X0, X1	V_{CC} ≥ 4.5V	4	40	MHz	When the crystal oscillator is connected
			V_{CC} < 4.5V	4	20		
			-	4	40	MHz	When the external clock is used
Input clock cycle	t_{CYLH}		-	25	250	ns	When the external clock is used
Input clock pulse width	-		P_{WH}/t_{CYLH}, P_{WL}/t_{CYLH}	45	55	%	When the external clock is used
Input clock rising time and falling time	t_{CF}, t_{CR}		-	-	5	ns	When the external clock is used
Internal operating clock*1 frequency	F_{CM}	-	-	-	41.2	MHz	Master clock
	F_{CC}	-	-	-	41.2	MHz	Base clock (HCLK/FCLK)
	F_{CP0}	-	-	-	41.2	MHz	APB0 bus clock*2
	F_{CP1}	-	-	-	41.2	MHz	APB1 bus clock*2
Internal operating clock*1 cycle time	t_{CYCC}	-	-	24.27	-	ns	Base clock (HCLK/FCLK)
	t_{CYCP0}	-	-	24.27	-	ns	APB0 bus clock*2
	t_{CYCP1}	-	-	24.27	-	ns	APB1 bus clock*2

*1: For details of each internal operating clock, refer to "CHAPTER: Clock" in "FM0+ Family PERIPHERAL MANUAL".

*2: For details of the APB bus to which a peripheral is connected, see "8. Block Diagram".

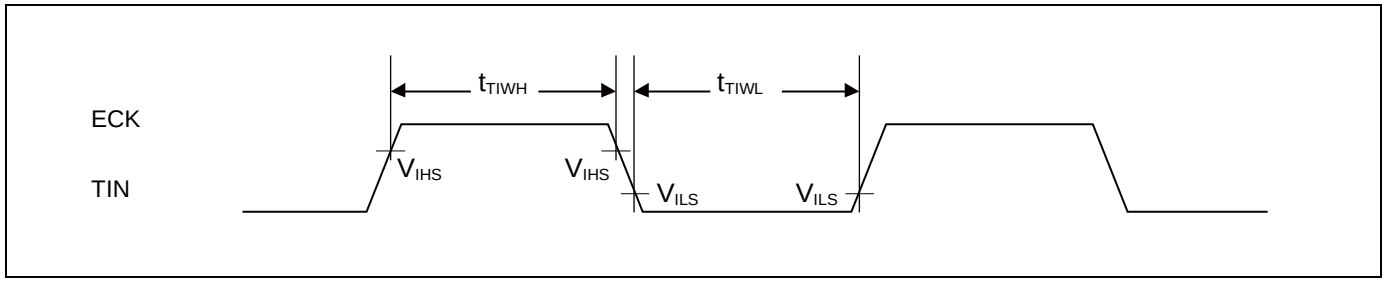


12.4.8 Base Timer Input Timing

Timer input timing

(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

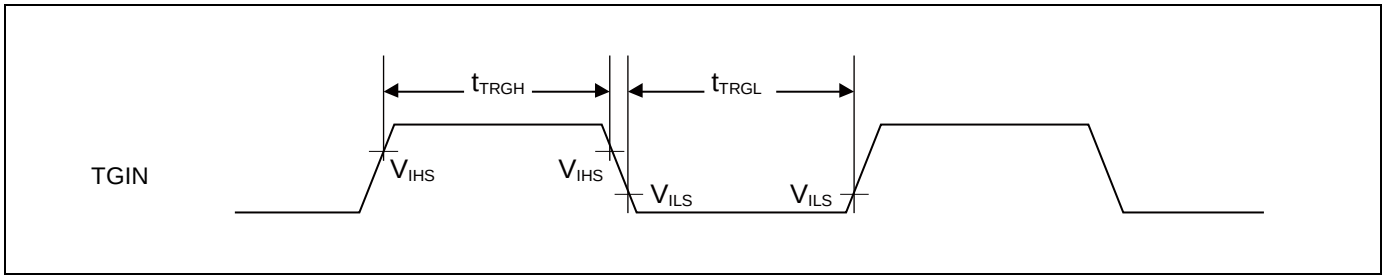
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}, t_{TIWL}	TIOAn/TIOBn (when using as ECK, TIN)	-	2 t_{CYCP}	-	ns	



Trigger input timing

(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	TIOAn/TIOBn (when using as TGIN)	-	2 t_{CYCP}	-	ns	



Note:

- t_{CYCP} indicates the APB bus clock cycle time.
  For the number of the APB bus to which the Base Timer has been connected, see "8. Block Diagram".

Synchronous serial (SPI = 1, SCINV = 1)

(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	4 t_{CYCP}	-	4 t_{CYCP}	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	30	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCKx, SOTx		2 t_{CYCP} - 30	-	2 t_{CYCP} - 30	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	External shift clock operation	2 t_{CYCP} - 10	-	2 t_{CYCP} - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	-	30	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- The above AC characteristics are for CLK synchronous mode.
- t_{CYCP} represents the APB bus clock cycle time.
  For the number of the APB bus to which Multi-function Serial has been connected, see "8. Block Diagram ".
- The characteristics are only applicable when the relocate port numbers are the same.
  For instance, they are not applicable for the combination of SCLKx_0 and SOTx_1.
- External load capacitance C_L = 30 pF

When using synchronous serial chip select (SPI = 1, SCINV = 0, MS=0, CSLVL=0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5V		V_{CC} ≥ 4.5V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↓ setup time	t_{CSSI}	Internal shift clock operation	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↑→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	ns
SCS↑→SCK↓ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCK↑→SCS↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCS↑→SOT delay time	t_{DSE}		-	40	-	40	ns
SCS↓→SOT delay time	t_{DEE}		0	-	0	-	ns

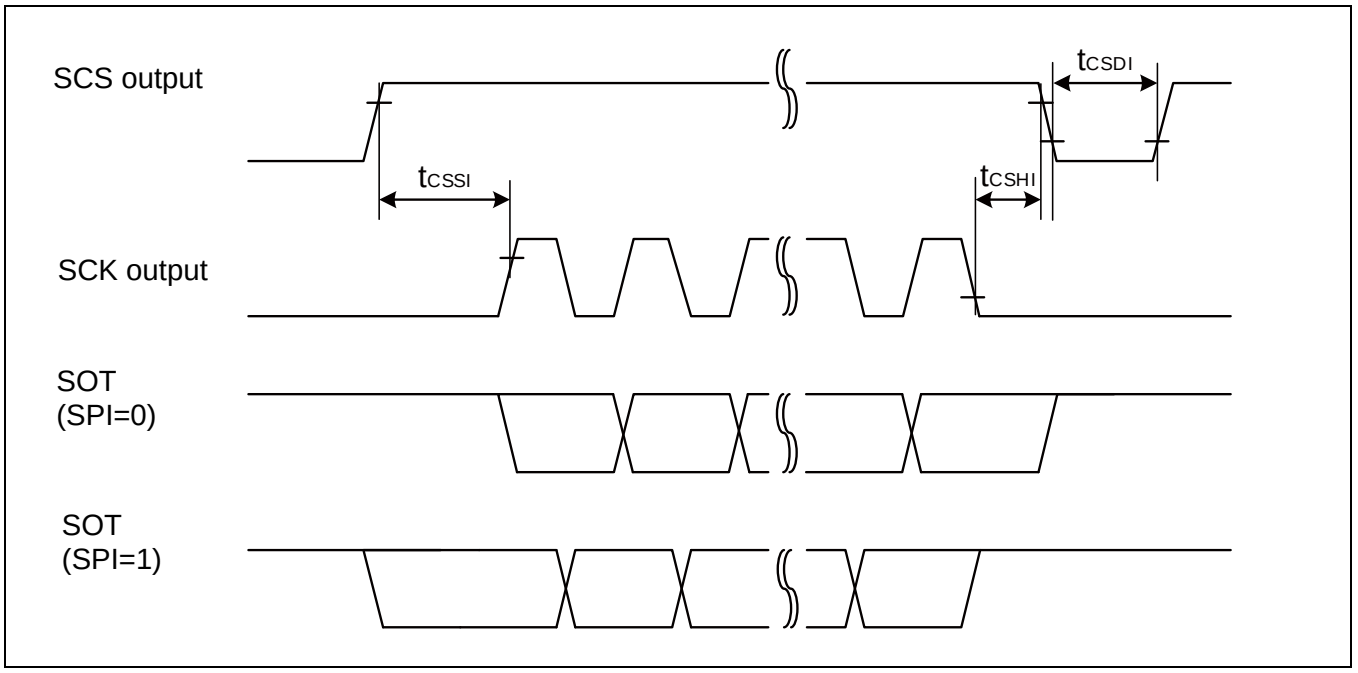
(*1): CSSU bit value × serial chip select timing operating clock cycle [ns]

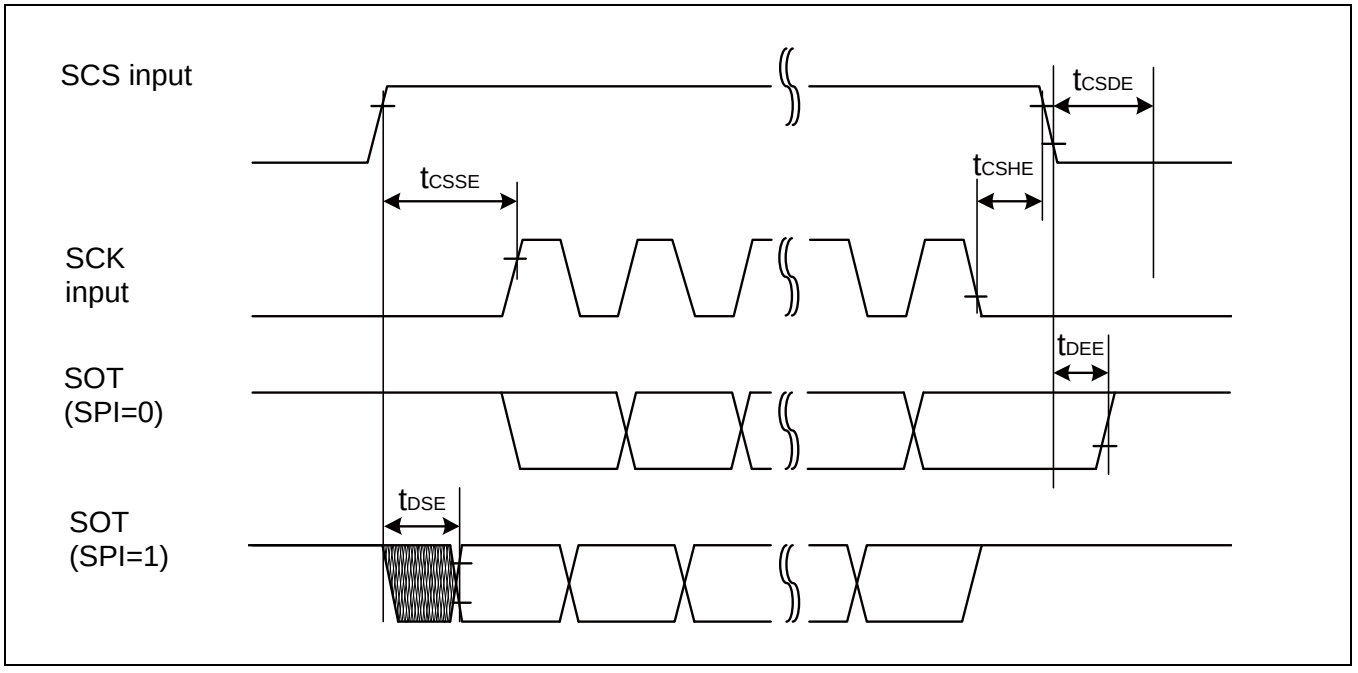
(*2): CSHD bit value × serial chip select timing operating clock cycle [ns]

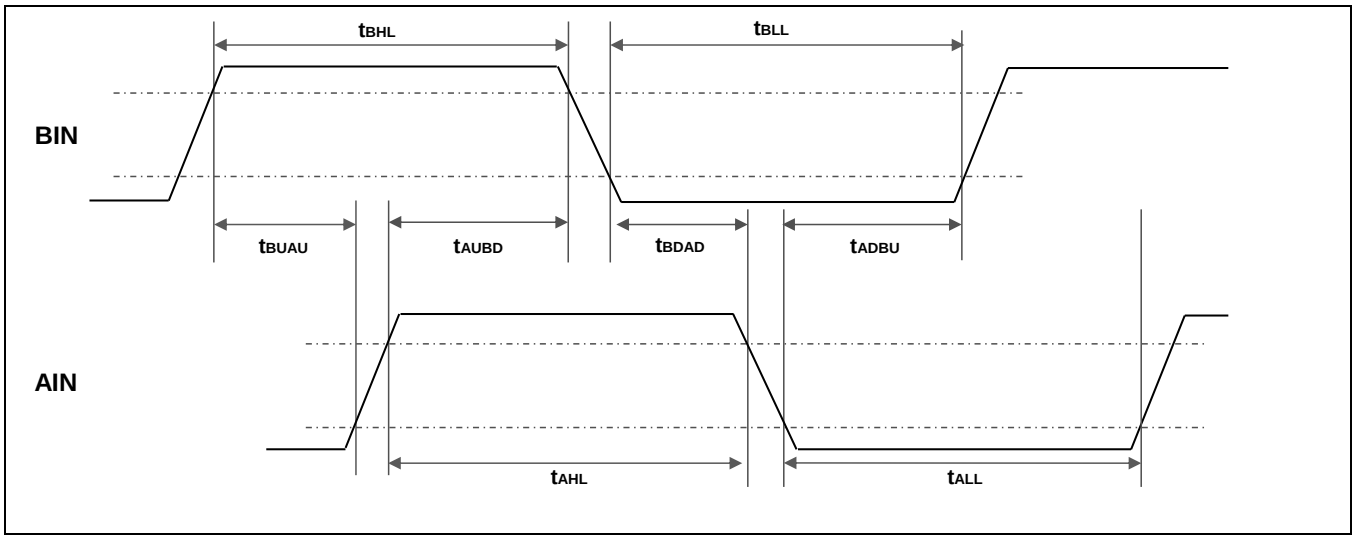
(*3): CSDS bit value × serial chip select timing operating clock cycle [ns]

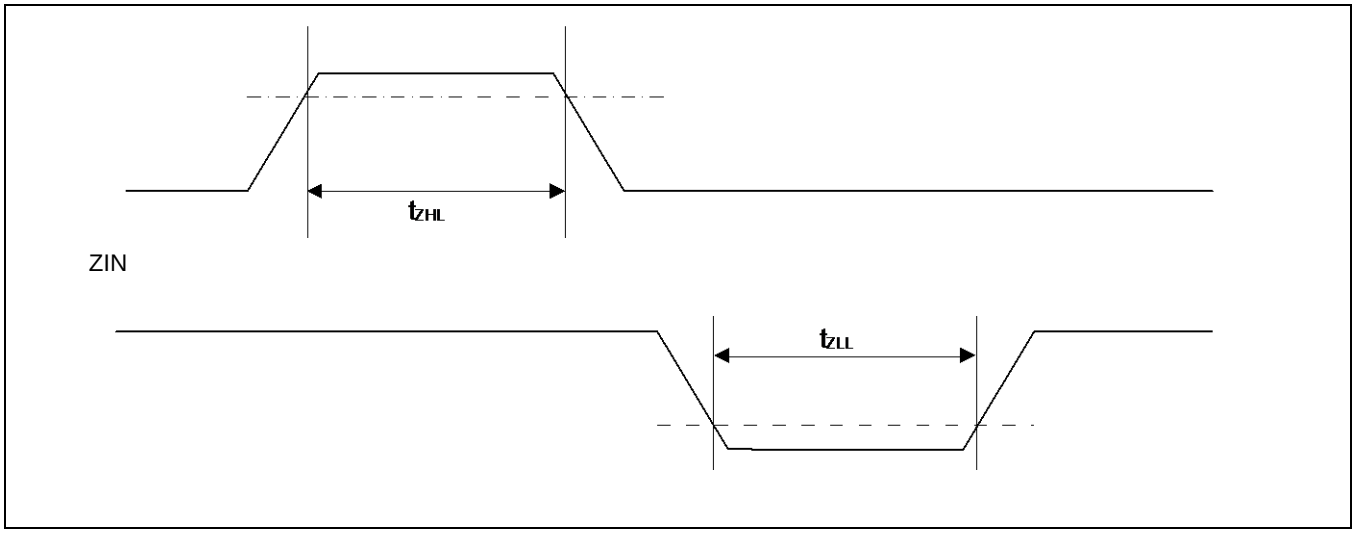
Notes:

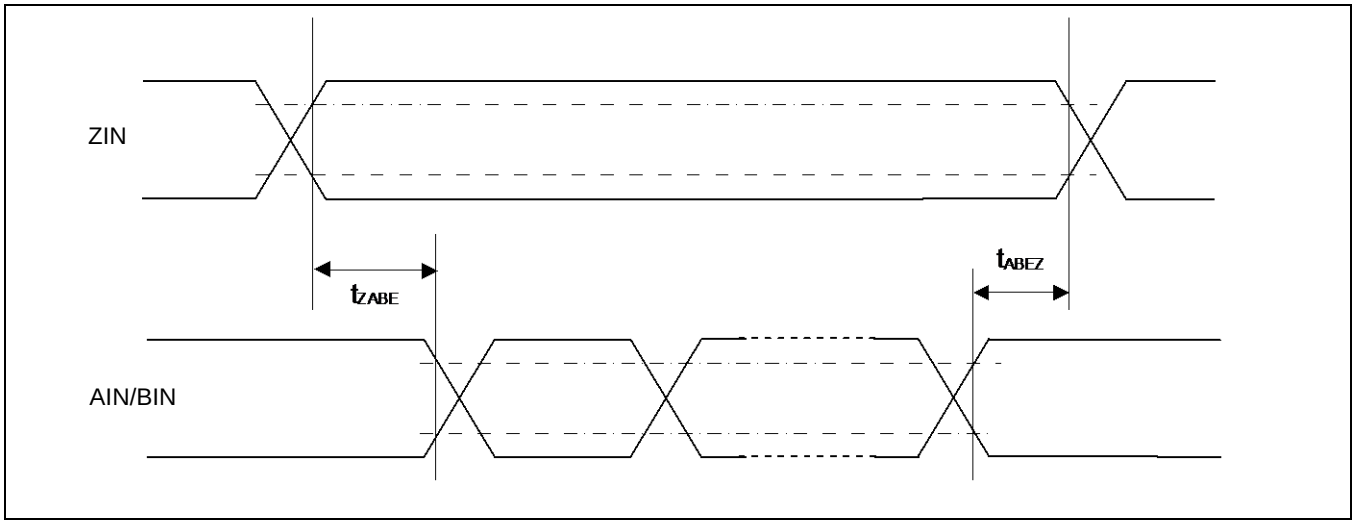
- t_{CYCP} indicates the APB bus clock cycle time.
  About the APB bus number which Multi-function Serial is connected to, see "8. Block Diagram ".
- About CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM0+ Family PERIPHERAL MANUAL".
- When the external load capacitance C_L = 30pF.

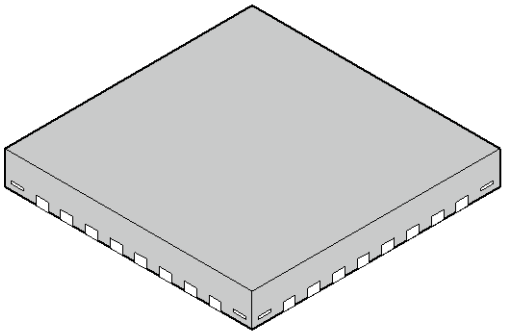

SCS output
SCK output
SOT
(SPI=0)
SOT
(SPI=1)
tCSDI
tCSSI
tCSHI


SCS input
SCK
input
SOT
(SPI=0)
SOT
(SPI=1)
tCSDE
tCSSE
tCSHE
tDEE
tDSE

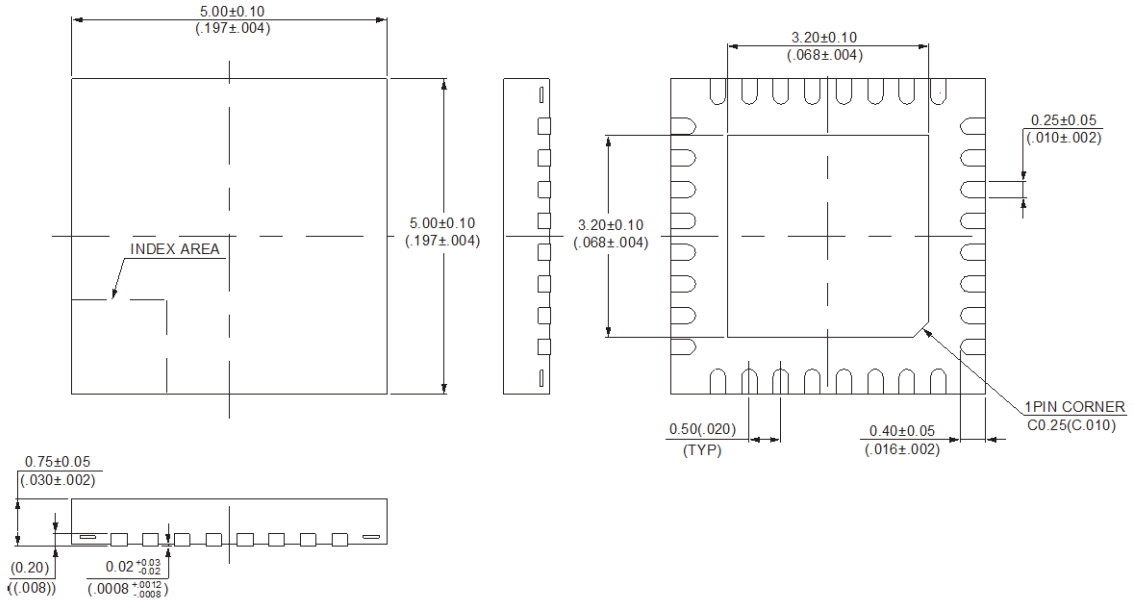

tBHL
tBLL
BIN
tBUAU
tAUBD
tBDAD
tADBU
AIN
tAHL
tALL


tZHL
ZIN
tZLL

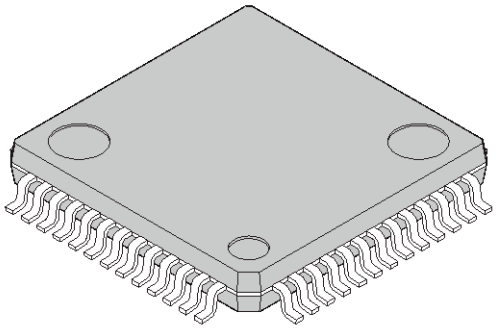

ZIN
tZABE
tABEZ
AIN/BIN

32-pin plastic QFN		
 (LCC-32P-M73)	Lead pitch	0.50 mm
	Package width × package length	5.00 mm × 5.00 mm
	Sealing method	Plastic mold
	Mounting height	0.80 mm MAX
	Weight	0.06 g

32-pin plastic QFN
(LCC-32P-M73)

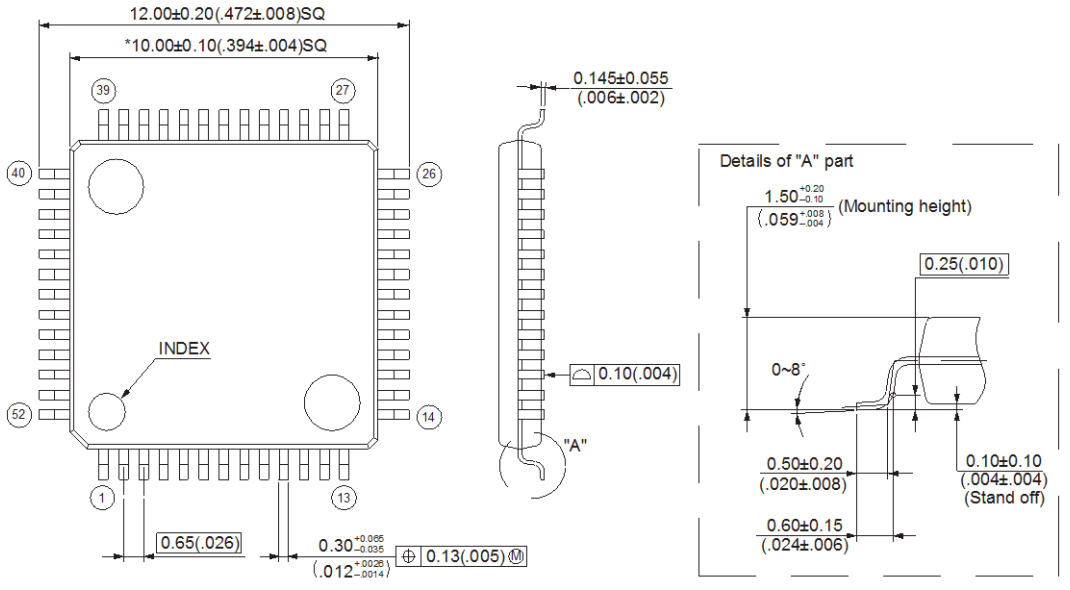


Dimensions in mm (inches).
Note: The values in parentheses are reference values.

52-pin plastic LQFP		
	Lead pitch	0.65 mm
	Package width × package length	10.00 × 10.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.32 g
(FPT-52P-M02)	Code (Reference)	P-LFQFP52-10 × 10-0.65

52-pin plastic LQFP
(FPT-52P-M02)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values

15. Major Changes

Spansion Publication Number: S6E1A1_DS710-00001

Page	Section	Change Results
Revision 0.1		
-	-	Initial release
Revision 1.0 [July 16,2014]		
-	-	Revised from "Preliminary" to "Full Production"
3	1. Description	Revised from "TYPE1" product to "TYPE1-M0+" product
5	2. Features	Revised "Processor version"
6	2. Features	Revised "Conversion time" of 12-bit A/D converter
9	3. Product Lineup	Added "Note" for accuracy of built-in CR
21,22,23, 24,25	6. List of Pin Functions List of pin functions	Revised Pin number 30 and 31 of LQFP-32 and QFN-32
23	6. List of Pin Functions List of pin functions	Revised Function description of SOT1_x(SDA1_x)
40	12. Memory Map Memory map (1)	Revised from "MTB resister" to "MTB resister(SFR)"
41	12. Memory Map Memory map (2)	Revised product name and RAM address
46	14. Electrical Characteristics 14.1 Absolute Maximum Ratings	Revised Analog pin input voltage
47	14. Electrical Characteristics 14.2 Recommended Operating Conditions	Added note "*2"
48,49,50	14. Electrical Characteristics 14.3 DC Characteristics 14.3.1 Current Rating	• Revised and added "Conditions" • Revised the value of "TBD"
52	14. Electrical Characteristics 14.4 AC Characteristics 14.4.1 Main Clock Input Characteristics	Revised the value of "Internal operating clock frequency" and "Internal operating clock cycle time"
54	14. Electrical Characteristics 14.4 AC Characteristics 14.4.3 Built-in CR Oscillation Characteristics	Revised the value of "TBD"
55	14. Electrical Characteristics 14.4 AC Characteristics 14.4.5 Operating Conditions of Main PLL(In the case of using the built-in high-speed CR clock as the input clock of the main PLL)	• Revised the value of "TBD" • Revised the maximum value of "Main PLL clock frequency"
56	14. Electrical Characteristics 14.4 AC Characteristics 14.4.7 Power-on Reset Timing	• Revised the value of "TBD" • Revised from "LVDL_minimum" to "VDH_minimum"
78	14. Electrical Characteristics 14.4 AC Characteristics 14.4.12 I2C Timing	• Revised the condition of "Noise filter" • Revised the note for noise filter
80	14. Electrical Characteristics 14.5 12-bit A/D Converter	• Revised the value of "Conversion time", "Sampling time" and "Compare clock cycle" • Revised the value of "State transition time to operation permission" • Revised the note
83,84	14. Electrical Characteristics 14.6 Low-voltage Detection Characteristics	Revised the value of SVHR and SVHI
85	14. Electrical Characteristics 14.7 Flash Memory Write/Erase Characteristics	• Revised the value of "TBD" • Revised the value of typical