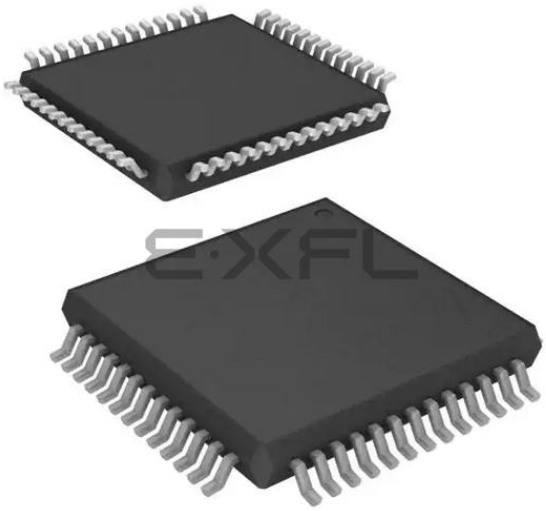


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

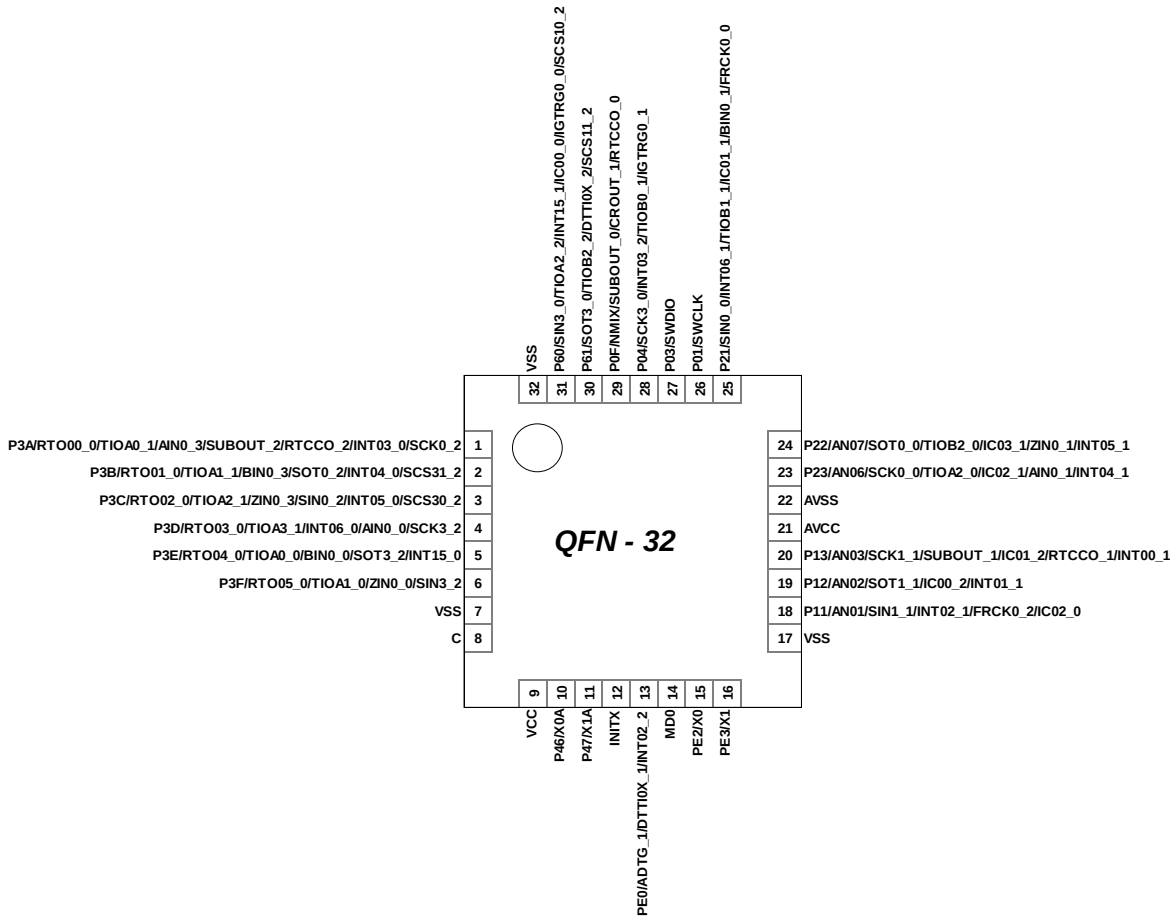
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CSIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	88KB (88K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LQFP
Supplier Device Package	52-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e1a12c0agf20000

LCC-32P-M73

(TOP VIEW)

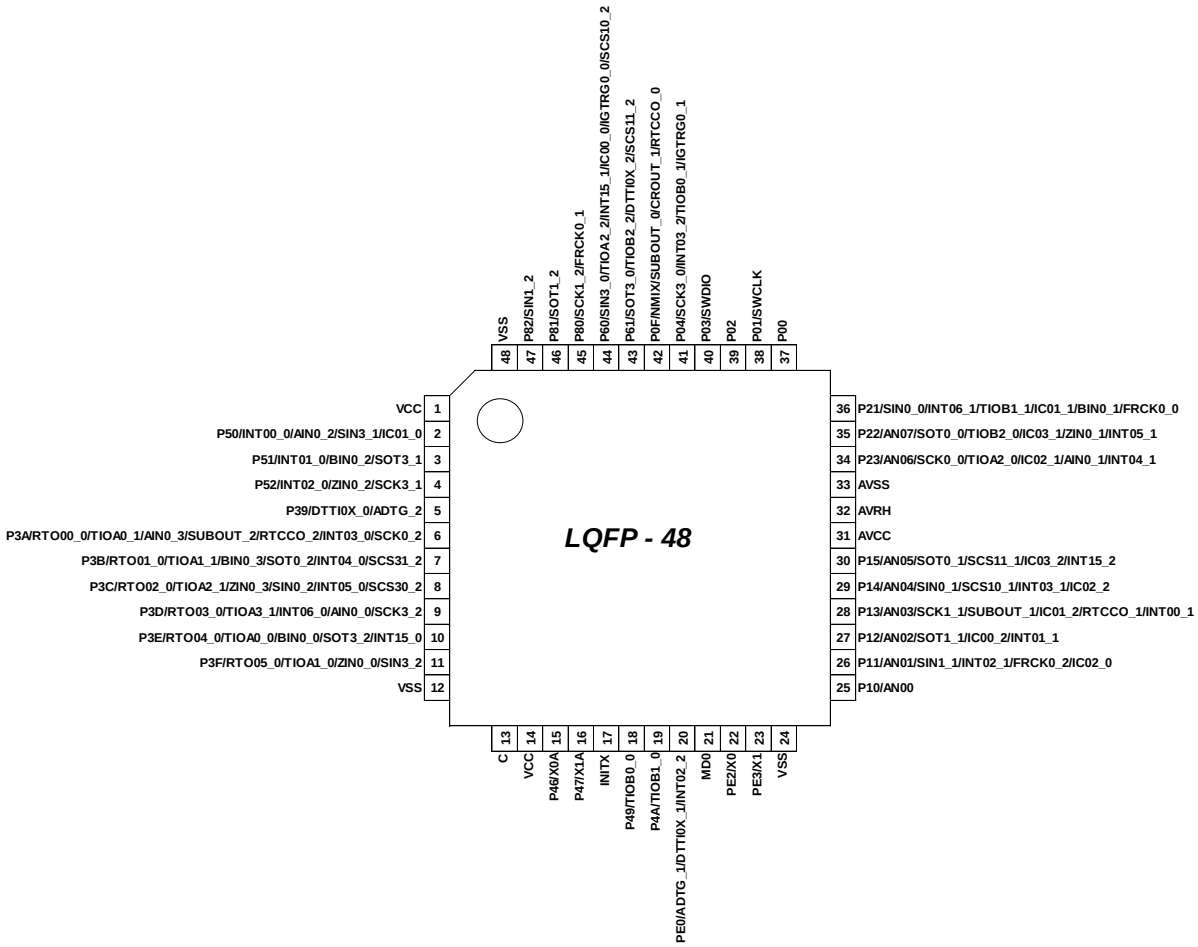


Note:

- The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.
  Use the extended port function register (EPFR) to select the pin.

FPT-48P-M49

(TOP VIEW)



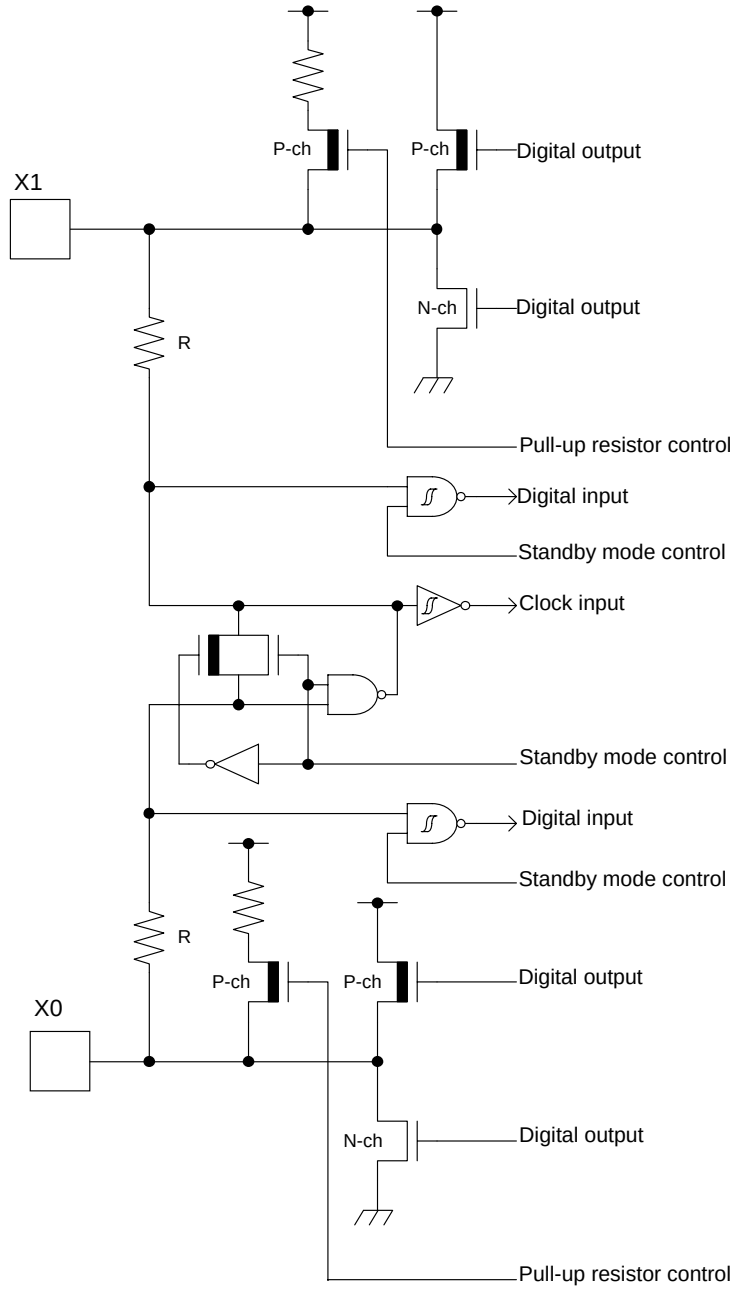
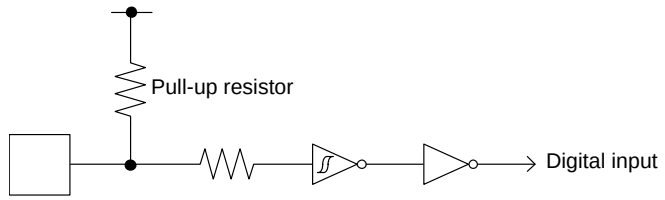
Note:

- The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.
  Use the extended port function register (EPFR) to select the pin.

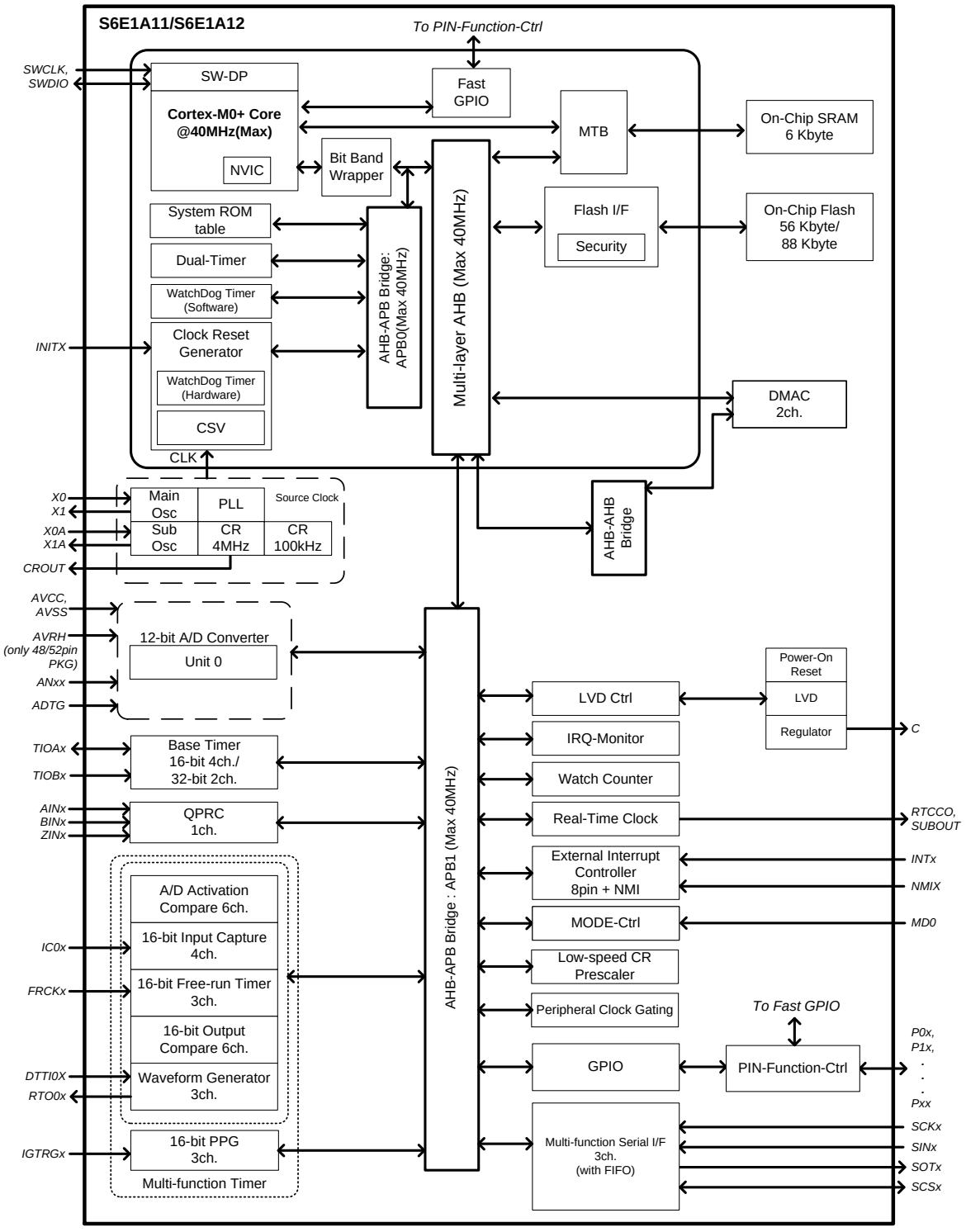
Pin no.			Pin name	I/O circuit type	Pin state type
LQFP-52	LQFP-48 QFN-48	LQFP-32 QFN-32			
9	8	3	P3C RTO02_0 TIOA2_1 ZIN0_3 SIN0_2 INT05_0 SCS30_2	F	J
10	9	4	P3D RTO03_0 TIOA3_1 INT06_0 AIN0_0 SCK3_2	F	J
11	10	5	P3E RTO04_0 TIOA0_0 BIN0_0 SOT3_2 INT15_0	F	J
12	11	6	P3F RTO05_0 TIOA1_0 ZIN0_0 SIN3_2	F	I
13	12	7	VSS	-	
14	13	8	C	-	
15	14	9	VCC	-	
16	15	10	P46 X0A	D	E
17	16	11	P47 X1A	D	F
18	17	12	INITX	B	C
19	18	-	P49 TIOB0_0	E	I
20	19	-	P4A TIOB1_0	E	I

Pin function	Pin name	Function description	Pin no.		
			LQFP-52	LQFP-48 QFN-48	LQFP-32 QFN-32
GPIO	P00	General-purpose I/O port 0	41	37	-
	P01		42	38	26
	P02		43	39	-
	P03		44	40	27
	P04		45	41	28
	P0F		46	42	29
	P10	General-purpose I/O port 1	27	25	-
	P11		28	26	18
	P12		29	27	19
	P13		30	28	20
	P14		31	29	-
	P15		32	30	-
	P21	General-purpose I/O port 2	39	36	25
	P22		38	35	24
	P23		37	34	23
	P39	General-purpose I/O port 3	6	5	-
	P3A		7	6	1
	P3B		8	7	2
	P3C		9	8	3
	P3D		10	9	4
	P3E		11	10	5
	P3F		12	11	6
GPIO	P46	General-purpose I/O port 4	16	15	10
	P47		17	16	11
	P49		19	18	-
	P4A		20	19	-
	P50	General-purpose I/O port 5	2	2	-
	P51		3	3	-
	P52		4	4	-
	P60	General-purpose I/O port 6	48	44	31
	P61		47	43	30
	P80	General-purpose I/O port 8	49	45	-
	P81		50	46	-
	P82		51	47	-
	PE0*	General-purpose I/O port E	22	20	13
	PE2		24	22	15
	PE3		25	23	16

5. I/O Circuit Type

Type	Circuit	Remarks
A		It is possible to select the main oscillation / GPIO function When the main oscillation is selected. • Oscillation feedback resistor : Approximately 1MΩ • With standby mode control When the GPIO is selected. • CMOS level output. • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50kΩ • I_{OH}= -4mA, I_{OL}= 4mA
B		• CMOS level hysteresis input • Pull-up resistor : Approximately 50kΩ

8. Block Diagram



List of Pin Status

Pin status type	Function group	State upon power-on reset or low-voltage detection	State at INITX input	State upon device internal reset	State in Run mode or SLEEP mode	State in TIMER mode, RTC mode, or STOP mode	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable	
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1	
		-	-	-	-	SPL = 0	SPL = 1
A	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"
	Main crystal oscillator input pin/ External main clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
B	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"
	External main clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"
	Main crystal oscillator output pin	Hi-Z / Internal input fixed at "0"/ Input enabled	Hi-Z / Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	Maintain previous state/When oscillation stops*[1], Hi-Z / Internal input fixed at "0"	Maintain previous state/When oscillation stops*[1], Hi-Z / Internal input fixed at "0"	Maintain previous state/When oscillation stops*[1], Hi-Z / Internal input fixed at "0"
C	INITX input pin	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled
D	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
E	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"
	Sub crystal oscillator input pin / External sub clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
F	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"
	External sub clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"

Pin status type	Function group	State upon power-on reset or low-voltage detection	State at INITX input	State upon device internal reset	State in Run mode or SLEEP mode	State in TIMER mode, RTC mode, or STOP mode	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable	
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1	
		-	-	-	-	SPL = 0	SPL = 1
	Sub crystal oscillator output pin	Hi-Z / Internal input fixed at "0"/ Input enabled	Hi-Z / Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	Maintain previous state	Maintain previous state/When oscillation stops*2, Hi-Z / Internal input fixed at "0"	Maintain previous state/When oscillation stops*2, Hi-Z / Internal input fixed at "0"
G	NMIX selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state
	Resource other than the above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at "0"
	GPIO selected						
H	Serial wire debug selected	Hi-Z	Pull-up / Input enabled	Pull-up / Input enabled	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected	Setting disabled	Setting disabled	Setting disabled			Hi-Z / Internal input fixed at "0"
I	Resource selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"
	GPIO selected						
J	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state
	Resource other than the above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at "0"
	GPIO selected						
K	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled
	Resource other than the above selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"
	GPIO selected						
L	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled

12.2 Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0.0V)

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Power supply voltage	V_{CC}	-	2.7*2	5.5	V	
Analog power supply voltage	AV_{CC}	-	2.7	5.5	V	AV_{CC} = V_{CC}
Analog reference voltage	AVRH	-	2.7	AV_{CC}	V	Only S6E1A1xC0A
Smoothing capacitor	C_S	-	1	10	µF	For regulator*1
Operating temperature	Ta	-	- 40	+ 105	°C	

“1: See "C Pin" in "6. Handling Precautions" for the connection of the smoothing capacitor.

*2: In between less than the minimum power supply voltage and low voltage reset/interrupt detection voltage or more, instruction execution and low voltage detection function by built-in High-speed CR(including Main PLL is used) or built-in Low-speed CR is possible to operate only.

Warning

1. The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.
2. Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.
3. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet.
4. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

12.3 DC Characteristics

12.3.1 Current Rating

Symbol (Pin name)	Conditions		HCLK Frequency *4	Value Typ*1	Value Max*2	Unit	Remarks
Icc (VCC)	Run mode, code executed from Flash	4MHz external clock input, PLL ON*8 NOP code executed Built-in high speed CR stopped All peripheral clock stopped by CKENx	4MHz	0.7	1.5	mA	*3
			8MHz	1.3	2.3		
			20MHz	2.8	4.0		
			40MHz	5.7	7.3		
		4MHz external clock input, PLL ON*8 Benchmark code executed Built-in high speed CR stopped PCLK1 stopped	4MHz	0.6	1.4	mA	*3
			8MHz	1.2	2.1		
			20MHz	2.6	3.7		
			40MHz	4.8	6.3		
		4MHz crystal oscillation, PLL ON*8 NOP code executed Built-in high speed CR stopped All peripheral clock stopped by CKENx	4MHz	1.0	2.9	mA	*3
			8MHz	1.7	3.6		
			20MHz	3.4	5.6		
			40MHz	5.7	8.2		
	Run mode, code executed from RAM	4MHz external clock input, PLL ON*8 NOP code executed Built-in high speed CR stopped All peripheral clock stopped by CKENx	4MHz	0.5	1.2	mA	*3
			8MHz	0.9	1.8		
			20MHz	2.0	2.9		
			40MHz	3.7	4.8		
	Run mode, code executed from Flash	4MHz external clock input, PLL ON NOP code executed Built-in high speed CR stopped PCLK1 stopped	40MHz	2.8	3.7	mA	*3,*6,*7
	Run mode, code executed from Flash	Built-in high speed CR*5 NOP code executed All peripheral clock stopped by CKENx	4MHz	0.8	1.5	mA	*3
		32kHz crystal oscillation NOP code executed All peripheral clock stopped by CKENx	32kHz	65	900	µA	*3
		Built-in low speed CR NOP code executed All peripheral clock stopped by CKENx	100kHz	73	920	µA	*3
Iccs (VCC)	SLEEP operation	4MHz external clock input, PLL ON*8 All peripheral clock stopped by CKENx	4MHz	0.4	1.2	mA	*3
			8MHz	0.7	1.6		
			20MHz	1.5	2.4		
			40MHz	2.7	3.7		
		Built-in high speed CR*5 All peripheral clock stopped by CKENx	4MHz	0.5	1.2	mA	*3
		32kHz crystal oscillation All peripheral clock stopped by CKENx	32kHz	63	880	µA	*3
		Built-in low speed CR All peripheral clock stopped by CKENx	100kHz	66	890	µA	*3

LVD current

(V_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Low-Voltage detection circuit (LVD) power supply current	I_{CCLVD}	VCC	At operation	0.13	0.3	µA	For occurrence of reset
				0.13	0.3	µA	For occurrence of interrupt

Flash memory current

(V_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Flash memory write/erase current	$I_{CCFLASH}$	VCC	At Write/Erase	9.5	11.2	mA	

A/D convertor current (S6E1A1xC0A)

(V_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Power supply current	I_{CCAD}	AVCC	At operation	0.7	0.9	mA	
			At stop	0.13	13	µA	
Reference power supply current (AVRH)	I_{CCAVRH}	AVRH	At operation	1.1	1.97	mA	AVRH=5.5V
			At stop	0.1	1.7	µA	

A/D convertor current (S6E1A1xB0A)

(V_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Power supply current	I_{CCAD}	AVCC	At operation	1.8	2.87	mA	
			At stop	0.23	14.7	µA	

Peripheral current dissipation

Clock system	Peripheral	Conditions	Frequency (MHz)				Unit	Remarks
			4	8	20	40		
HCLK	GPIO	At all ports operation	0.11	0.22	0.55	1.10	mA	
	DMAC	At 2ch operation	0.05	0.11	0.25	0.51		
PCLK1	Base timer	At 4ch operation	0.03	0.05	0.15	0.30	mA	
	Multi-functional timer/PPG	At 1unit/4ch operation	0.14	0.28	0.68	1.38		
	Quadrature position/Revolution counter	At 1unit operation	0.02	0.04	0.11	0.22		
	ADC	At 1unit operation	0.07	0.14	0.37	0.73		
	Multi-function serial	At 1ch operation	0.15	0.31	0.77	1.54		

When using synchronous serial chip select (SPI = 1, SCINV = 1, MS=0, CSLVL=0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5V		V_{CC} ≥ 4.5V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↑ setup time	t_{CSSI}	Internal shift clock operation	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↓→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	ns
SCS↑→SCK↑ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCK↓→SCS↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCS↑→SOT delay time	t_{DSE}		-	40	-	40	ns
SCS↓→SOT delay time	t_{DEE}		0	-	0	-	ns

(*1): CSSU bit value × serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value × serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value × serial chip select timing operating clock cycle [ns]

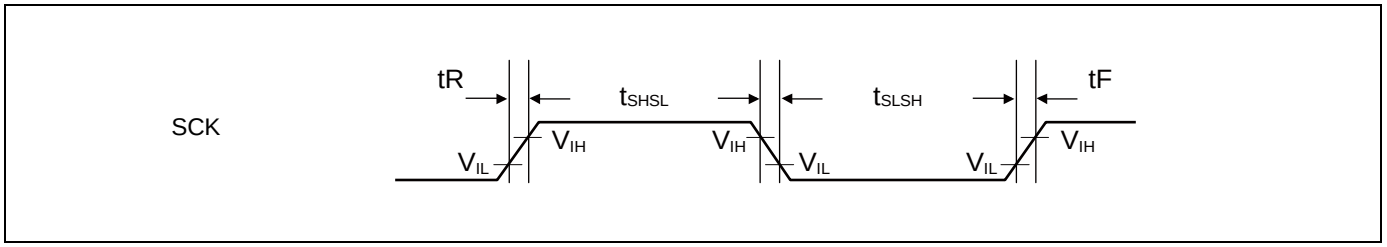
Notes:

- t_{CYCP} indicates the APB bus clock cycle time.
  About the APB bus number which Multi-function Serial is connected to, see "8. Block Diagram ".
- About CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM0+ Family PERIPHERAL MANUAL".
- When the external load capacitance C_L = 30pF.

External clock (EXT = 1): asynchronous only

(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Serial clock "L" pulse width	t_{SLSH}	C_L = 30 pF	t_{CYCP} + 10	-	ns	
Serial clock "H" pulse width	t_{SHSL}		t_{CYCP} + 10	-	ns	
SCK falling time	tF		-	5	ns	
SCK rising time	tR		-	5	ns	

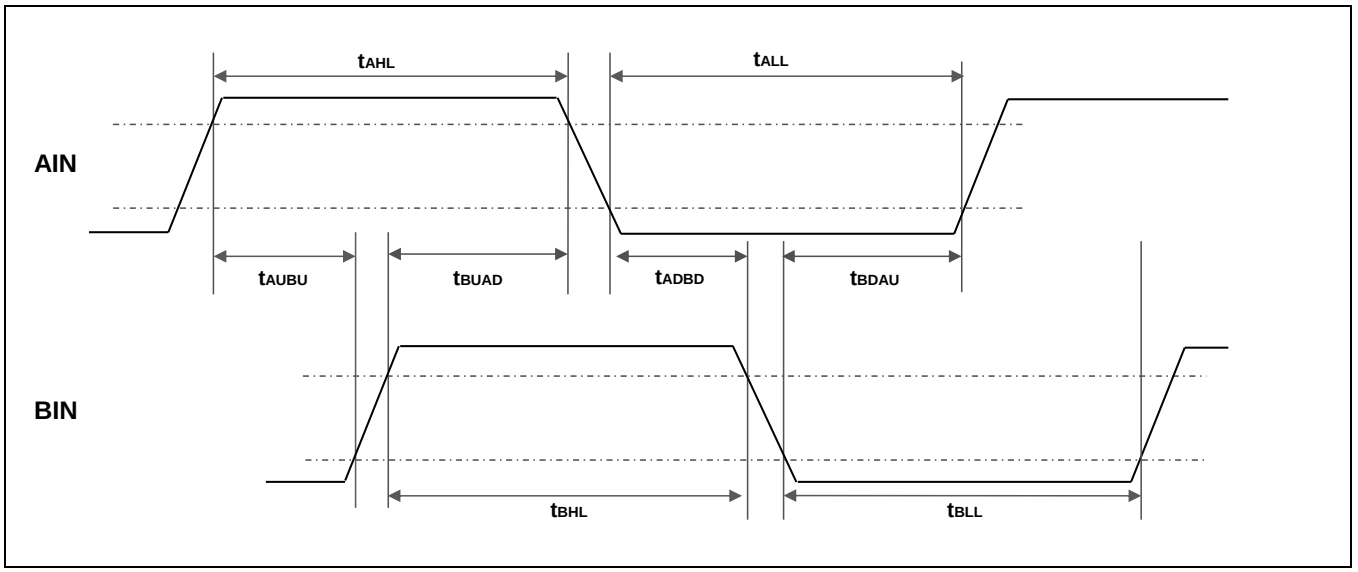


12.4.11 QPRC Timing

(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
AIN pin "H" width	t_{AHL}	-	2 t_{CYCP}*	-	ns
AIN pin "L" width	t_{ALL}	-			
BIN pin "H" width	t_{BHL}	-			
BIN pin "L" width	t_{BLL}	-			
Time from AIN pin "H" level to BIN rise	t_{AUBU}	PC_Mode2 or PC_Mode3			
Time from BIN pin "H" level to AIN fall	t_{BUAD}	PC_Mode2 or PC_Mode3			
Time from AIN pin "L" level to BIN fall	t_{ADBD}	PC_Mode2 or PC_Mode3			
Time from BIN pin "L" level to AIN rise	t_{BDAU}	PC_Mode2 or PC_Mode3			
Time from BIN pin "H" level to AIN rise	t_{BUAU}	PC_Mode2 or PC_Mode3			
Time from AIN pin "H" level to BIN fall	t_{AUBD}	PC_Mode2 or PC_Mode3			
Time from BIN pin "L" level to AIN fall	t_{BDAD}	PC_Mode2 or PC_Mode3			
Time from AIN pin "L" level to BIN rise	t_{ADBU}	PC_Mode2 or PC_Mode3			
ZIN pin "H" width	t_{ZHL}	QCR:CGSC="0"			
ZIN pin "L" width	t_{ZLL}	QCR:CGSC="0"			
Time from determined ZIN level to AIN/BIN rise and fall	t_{ZABE}	QCR:CGSC="1"			
Time from AIN/BIN rise and fall time to determined ZIN level	t_{ABEZ}	QCR:CGSC="1"			

*: t_{CYCP} represents the APB bus clock cycle time except when the APB bus clock stops in STOP mode or in TIMER mode. For the number of the APB bus to which the QPRC is connected, see "8. Block Diagram".



12.5 12-bit A/D Converter

Electrical characteristics of A/D Converter

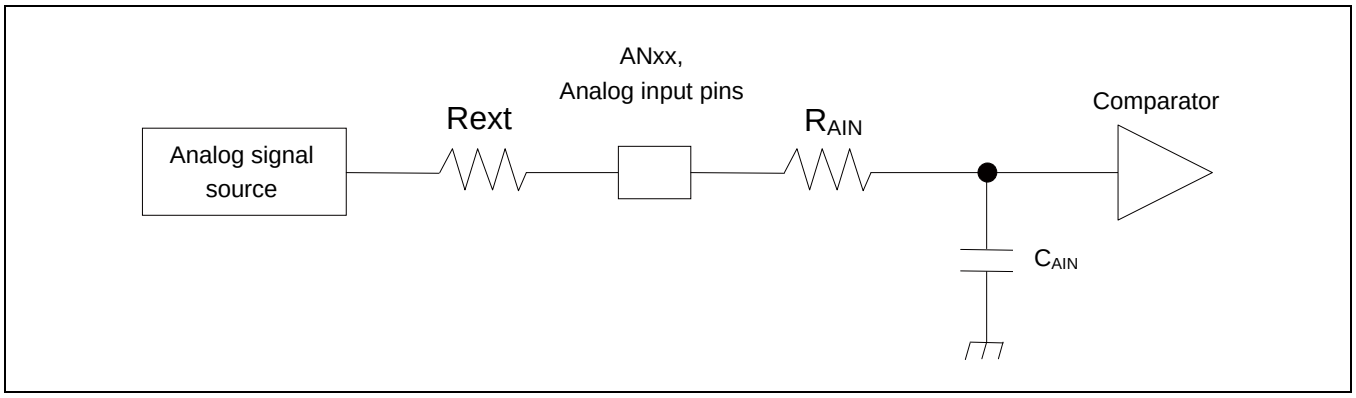
(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Integral Nonlinearity	-	-	- 4.5	-	4.5	LSB	
Differential Nonlinearity	-	-	- 2.5	-	+ 2.5	LSB	
Zero transition voltage	V_{ZT}	ANxx	- 20	-	+ 20	mV	
Full-scale transition voltage	V_{FST}	ANxx	AVRH - 20	-	AVRH+ 20	mV	S6E1A1xC0A
			AV_{CC}-20	-	AV_{CC}+20		S6E1A1xB0A
Conversion time	-	-	0.8*1	-	-	μs	S6E1A1xC0A AV_{CC} ≥ 4.5V
			2.0*1	-	-		S6E1A1xB0A
Sampling time*2	Ts	-	0.24	-	10	μs	S6E1A1xC0A AV_{CC} ≥ 4.5V
			0.5				S6E1A1xC0A AV_{CC} < 4.5V
			0.6				S6E1A1xB0A
Compare clock cycle*3	Tcck	-	40	-	1000	ns	S6E1A1xC0A AV_{CC} ≥ 4.5V
			50				S6E1A1xC0A AV_{CC} < 4.5V
			100				S6E1A1xB0A
State transition time to operation permission	Tstt	-	-	-	1.0	μs	
Analog input capacity	C_{AIN}	-	-	-	9.7	pF	
Analog input resistance	R_{AIN}	-	-	-	1.6	kΩ	AV_{CC} ≥ 4.5V
					2.3		AV_{CC} < 4.5V
Interchannel disparity	-	-	-	-	4	LSB	
Analog port input current	-	ANxx	-	-	5	μA	
Analog input voltage	-	ANxx	AV_{SS}	-	AVRH	V	S6E1A1xC0A
			AV_{SS}	-	AV_{CC}		S6E1A1xB0A
Reference voltage	-	AVRH	2.7	-	AV_{CC}	V	Only S6E1A1xB0A

*1: The conversion time is the value of "sampling time (Ts) + compare time (Tc)".
The minimum conversion time is computed according to the following conditions: sampling time = 240 ns, compare time = 560 ns (AVcc ≥ 4.5 V). Must be set 25MHz to the Base clock (HCLK).
Ensure that the conversion time satisfies the specifications of the sampling time (Ts) and compare clock cycle (Tcck).
For details of the settings of the sampling time and compare clock cycle, refer to "CHAPTER: A/D Converter" in "FM0+ Family PERIPHERAL MANUAL Analog Macro Part".
The register settings of the A/D Converter are reflected in the operation according to the APB bus clock timing.
For the number of the APB bus to which the A/D Converter is connected, see "8. Block Diagram".
The base clock (HCLK) is used to generate the sampling time and the compare clock cycle.

*2: The required sampling time varies according to the external impedance.
Set a sampling time that satisfies (Equation 1).

*3: The compare time (Tc) is the result of (Equation 2).



(Equation 1) $Ts \geq (R_{AIN} + Rext) \times C_{AIN} \times 9$

Ts:	Sampling time
R_{AIN}:	Input resistance of A/D Converter = 1.6 kΩ with 4.5 < AVCC < 5.5 ch.1 to ch.5
	Input resistance of A/D Converter = 1.4 kΩ with 4.5 < AVCC < 5.5 ch.0, ch.6, ch.7
	Input resistance of A/D Converter = 2.3 kΩ with 2.7 < AVCC < 4.5 ch.1 to ch.5
	Input resistance of A/D Converter = 2.0 kΩ with 2.7 < AVCC < 4.5 ch.0, ch.6, ch.7
CAIN:	Input capacitance of A/D Converter = 9.7 pF with 2.7 < AVCC < 5.5
Rext:	Output impedance of external circuit

(Equation 2) $Tc = Tcck \times 14$

Tc:	Compare time
Tcck:	Compare clock cycle

12.7 Flash Memory Write/Erase Characteristics

(V_{CC} = 2.7 V to 5.5 V, Ta = - 40°C to + 105°C)

Parameter		Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	Large sector	-	0.7	2.2	s	The sector erase time includes the time of writing prior to internal erase.
	Small sector		0.3	0.9		
Halfword (16-bit) write time		-	30	528	µs	The halfword (16-bit) write time excludes the system-level overhead.
Chip erase time		-	2.6	8	s	The chip erase time includes the time of writing prior to internal erase.

Write/erase cycle and data hold time

Write/erase cycle	Data hold time (year)	Remarks
1,000	20*	
10,000	10*	

*: This value was converted from the result of a technology reliability assessment. (This value was converted from the result of a high temperature accelerated test using the Arrhenius equation with the average temperature value being + 85°C).

12.8.2 Return Factor: Reset

The return time from Low-Power consumption mode is indicated as follows. It is from releasing reset to starting the program operation.

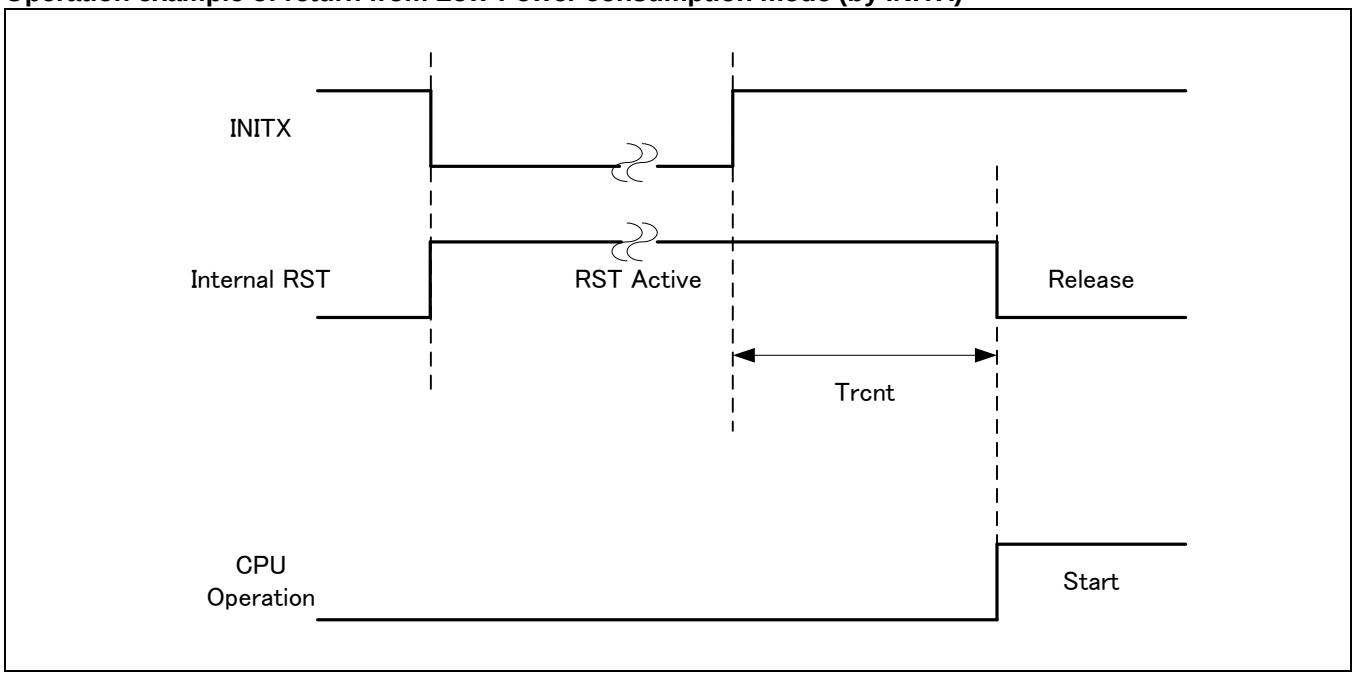
Return Count Time

(V_{CC} = 2.7V to 5.5V, Ta = - 40°C to + 105°C)

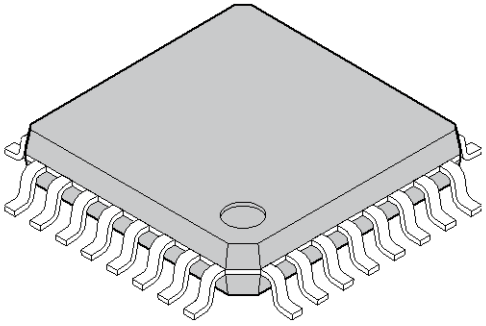
Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
SLEEP mode	Trcnt	208	378	µs	
High-speed CR TIMER mode, Main TIMER mode, PLL TIMER mode		208	378	µs	
Low-speed CR TIMER mode		398	758	µs	
Sub TIMER mode		490	849	µs	
RTC/STOP mode		288	538	µs	

*: The maximum value depends on the accuracy of built-in CR.

Operation example of return from Low-Power consumption mode (by INITX)

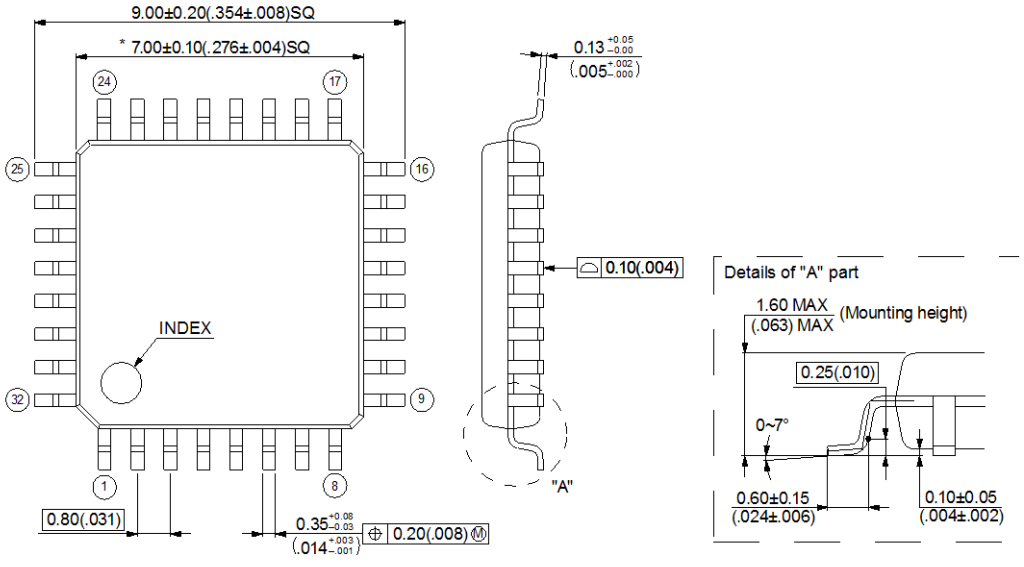


14. Package Dimensions

32-pin plastic LQFP		
 (FPT-32P-M30)	Lead pitch	0.80 mm
	Package width × package length	7.00 mm × 7.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.60 mm MAX

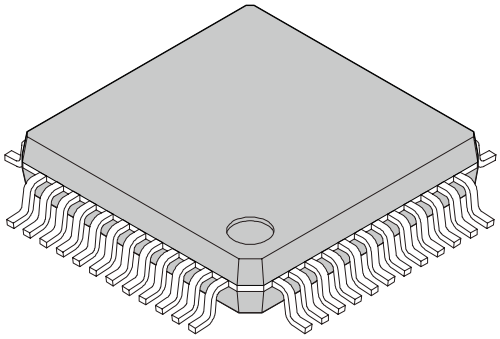
32-pin plastic LQFP
(FPT-32P-M30)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference **values.**

48-pin plastic LQFP

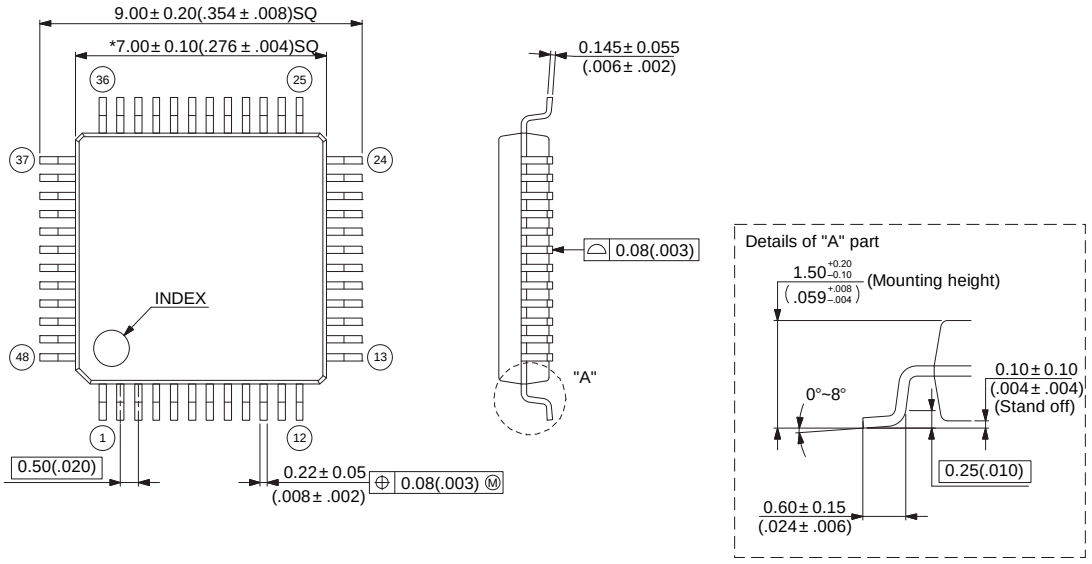


(FPT-48P-M49)

Lead pitch	0.50 mm
Package width × package length	7.00 mm × 7.00 mm
Lead shape	Gullwing
Lead bend direction	Normal bend
Sealing method	Plastic mold
Mounting height	1.70 mm MAX
Weight	0.17 g

48-pin plastic LQFP
(FPT-48P-M49)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.