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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CSIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	88KB (88K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-WFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e1a12c0agn2b000

A/D Converter (Max: 8 channels)

- 12-bit A/D Converter
  - Successive approximation type
  - Conversion time: 0.8 µs @ 5 V (S6E1A1xC0A) / 2.0 µs (S6E1A1xB0A)
  - Priority conversion available (2 levels of priority)
  - Scan conversion mode
  - Built-in FIFO for conversion data storage (for scan conversion: 16 steps, for priority conversion: 4 steps)

Base Timer (Max: 4 channels)

The operation mode of each channel can be selected from one of the following.

- 16-bit PWM timer
- 16-bit PPG timer
- 16/32-bit reload timer
- 16/32-bit PWC timer

General-purpose I/O Port

This series can use its pin as a general-purpose I/O port when it is not used for an external bus or a peripheral function. All ports can be set to fast general-purpose I/O ports or slow general-purpose I/O ports. In addition, this series has a port relocate function that can set to which I/O port a peripheral function can be allocated.

- All ports are Fast GPIO which can be accessed by 1cycle
- Capable of controlling the pull-up of each pin
- Capable of reading pin level directly
- Port relocate function
- Up to 37 fast general-purpose I/O ports @48pin package
- Certain ports are 5 V tolerant.

  See "3. Pin Assignment" and "5. I/O Circuit Type" for details of such pins.

Dual Timer (32/16-bit Down Counter)

The Dual Timer consists of two programmable 32/16-bit down counters. The operation mode of each timer channel can be selected from one of the following.

- Free-running mode
- Periodic mode (= Reload mode)
- One-shot mode

Quadrature Position/Revolution Counter (QPRC)

The Quadrature Position/Revolution Counter (QPRC) is used to measure the position of the position encoder. In addition, it can be used as an up/down counter.

- The detection edge for the three external event input pins AIN, BIN and ZIN is configurable.
- 16-bit position counter
- 16-bit revolution counter
- Two 16-bit compare registers

Multi-function Timer

The Multi-function Timer consists of the following blocks.

- 16-bit free-run timer × 3 channels
- Input capture × 4 channels
- Output compare × 6 channels
- ADC start compare × 6 channel
- Waveform generator × 3 channels
- 16-bit PPG timer × 3 channels

  IGBT mode is contained.

The following function can be used to achieve the motor control.

- PWM signal output function
- DC chopper waveform output function
- Dead time function
- Input capture function
- ADC start function
- DTIF (motor emergency stop) interrupt function

Real-time Clock (RTC)

The Real-time Clock counts year/month/day/hour/minute/second/day of the week from year 01 to year 99.

- The RTC can generate an interrupt at a specific time (year/month/day/hour/minute/second/day of the week) and can also generate an interrupt in a specific year, in a specific month, on a specific day, at a specific hour or at a specific minute.
- It has a timer interrupt function generating an interrupt upon a specific time or at specific intervals.
- It can keep counting while rewriting the time.
- It can count leap years automatically.

Contents

1. Product Lineup

Memory Size

Product name	S6E1A11B0A S6E1A11C0A	S6E1A12B0A S6E1A12C0A
On-chip Flash memory	56 Kbyte	88 Kbyte
On-chip SRAM	6 Kbyte	6 Kbyte

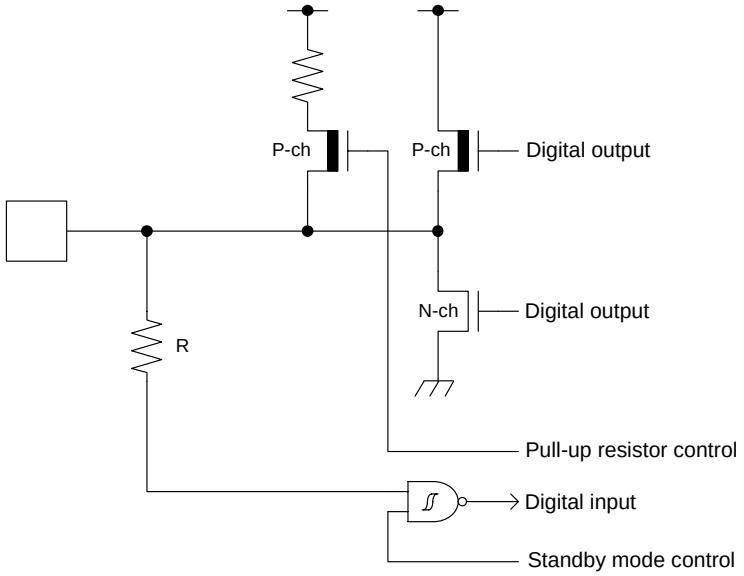
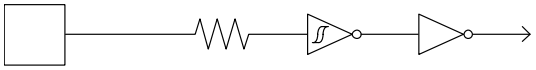
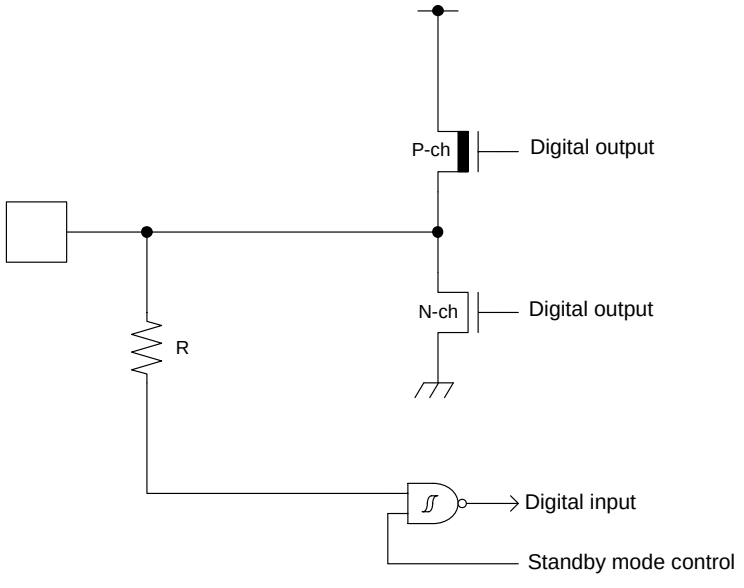
Function

Product name			S6E1A11B0A S6E1A12B0A	S6E1A11C0A S6E1A12C0A
Pin count			32	48/52
CPU			Cortex-M0+	
	Frequency		40 MHz	
Power supply voltage range			2.7 V to 5.5 V	
DMAC			2 ch.	
Multi-function Serial Interface (UART/CSIO/I^{2}C)			3 ch. (Max) ch.0/ch.1/ch.3: FIFO	
Base Timer (PWC/Reload timer/PWM/PPG)			4 ch. (Max)	
Multi-function Timer	A/D start compare	6 ch.	1 unit	
	Input capture	4 ch.		
	Free-run timer	3 ch.		
	Output compare	6 ch.		
	Waveform generator	3 ch.		
	PPG	3 ch.		
QPRC			1 ch.	
Dual Timer			1 unit	
Real-time Clock			1 unit	
Watch Counter			1 unit	
Watchdog timer			1 ch. (SW) + 1 ch. (HW)	
External Interrupt			8 pins (Max) + NMI × 1	
I/O port			23 pins (Max)	37 pins (Max)
12-bit A/D converter			5 ch. (1 unit)	8 ch. (1 unit)
CSV (Clock Supervisor)			Yes	
LVD (Low-voltage Detection)			2 ch.	
Built-in CR	High-speed		4 MHz	
	Low-speed		100 kHz	
Debug Function			SW-DP	
Unique ID			Yes	

Note:

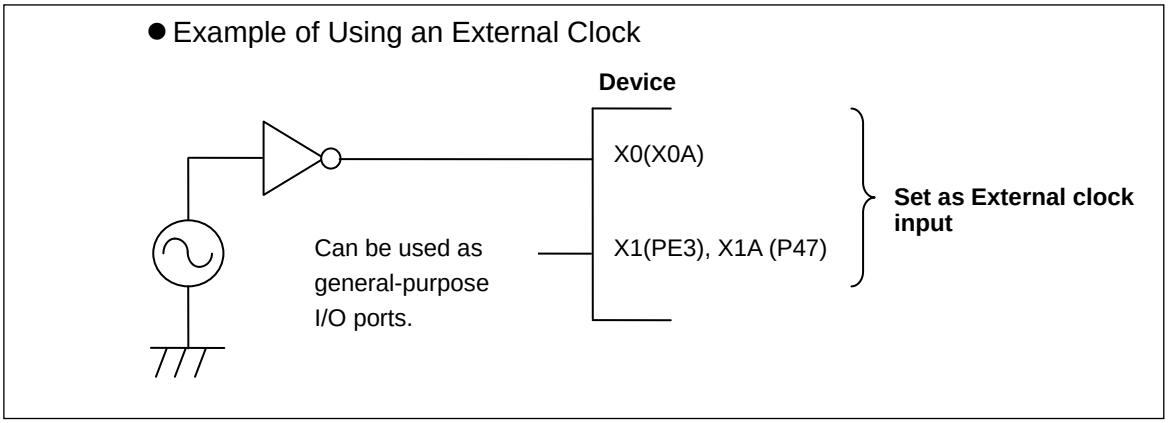
- All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the I/O port according to your function use.
  See "14. ELECTRICAL CHARACTERISTICS 14.4 AC Characteristics 14.4.3 Built-in CR Oscillation Characteristics" for accuracy of built-in CR.

Pin function	Pin name	Function description	Pin no.		
			LQFP-52	LQFP-48 QFN-48	LQFP-32 QFN-32
GPIO	P00	General-purpose I/O port 0	41	37	-
	P01		42	38	26
	P02		43	39	-
	P03		44	40	27
	P04		45	41	28
	P0F		46	42	29
	P10	General-purpose I/O port 1	27	25	-
	P11		28	26	18
	P12		29	27	19
	P13		30	28	20
	P14		31	29	-
	P15		32	30	-
	P21	General-purpose I/O port 2	39	36	25
	P22		38	35	24
	P23		37	34	23
	P39	General-purpose I/O port 3	6	5	-
	P3A		7	6	1
	P3B		8	7	2
	P3C		9	8	3
	P3D		10	9	4
	P3E		11	10	5
	P3F		12	11	6
GPIO	P46	General-purpose I/O port 4	16	15	10
	P47		17	16	11
	P49		19	18	-
	P4A		20	19	-
	P50	General-purpose I/O port 5	2	2	-
	P51		3	3	-
	P52		4	4	-
	P60	General-purpose I/O port 6	48	44	31
	P61		47	43	30
	P80	General-purpose I/O port 8	49	45	-
	P81		50	46	-
	P82		51	47	-
	PE0*	General-purpose I/O port E	22	20	13
	PE2		24	22	15
	PE3		25	23	16

Type	Circuit	Remarks
I		• CMOS level output • CMOS level hysteresis input • 5V tolerant • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50kΩ • I_{OH}= -4mA, I_{OL}= 4mA • Available to control PZR registers • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off
J		CMOS level hysteresis input
K		• CMOS level output • CMOS level hysteresis input • With standby mode control • I_{OH}= -4mA, I_{OL}= 4mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off

Using an External Clock

When using an external clock as an input of the main clock, set X0/X1 to the external clock input, and input the clock to X0. X1(PE3) can be used as a general-purpose I/O port.
Similarly, when using an external clock as an input of the sub clock, set X0A/X1A to the external clock input, and input the clock to X0A. X1A (P47) can be used as a general-purpose I/O port.

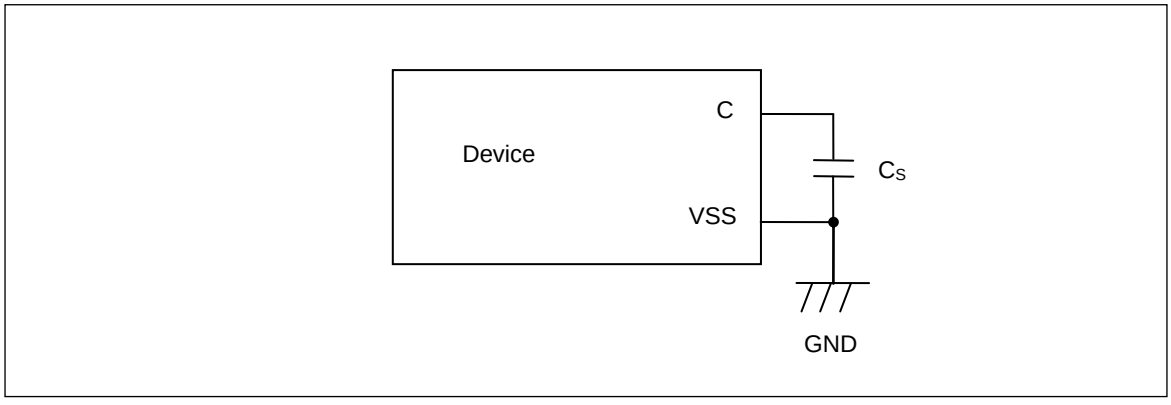


Handling when Using Multi-Function Serial Pin as I²C Pin

If it is using the multi-function serial pin as I²C pins, P-ch transistor of digital output is always disabled.
However, I²C pins need to keep the electrical characteristic like other pins and not to connect to the external I²C bus system with power OFF.

C Pin

This series contains the regulator. Be sure to connect a smoothing capacitor (C_S) for the regulator between the C pin and the GND pin. Please use a ceramic capacitor or a capacitor of equivalent frequency characteristics as a smoothing capacitor.
However, some laminated ceramic capacitors have the characteristics of capacitance variation due to thermal fluctuation (F characteristics and Y5V characteristics). Please select the capacitor that meets the specifications in the operating conditions to use by evaluating the temperature characteristics of a capacitor.
A smoothing capacitor of about 4.7 µF would be recommended for this series.



Mode Pins (MD0)

Connect the MD pin (MD0) directly to VCC or VSS pins. Design the printed circuit board such that the pull-up/down resistance stays low, as well as the distance between the mode pins and VCC pins or VSS pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

Notes on Power-on

Turn power on/off in the following order or at the same time.

Turning on : VBAT → VCC
VCC → AVCC → AVRH
Turning off : VCC → VBAT
AVRH → AVCC → VCC

Serial Communication

There is a possibility to receive wrong data due to the noise or other causes on the serial communication.
Therefore, design a printed circuit board so as to avoid noise.

Consider the case of receiving wrong data due to noise, perform error detection such as by applying a checksum of data at the end.
If an error is detected, retransmit the data.

Differences in Features among the Products with Different Memory Sizes and between Flash Products and MASK Products

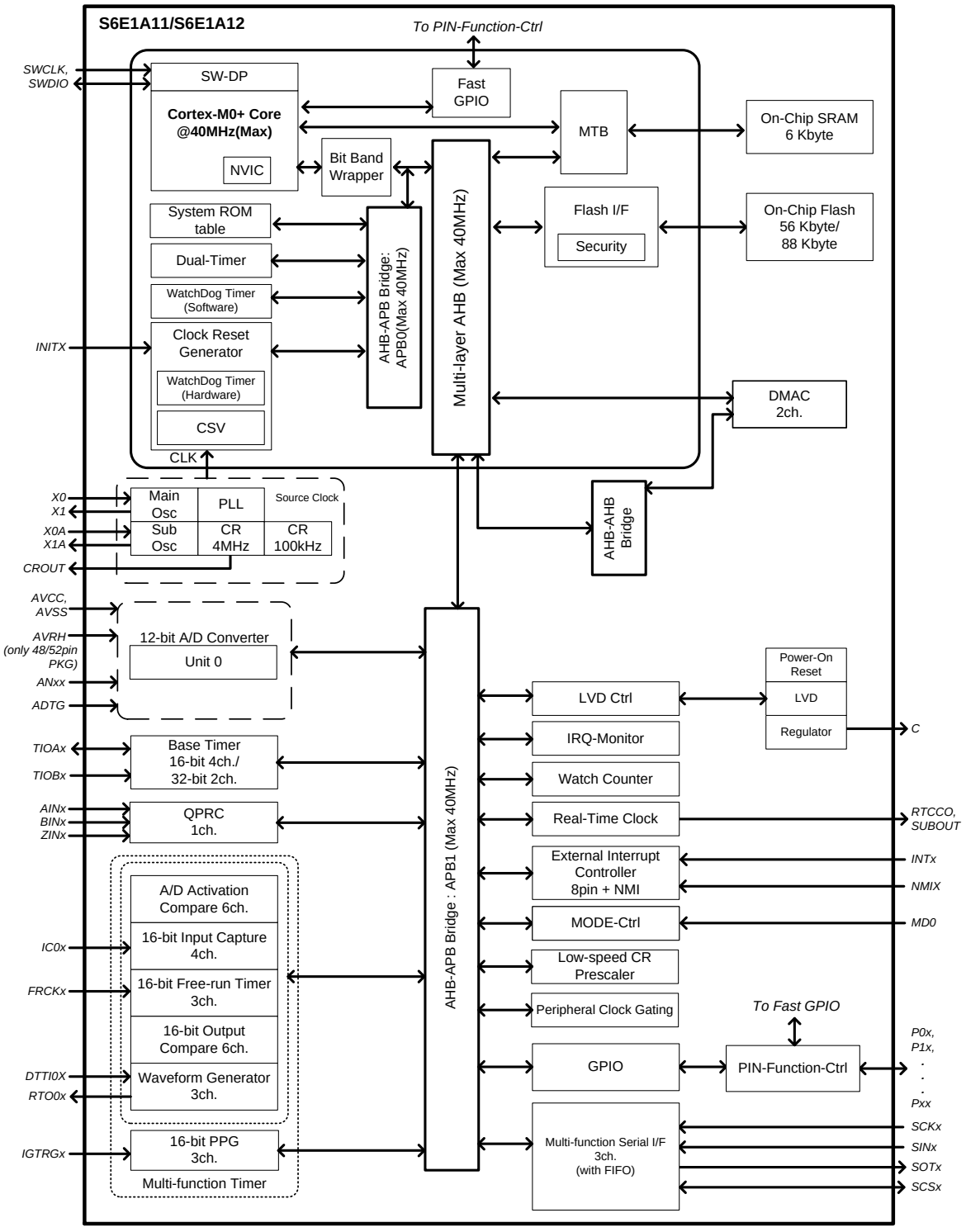
The electric characteristics including power consumption, ESD, latch-up, noise characteristics, and oscillation characteristics among the products with different memory sizes and between Flash products and MASK products are different because chip layout and memory structures are different.

If you are switching to use a different product of the same series, please make sure to evaluate the electric characteristics.

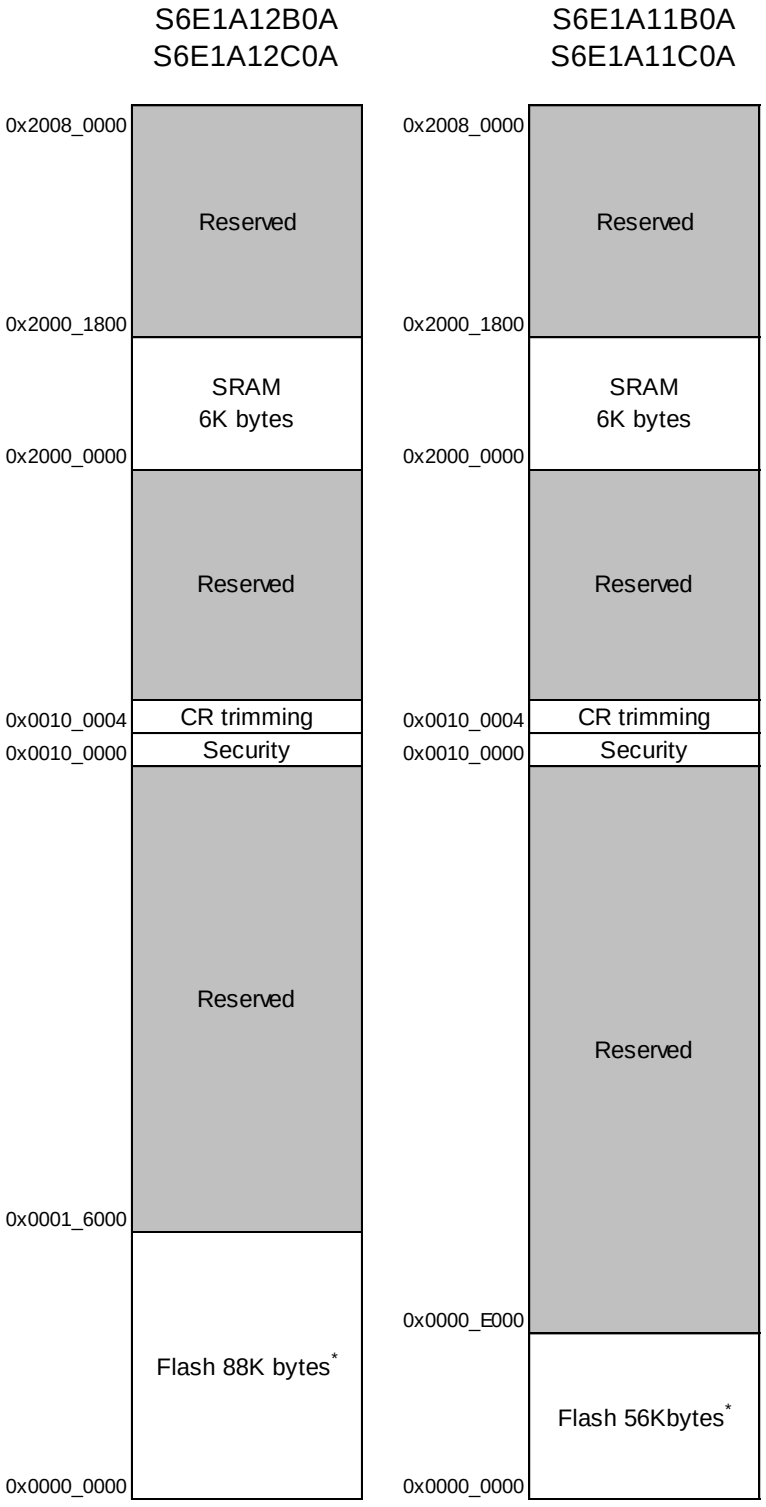
Pull-Up Function of 5V Tolerant I/O

Please do not input the signal more than VCC voltage at the time of Pull-Up function use of 5V tolerant I/O.

8. Block Diagram



Memory Map(2)


S6E1A12B0A
S6E1A12C0A
S6E1A11B0A
S6E1A11C0A
0x2008_0000
Reserved
0x2000_1800
SRAM
6K bytes
0x2000_0000
Reserved
0x0010_0004
CR trimming
0x0010_0000
Security
Reserved
0x0001_6000
Flash 88K bytes*
0x0000_0000
0x2008_0000
Reserved
0x2000_1800
SRAM
6K bytes
0x2000_0000
Reserved
0x0010_0004
CR trimming
0x0010_0000
Security
Reserved
0x0000_E000
Flash 56Kbytes*
0x0000_0000

Pin status type	Function group	State upon power-on reset or low-voltage detection	State at INITX input	State upon device internal reset	State in Run mode or SLEEP mode	State in TIMER mode, RTC mode, or STOP mode	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable	
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1	
		-	-	-	-	SPL = 0	SPL = 1
	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state
	Resource other than the above selected						Hi-Z / Internal input fixed at "0"
	GPIO selected						

*1:Oscillation stops in Sub timer mode, Low-speed CR timer mode, STOP mode, RTC mode.

*2:Oscillation stops in STOP mode.

12.4.3 Built-in CR Oscillation Characteristics

Built-in high-speed CR

(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} =AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	F_{CRH}	Ta = + 25°C, 3.6V < V_{CC} ≤ 5.5V	3.92	4	4.08	MHz	During trimming*1
		Ta =0°C to + 85°C, 3.6V < V_{CC} ≤ 5.5V	3.9	4	4.1		
		Ta = - 40°C to + 105°C, 3.6V < V_{CC} ≤ 5.5V	3.88	4	4.12		
		Ta = + 25°C, 2.7V ≤ V_{CC} ≤ 3.6V	3.94	4	4.06		
		Ta = - 20°C to + 85°C, 2.7V ≤ V_{CC} ≤ 3.6V	3.92	4	4.08		
		Ta = - 20°C to + 105°C, 2.7V ≤ V_{CC} ≤ 3.6V	3.9	4	4.1		
		Ta = - 40°C to + 105°C, 2.7V ≤ V_{CC} ≤ 3.6V	3.88	4	4.12		
		Ta = - 40°C to + 105°C	2.8	4	5.2		Not during trimming
Frequency stabilization time	t_{CRWT}	-	-	-	30	µs	*2

*1: In the case of using the values in CR trimming area of Flash memory at shipment for frequency trimming/temperature trimming.

*2: This is time from the trim value setting to stable of the frequency of the High-speed CR clock. After setting the trim value, the period when the frequency stability time passes can use the High-speed CR clock as a source clock.

Built-in low-speed CR

(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} =AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	F_{CRL}	-	50	100	150	kHz	

12.4.4 Operating Conditions of Main PLL (In the case of using the main clock as the input clock of the PLL)

(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	F_{PLLI}	4	-	16	MHz	
PLL multiple rate	-	5	-	37	multiple	
PLL macro oscillation clock frequency	F_{PLLO}	75	-	150	MHz	
Main PLL clock frequency*2	F_{CLKPLL}	-	-	40	MHz	

*1: The wait time is the time it takes for PLL oscillation to stabilize.

*2: For details of the main PLL clock (CLKPLL), refer to "CHAPTER: Clock" in "FM0+ Family PERIPHERAL MANUAL".

12.4.5 Operating Conditions of Main PLL (In the case of using the built-in high-speed CR clock as the input clock of the main PLL)

(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	F_{PLLI}	3.88	4	4.12	MHz	
PLL multiple rate	-	19	-	35	multiple	
PLL macro oscillation clock frequency	F_{PLLO}	72	-	150	MHz	
Main PLL clock frequency*2	F_{CLKPLL}	-	-	41.2	MHz	

*1: The wait time is the time it takes for PLL oscillation to stabilize.

*2: For details of the main PLL clock (CLKPLL), refer to "CHAPTER: Clock" in "FM0+ Family PERIPHERAL MANUAL".

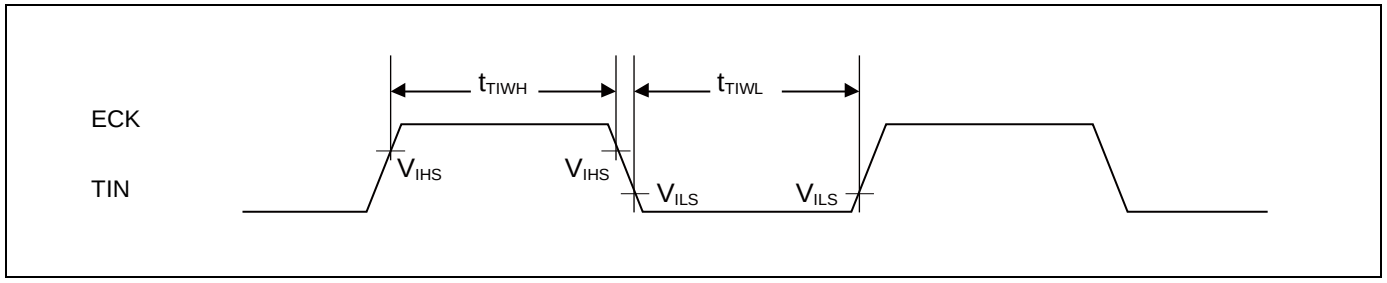
Note:
For the main PLL source clock, input the high-speed CR clock (CLKHC) whose frequency has been trimmed.

12.4.8 Base Timer Input Timing

Timer input timing

(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

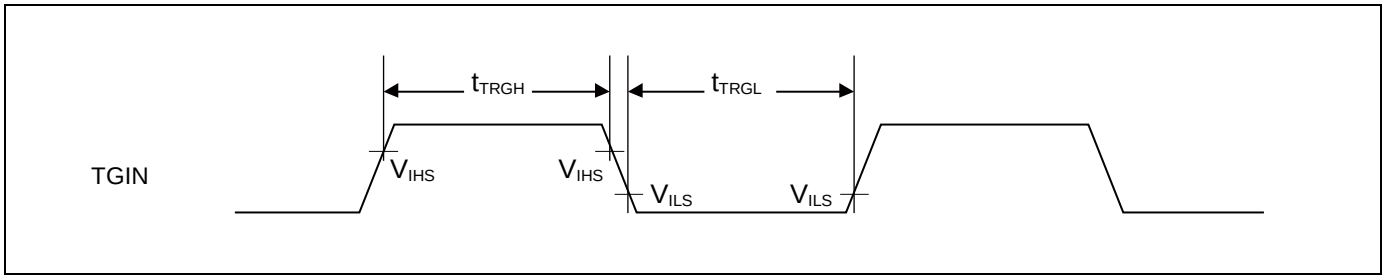
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}, t_{TIWL}	TIOAn/TIOBn (when using as ECK, TIN)	-	2 t_{CYCP}	-	ns	



Trigger input timing

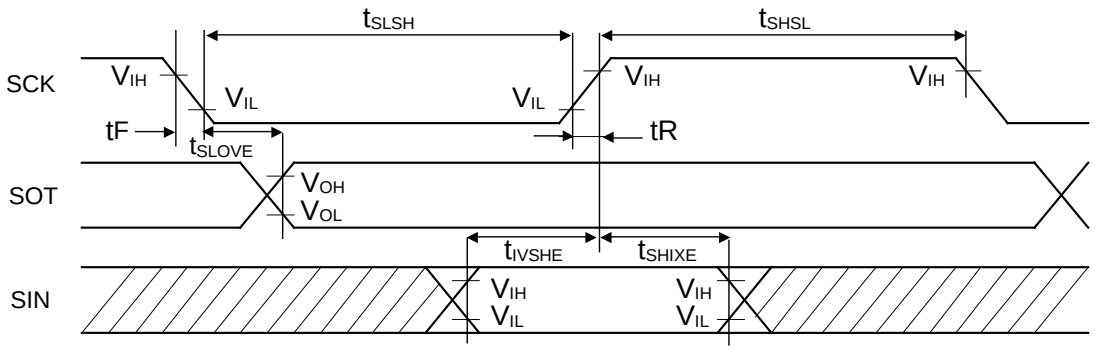
(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	TIOAn/TIOBn (when using as TGIN)	-	2 t_{CYCP}	-	ns	



Note:

- t_{CYCP} indicates the APB bus clock cycle time.
  For the number of the APB bus to which the Base Timer has been connected, see "8. Block Diagram".



Synchronous serial (SPI = 0, SCINV = 1)

(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	V_{CC} < 4.5V		V_{CC} ≥ 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	4 t_{CYCP}	-	4 t_{CYCP}	-	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKx, SINx		50	-	30	-	ns
SCK ↓ → SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	External shift clock operation	2 t_{CYCP} - 10	-	2 t_{CYCP} - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx, SOTx		-	50	-	30	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK ↓ → SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- The above AC characteristics are for CLK synchronous mode.
- t_{CYCP} represents the APB bus clock cycle time.
  For the number of the APB bus to which Multi-function Serial has been connected, see "8. Block Diagram ".
- The characteristics are only applicable when the relocate port numbers are the same.
  For instance, they are not applicable for the combination of SCLKx_0 and SOTx_1.
- External load capacitance C_L = 30 pF

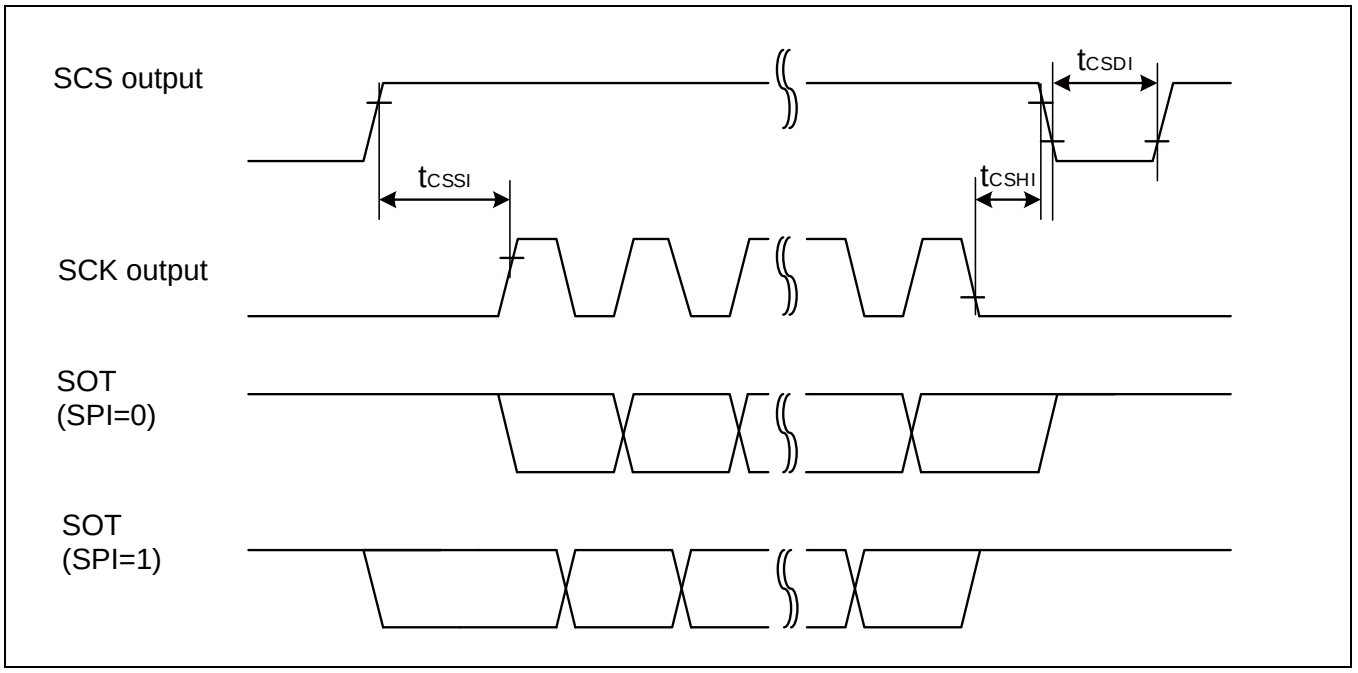
Synchronous serial (SPI = 1, SCINV = 1)

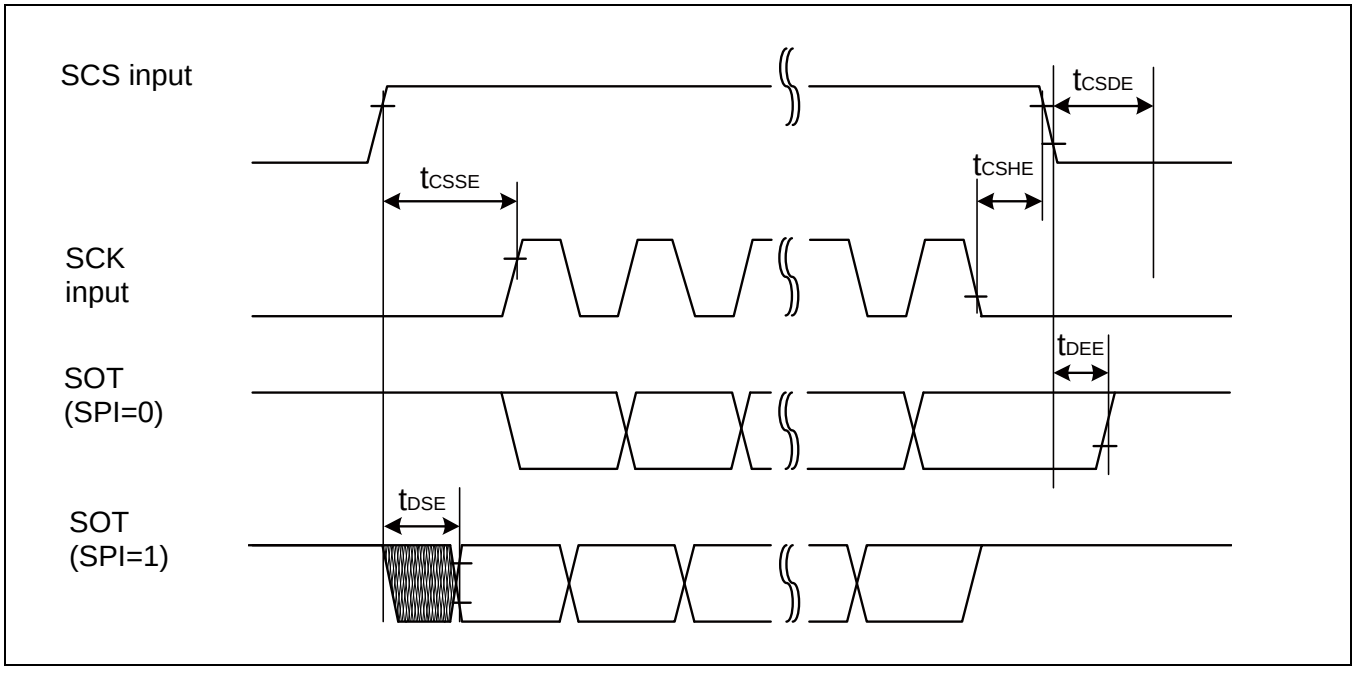
(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	4 t_{CYCP}	-	4 t_{CYCP}	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	30	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCKx, SOTx		2 t_{CYCP} - 30	-	2 t_{CYCP} - 30	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	External shift clock operation	2 t_{CYCP} - 10	-	2 t_{CYCP} - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	-	30	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- The above AC characteristics are for CLK synchronous mode.
- t_{CYCP} represents the APB bus clock cycle time.
  For the number of the APB bus to which Multi-function Serial has been connected, see "8. Block Diagram ".
- The characteristics are only applicable when the relocate port numbers are the same.
  For instance, they are not applicable for the combination of SCLKx_0 and SOTx_1.
- External load capacitance C_L = 30 pF


SCS output
SCK output
SOT
(SPI=0)
SOT
(SPI=1)
tCSDI
tCSSI
tCSHI


SCS input
SCK
input
SOT
(SPI=0)
SOT
(SPI=1)
tCSDE
tCSSE
tCSHE
tDEE
tDSE

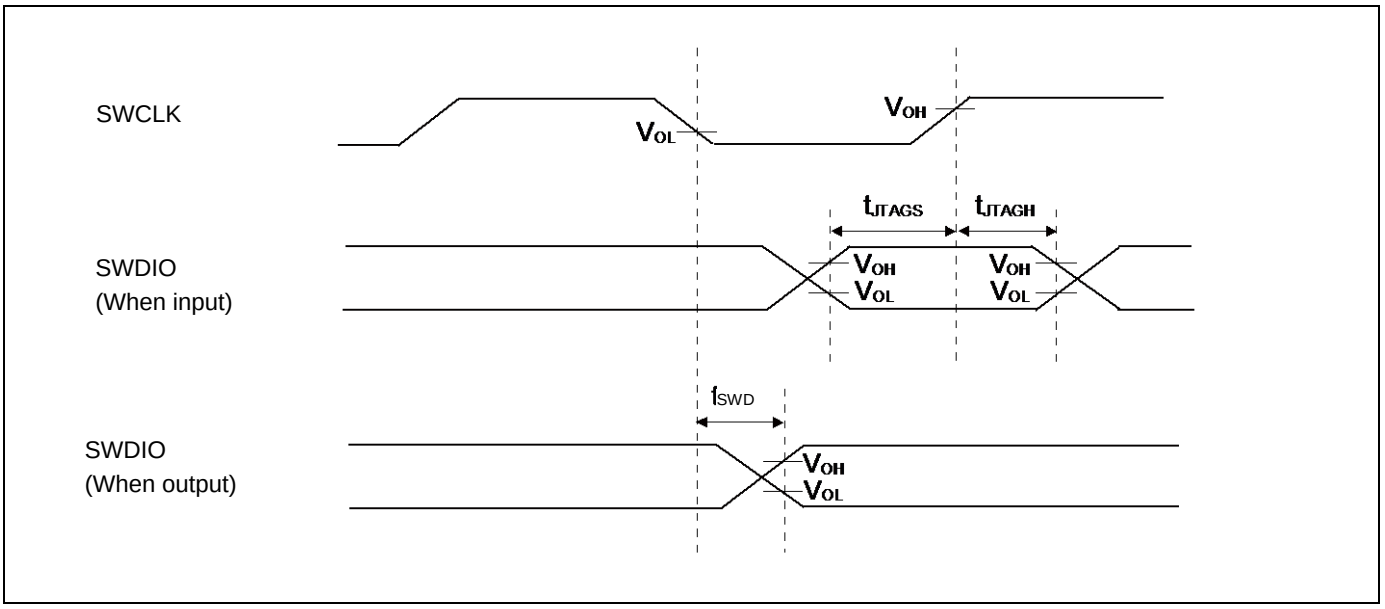
12.4.13 SW-DP Timing

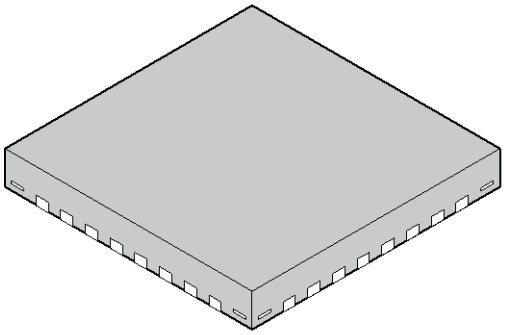
(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SWDIO setup time	t_{SWS}	SWCLK, SWDIO	-	15	-	ns	
SWDIO hold time	t_{SWH}	SWCLK, SWDIO	-	15	-	ns	
SWDIO delay time	t_{SWD}	SWCLK, SWDIO	-	-	45	ns	

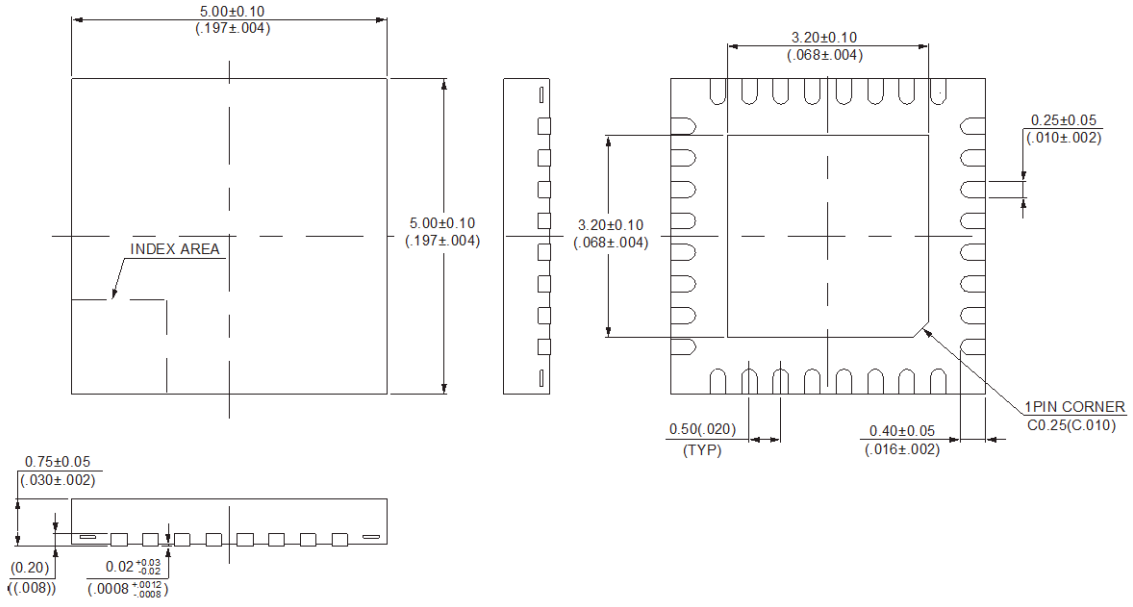
Note:

- External load capacitance C_L = 30 pF

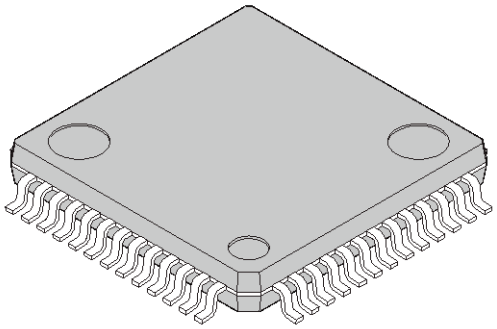


32-pin plastic QFN		
 (LCC-32P-M73)	Lead pitch	0.50 mm
	Package width × package length	5.00 mm × 5.00 mm
	Sealing method	Plastic mold
	Mounting height	0.80 mm MAX
	Weight	0.06 g

32-pin plastic QFN
(LCC-32P-M73)

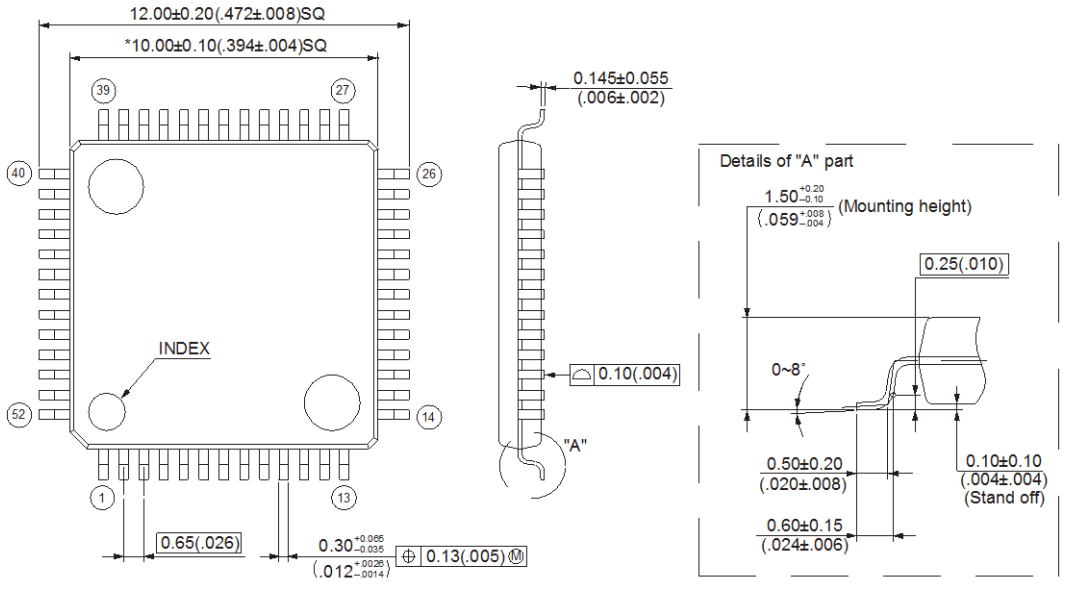


Dimensions in mm (inches).
Note: The values in parentheses are reference values.

52-pin plastic LQFP		
	Lead pitch	0.65 mm
	Package width × package length	10.00 × 10.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.32 g
(FPT-52P-M02)	Code (Reference)	P-LFQFP52-10 × 10-0.65

52-pin plastic LQFP
(FPT-52P-M02)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values

Page	Section	Change Results
86,88	14. Electrical Characteristics 14.8 Return Time from Low-Power Consumption Mode	Revised the value of "TBD"
90	15. Ordering Information	Revised from "LCC-52P-M02" to "FPT-52P-M02"

NOTE: Please see “Document History” about later revised information.