Infineon Technologies - S6E1A12C0AGV20000 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CSIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	88KB (88K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e1a12c0agv20000

Watch Counter
The Watch Counter wakes up the microcontroller from the low power consumption mode. The clock source can be selected from the main clock, the sub clock, the built-in high-speed CR clock or the built-in low-speed CR clock.

Interval timer: up to 64 s (sub clock: 32.768 kHz)

External Interrupt Controller Unit

- Up to 8 external interrupt input pins
- Non-maskable interrupt (NMI) input pin: 1

Watchdog Timer (2 channels)
The watchdog timer generates an interrupt or a reset when the counter reaches a time-out value.

This series consists of two different watchdogs, "hardware" watchdog and "software" watchdog.

The "hardware" watchdog timer is clocked by the built-in low-speed CR oscillator. Therefore, the "hardware" watchdog is active in any low-power consumption modes except RTC mode and STOP mode.

Clock and Reset

- Clocks

A clock can be selected from five clock sources (two external oscillators, two built-in CR oscillator, and main PLL).

  - Main clock : 4 MHz to 40MHz
  - Sub clock : 32.768 kHz
  - Built-in high-speed CR clock : 4 MHz
  - Built-in low-speed CR clock : 100 kHz
  - Main PLL clock

- Resets
  - Reset request from the INITX pin
  - Power on reset
  - Software reset
  - Watchdog timer reset
  - Low-voltage detection reset
  - Clock supervisor reset

Clock Supervisor (CSV)
The Clock Supervisor monitors the failure of external clocks with a clock generated by a built-in CR oscillator.

- If an external clock failure (clock stop) is detected, a reset is asserted.
- If an external frequency anomaly is detected, an interrupt or a reset is asserted.

Low-voltage Detector (LVD)
This series monitors the voltage on the VCC pin with a 2-stage mechanism. When the voltage falls below a designated voltage, the Low-voltage Detector generates an interrupt or a reset.

- LVD1: error reporting via an interrupt
- LVD2: auto-reset operation

Low Power Consumption Mode
This series has four low power consumption modes.

- SLEEP
- TIMER
- RTC
- STOP

Peripheral Clock Gating
The system can reduce the current consumption of the total system with gating the operation clocks of peripheral functions not used.

Debug

- Serial Wire Debug Port (SW-DP)
- Micro Trace Buffer (MTB)

Unique ID
A 41-bit unique value of the device has been set.

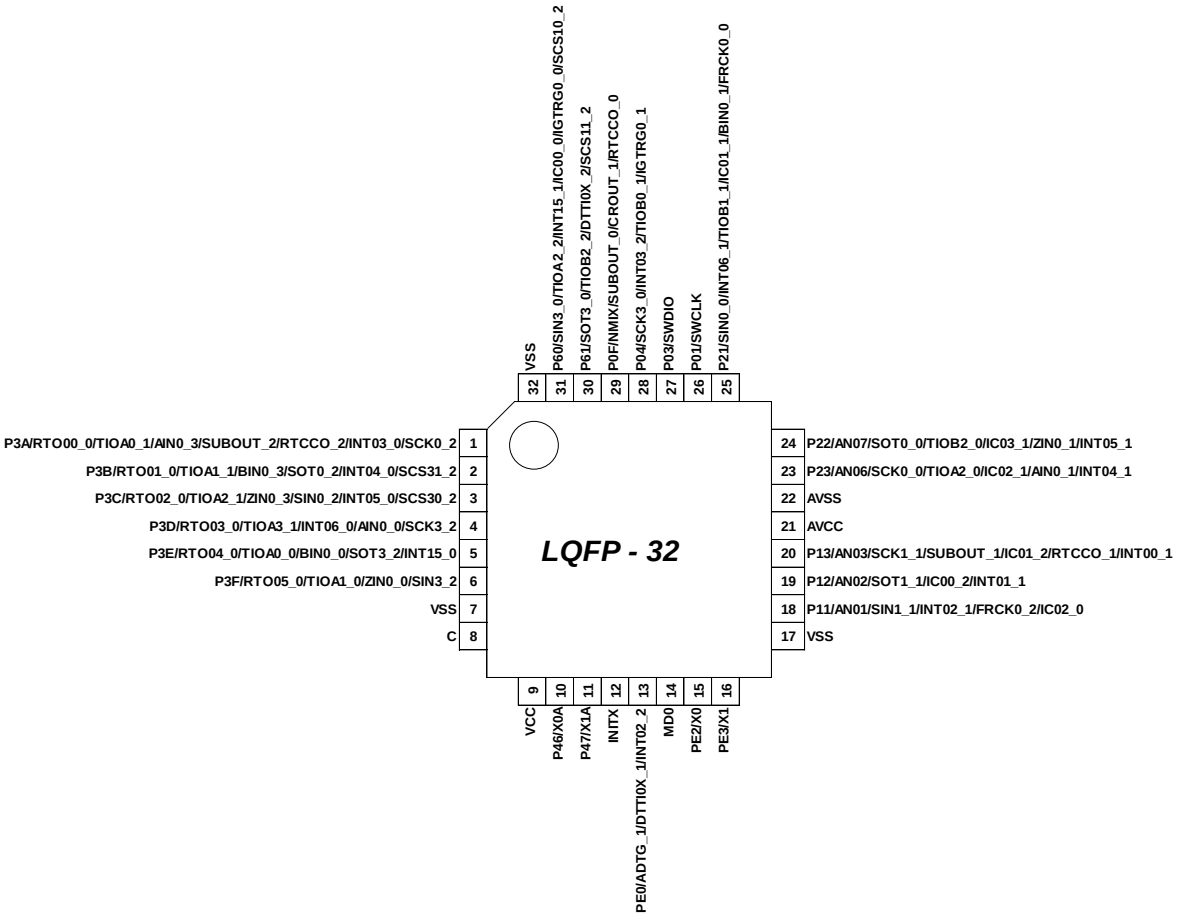
Power Supply
Wide voltage range: VCC = 2.7 V to 5.5 V

Contents

3. Pin Assignment

FPT-32P-M30

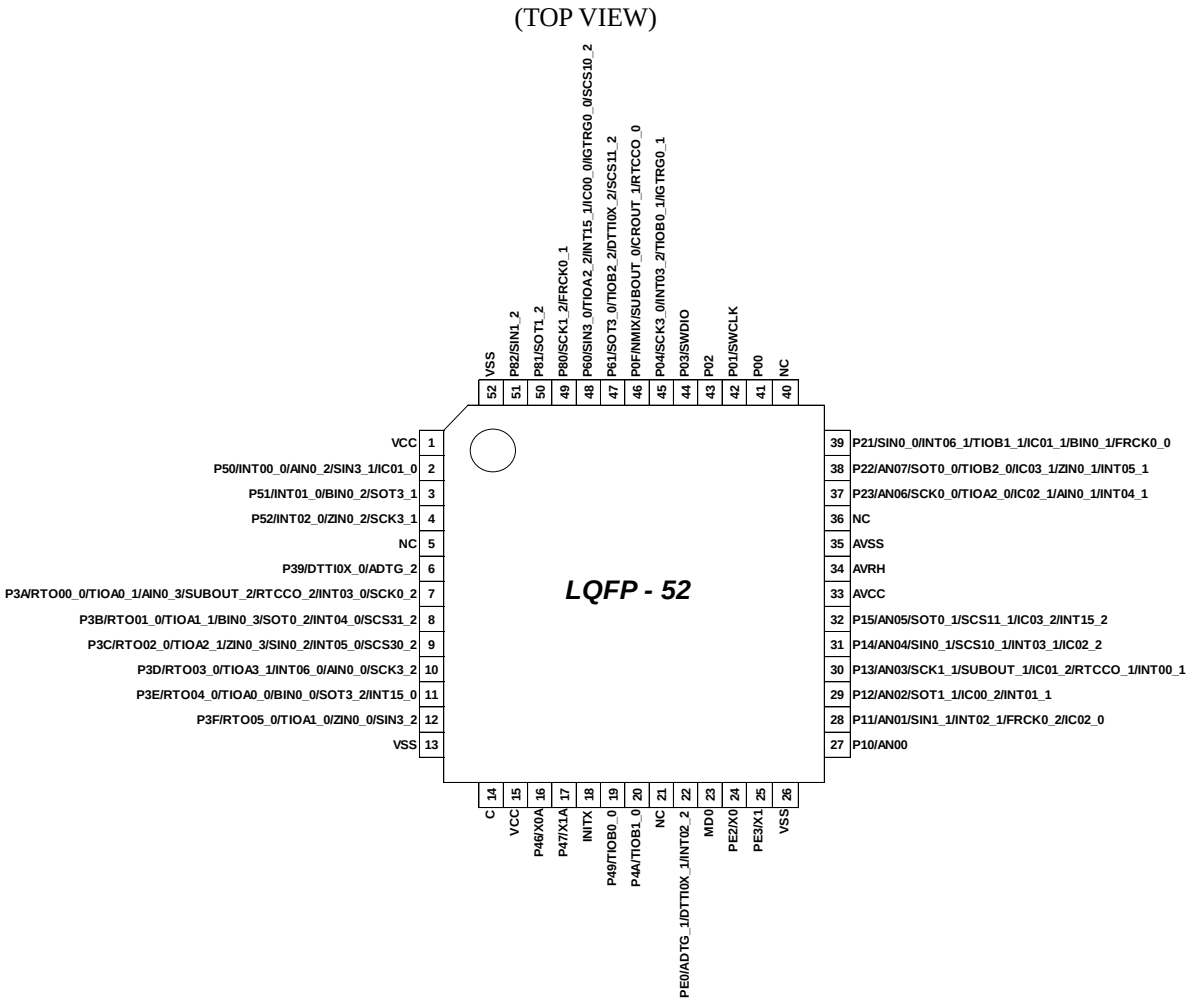
(TOP VIEW)



Note:

- The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.
  Use the extended port function register (EPFR) to select the pin.

FPT-52P-M02



Note:

- The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.

Pin no.			Pin name	I/O circuit type	Pin state type
LQFP-52	LQFP-48 QFN-48	LQFP-32 QFN-32			
9	8	3	P3C RTO02_0 TIOA2_1 ZIN0_3 SIN0_2 INT05_0 SCS30_2	F	J
10	9	4	P3D RTO03_0 TIOA3_1 INT06_0 AIN0_0 SCK3_2	F	J
11	10	5	P3E RTO04_0 TIOA0_0 BIN0_0 SOT3_2 INT15_0	F	J
12	11	6	P3F RTO05_0 TIOA1_0 ZIN0_0 SIN3_2	F	I
13	12	7	VSS	-	
14	13	8	C	-	
15	14	9	VCC	-	
16	15	10	P46 X0A	D	E
17	16	11	P47 X1A	D	F
18	17	12	INITX	B	C
19	18	-	P49 TIOB0_0	E	I
20	19	-	P4A TIOB1_0	E	I

6. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

6.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

1. Preventing Over-Voltage and Over-Current Conditions

   Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

2. Protection of Output Pins

   Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.
   Therefore, avoid this type of connection.

3. Handling of Unused Input Pins

   Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

Code: DS00-00004-2Ea

6.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity

   Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

2. Discharge of Static Electricity

   When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

3. Corrosive Gases, Dust, or Oil

   Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

4. Radiation, Including Cosmic Radiation

   Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

5. Smoke, Flame

   CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

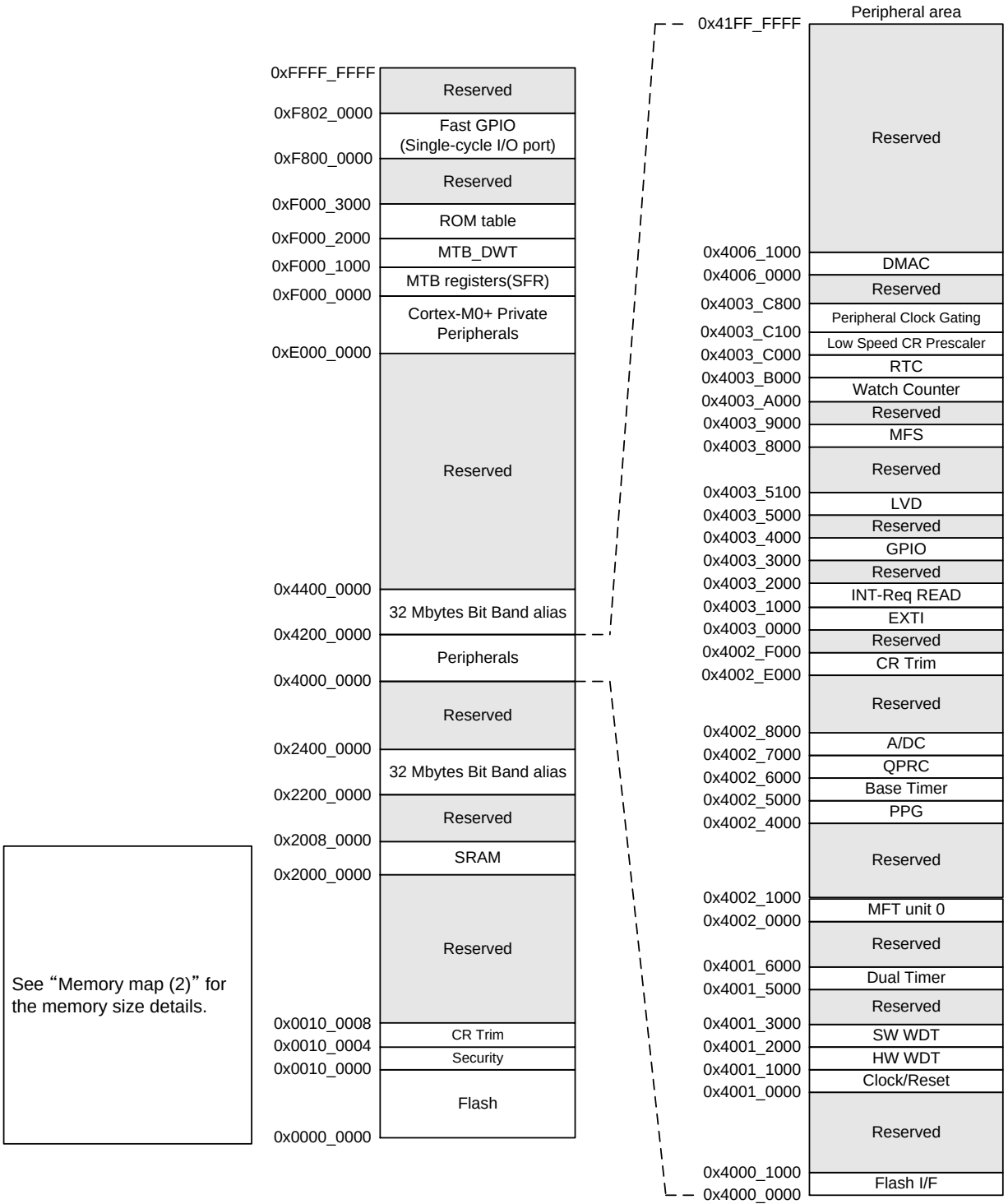
Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

9. Memory Size

See Memory size in 1. Product Lineup to confirm the memory size.

10. Memory Map

Memory Map (1)



Peripheral Address Map

Start address	End address	Bus	Peripheral
0x4000_0000	0x4000_0FFF	AHB	Flash memory I/F register
0x4000_1000	0x4000_FFFF		Reserved
0x4001_0000	0x4001_0FFF	APB0	Clock/Reset Control
0x4001_1000	0x4001_1FFF		Hardware Watchdog Timer
0x4001_2000	0x4001_2FFF		Software Watchdog Timer
0x4001_3000	0x4001_4FFF		Reserved
0x4001_5000	0x4001_5FFF		Dual-Timer
0x4001_6000	0x4001_FFFF		Reserved
0x4002_0000	0x4002_0FFF	APB1	Multi-function Timer unit0
0x4002_1000	0x4002_3FFF		Reserved
0x4002_4000	0x4002_4FFF		PPG
0x4002_5000	0x4002_5FFF		Base Timer
0x4002_6000	0x4002_6FFF		Quadrature Position/Revolution Counter
0x4002_7000	0x4002_7FFF		A/D Converter
0x4002_8000	0x4002_DFFF		Reserved
0x4002_E000	0x4002_EFFF		Built-in CR trimming
0x4002_F000	0x4002_FFFF		Reserved
0x4003_0000	0x4003_0FFF		External Interrupt Controller
0x4003_1000	0x4003_1FFF		Interrupt Request Batch-Read Function
0x4003_2000	0x4003_2FFF		Reserved
0x4003_3000	0x4003_3FFF		GPIO
0x4003_4000	0x4003_4FFF		Reserved
0x4003_5000	0x4003_57FF		Low-Voltage Detection
0x4003_5800	0x4003_7FFF		Reserved
0x4003_8000	0x4003_8FFF		Multi-function Serial Interface
0x4003_9000	0x4003_9FFF		Reserved
0x4003_A000	0x4003_AFFF		Watch Counter
0x4003_B000	0x4003_BFFF		Real-time clock
0x4003_C000	0x4003_C0FF		Low-speed CR Prescaler
0x4003_C100	0x4003_C7FF		Peripheral Clock Gating
0x4003_C800	0x4003_FFFF		Reserved
0x4004_0000	0x4005_FFFF	AHB	Reserved
0x4006_0000	0x4006_0FFF		DMAC register
0x4006_1000	0x41FF_FFFF		Reserved

Pin status type	Function group	State upon power-on reset or low-voltage detection	State at INITX input	State upon device internal reset	State in Run mode or SLEEP mode	State in TIMER mode, RTC mode, or STOP mode	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable	
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1	
		-	-	-	-	SPL = 0	SPL = 1
	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state
	Resource other than the above selected						Hi-Z / Internal input fixed at "0"
	GPIO selected						

*1:Oscillation stops in Sub timer mode, Low-speed CR timer mode, STOP mode, RTC mode.

*2:Oscillation stops in STOP mode.

12.2 Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0.0V)

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Power supply voltage	V_{CC}	-	2.7*2	5.5	V	
Analog power supply voltage	AV_{CC}	-	2.7	5.5	V	AV_{CC} = V_{CC}
Analog reference voltage	AVRH	-	2.7	AV_{CC}	V	Only S6E1A1xC0A
Smoothing capacitor	C_S	-	1	10	µF	For regulator*1
Operating temperature	Ta	-	- 40	+ 105	°C	

“1: See "C Pin" in "6. Handling Precautions" for the connection of the smoothing capacitor.

*2: In between less than the minimum power supply voltage and low voltage reset/interrupt detection voltage or more, instruction execution and low voltage detection function by built-in High-speed CR(including Main PLL is used) or built-in Low-speed CR is possible to operate only.

Warning

1. The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.
2. Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.
3. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet.
4. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

12.3 DC Characteristics

12.3.1 Current Rating

Symbol (Pin name)	Conditions		HCLK Frequency *4	Value Typ*1	Value Max*2	Unit	Remarks
Icc (VCC)	Run mode, code executed from Flash	4MHz external clock input, PLL ON*8 NOP code executed Built-in high speed CR stopped All peripheral clock stopped by CKENx	4MHz	0.7	1.5	mA	*3
			8MHz	1.3	2.3		
			20MHz	2.8	4.0		
			40MHz	5.7	7.3		
		4MHz external clock input, PLL ON*8 Benchmark code executed Built-in high speed CR stopped PCLK1 stopped	4MHz	0.6	1.4	mA	*3
			8MHz	1.2	2.1		
			20MHz	2.6	3.7		
			40MHz	4.8	6.3		
		4MHz crystal oscillation, PLL ON*8 NOP code executed Built-in high speed CR stopped All peripheral clock stopped by CKENx	4MHz	1.0	2.9	mA	*3
			8MHz	1.7	3.6		
			20MHz	3.4	5.6		
			40MHz	5.7	8.2		
	Run mode, code executed from RAM	4MHz external clock input, PLL ON*8 NOP code executed Built-in high speed CR stopped All peripheral clock stopped by CKENx	4MHz	0.5	1.2	mA	*3
			8MHz	0.9	1.8		
			20MHz	2.0	2.9		
			40MHz	3.7	4.8		
	Run mode, code executed from Flash	4MHz external clock input, PLL ON NOP code executed Built-in high speed CR stopped PCLK1 stopped	40MHz	2.8	3.7	mA	*3,*6,*7
	Run mode, code executed from Flash	Built-in high speed CR*5 NOP code executed All peripheral clock stopped by CKENx	4MHz	0.8	1.5	mA	*3
		32kHz crystal oscillation NOP code executed All peripheral clock stopped by CKENx	32kHz	65	900	µA	*3
		Built-in low speed CR NOP code executed All peripheral clock stopped by CKENx	100kHz	73	920	µA	*3
Iccs (VCC)	SLEEP operation	4MHz external clock input, PLL ON*8 All peripheral clock stopped by CKENx	4MHz	0.4	1.2	mA	*3
			8MHz	0.7	1.6		
			20MHz	1.5	2.4		
			40MHz	2.7	3.7		
		Built-in high speed CR*5 All peripheral clock stopped by CKENx	4MHz	0.5	1.2	mA	*3
		32kHz crystal oscillation All peripheral clock stopped by CKENx	32kHz	63	880	µA	*3
		Built-in low speed CR All peripheral clock stopped by CKENx	100kHz	66	890	µA	*3

12.4 AC Characteristics

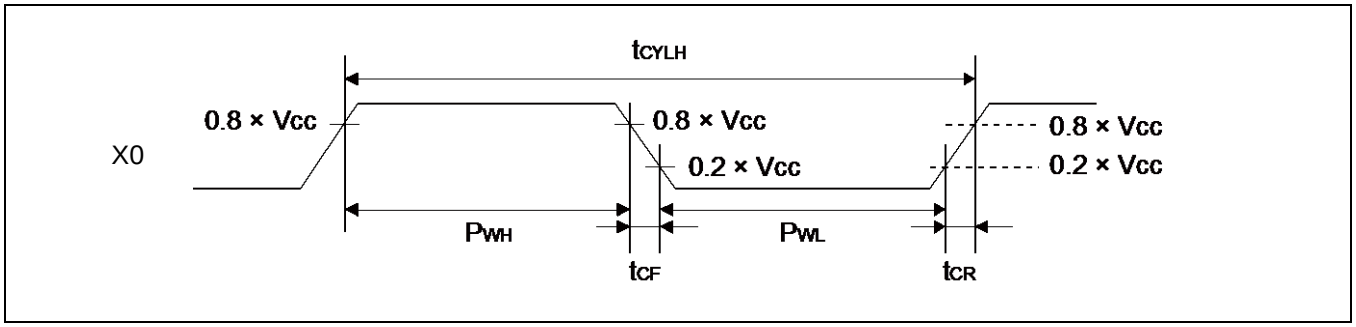
12.4.1 Main Clock Input Characteristics

(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	F_{CH}	X0, X1	V_{CC} ≥ 4.5V	4	40	MHz	When the crystal oscillator is connected
			V_{CC} < 4.5V	4	20		
			-	4	40	MHz	When the external clock is used
Input clock cycle	t_{CYLH}		-	25	250	ns	When the external clock is used
Input clock pulse width	-		P_{WH}/t_{CYLH}, P_{WL}/t_{CYLH}	45	55	%	When the external clock is used
Input clock rising time and falling time	t_{CF}, t_{CR}		-	-	5	ns	When the external clock is used
Internal operating clock*1 frequency	F_{CM}	-	-	-	41.2	MHz	Master clock
	F_{CC}	-	-	-	41.2	MHz	Base clock (HCLK/FCLK)
	F_{CP0}	-	-	-	41.2	MHz	APB0 bus clock*2
	F_{CP1}	-	-	-	41.2	MHz	APB1 bus clock*2
Internal operating clock*1 cycle time	t_{CYCC}	-	-	24.27	-	ns	Base clock (HCLK/FCLK)
	t_{CYCP0}	-	-	24.27	-	ns	APB0 bus clock*2
	t_{CYCP1}	-	-	24.27	-	ns	APB1 bus clock*2

*1: For details of each internal operating clock, refer to "CHAPTER: Clock" in "FM0+ Family PERIPHERAL MANUAL".

*2: For details of the APB bus to which a peripheral is connected, see "8. Block Diagram".



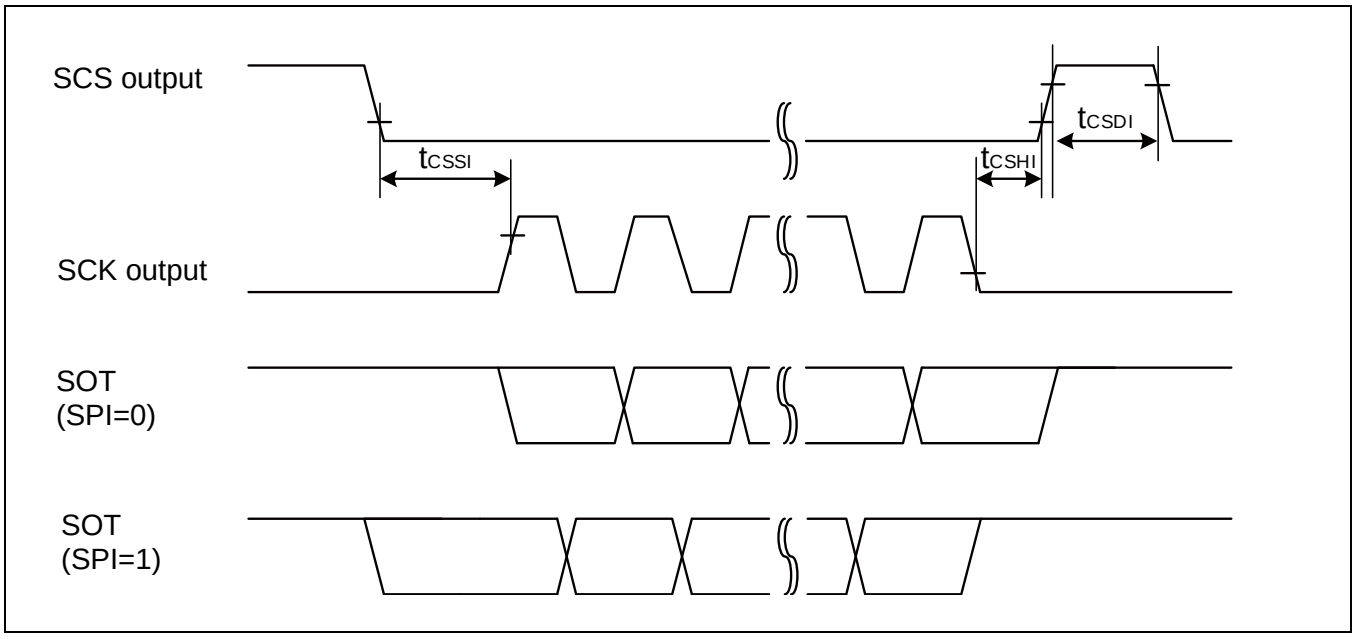
Synchronous serial (SPI = 1, SCINV = 0)

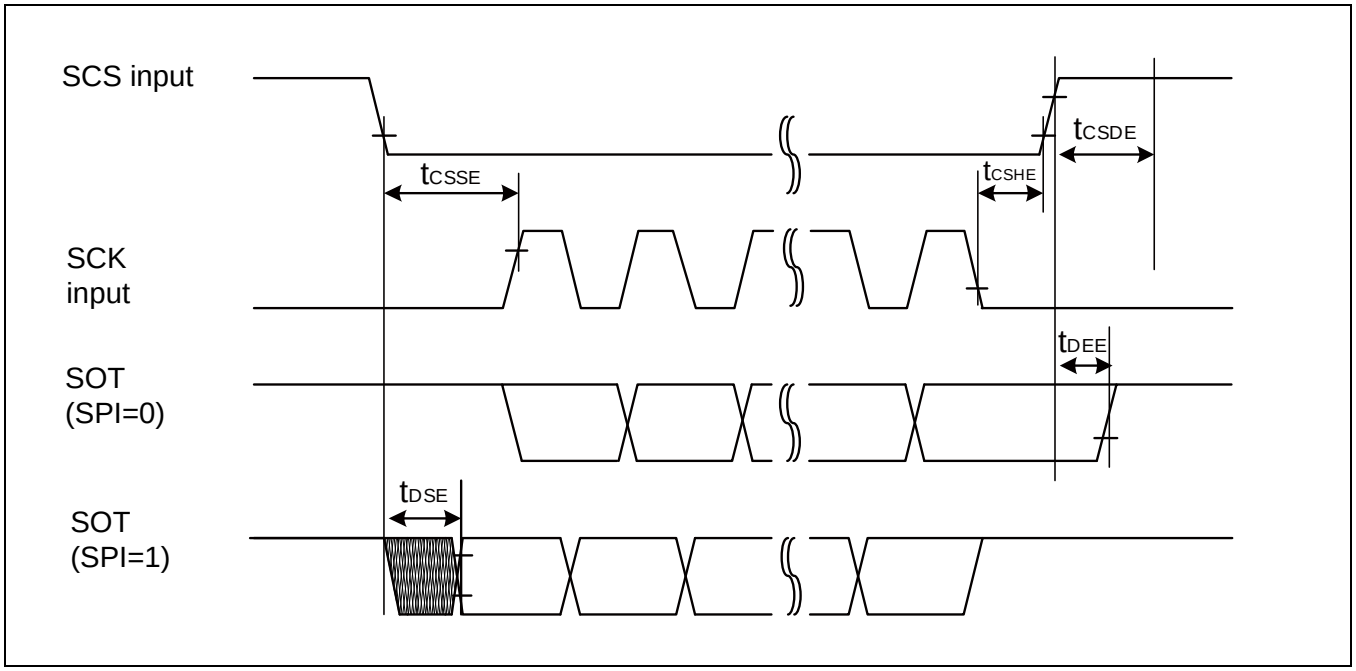
(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

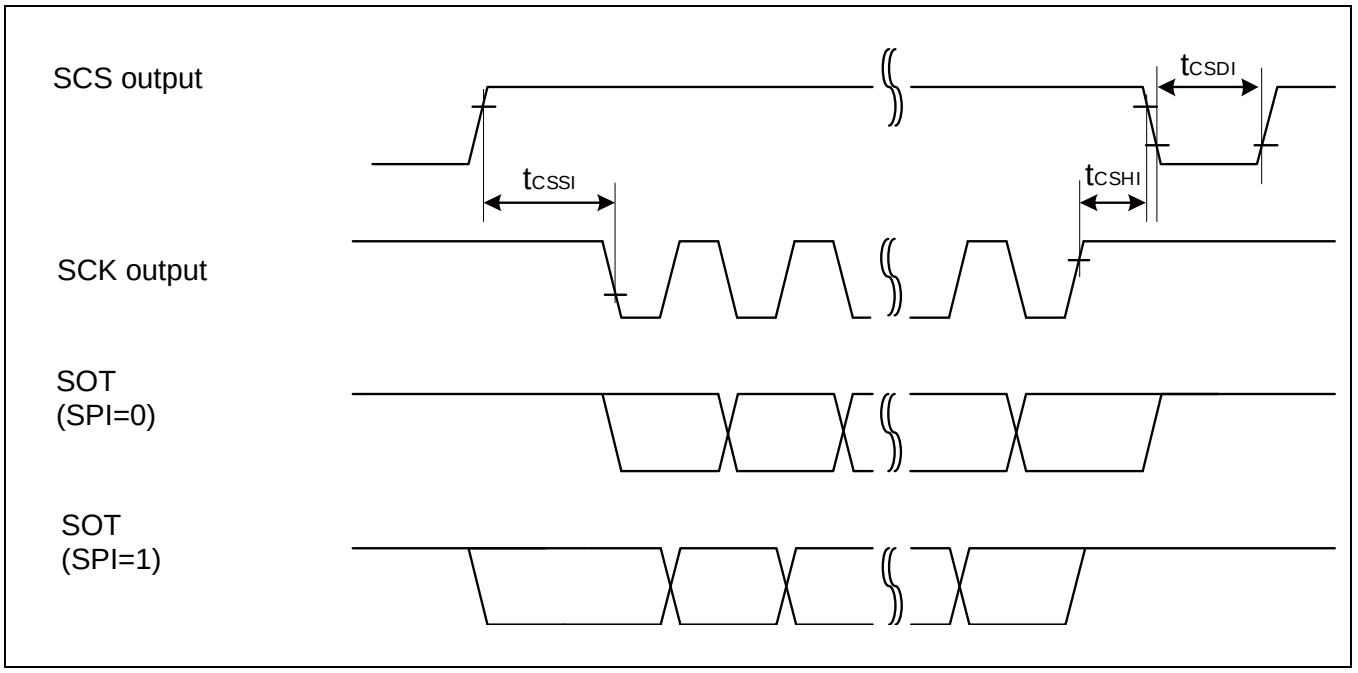
Parameter	Symbol	Pin name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	4 t_{CYCP}	-	4 t_{CYCP}	-	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKx, SINx		50	-	30	-	ns
SCK ↓→ SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCKx, SOTx		2 t_{CYCP} - 30	-	2 t_{CYCP} - 30	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	External shift clock operation	2 t_{CYCP} - 10	-	2 t_{CYCP} - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx, SOTx		-	50	-	30	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK ↓→ SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- The above AC characteristics are for CLK synchronous mode.
- t_{CYCP} represents the APB bus clock cycle time.
  For the number of the APB bus to which Multi-function Serial has been connected, see "8. Block Diagram ".
- The characteristics are only applicable when the relocate port numbers are the same.
  For instance, they are not applicable for the combination of SCLKx_0 and SOTx_1.
- External load capacitance C_L = 30 pF


SCS output
tCSSI
tCSDI
tCSHI
SCK output
SOT
(SPI=0)
SOT
(SPI=1)


SCS input
tCSSE
tCSDE
tCSHE
SCK
input
tDEE
SOT
(SPI=0)
tDSE
SOT
(SPI=1)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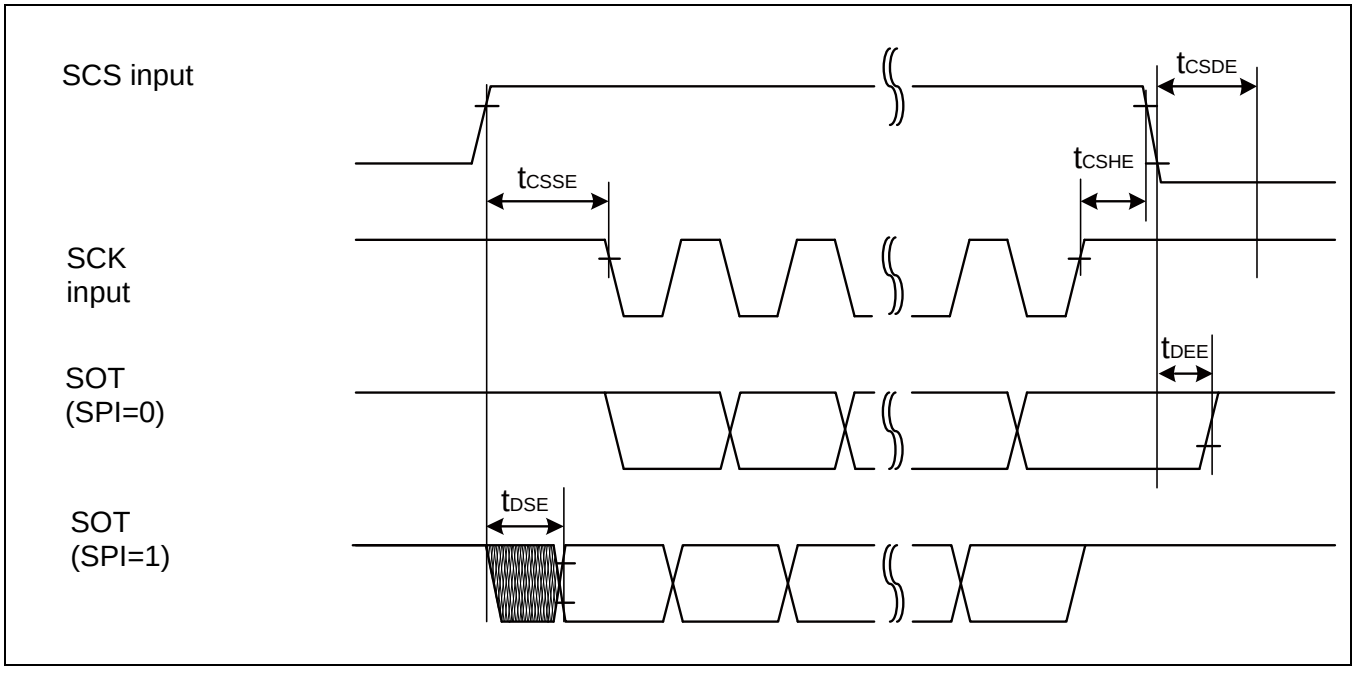
SCK output
SOT
(SPI=0)
SOT
(SPI=1)
tCSSI
tCSDI
tCSHI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SCK
input
SOT
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(SPI=1)
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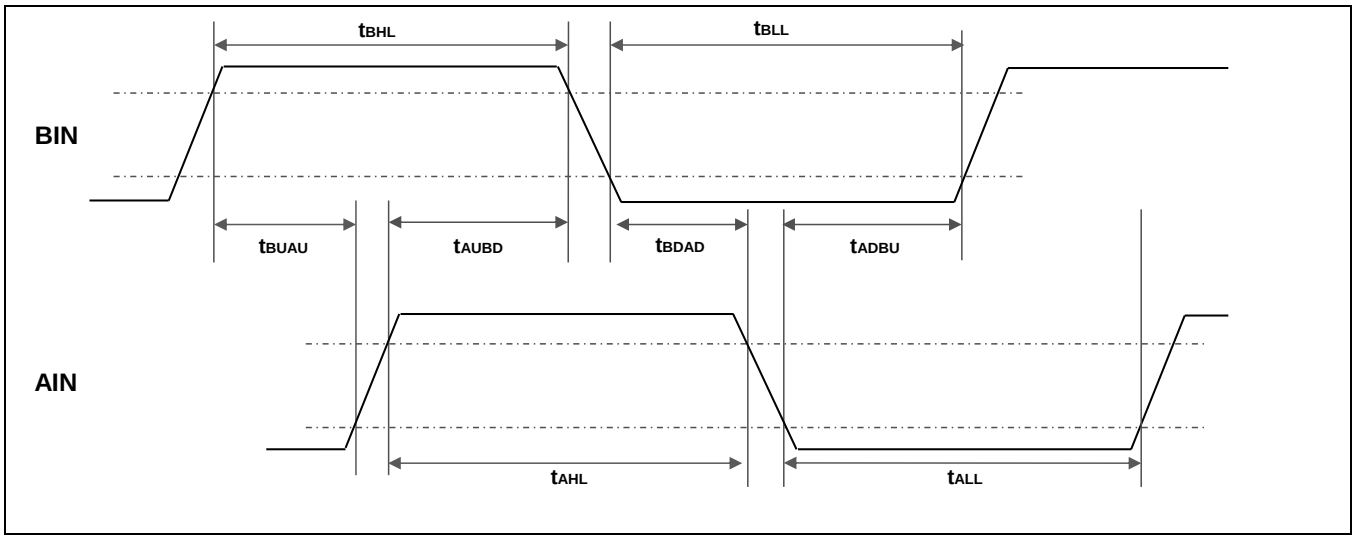
tCSDE
tCSHE
tDEE
tDSE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BIN
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tAUBD
tBDAD
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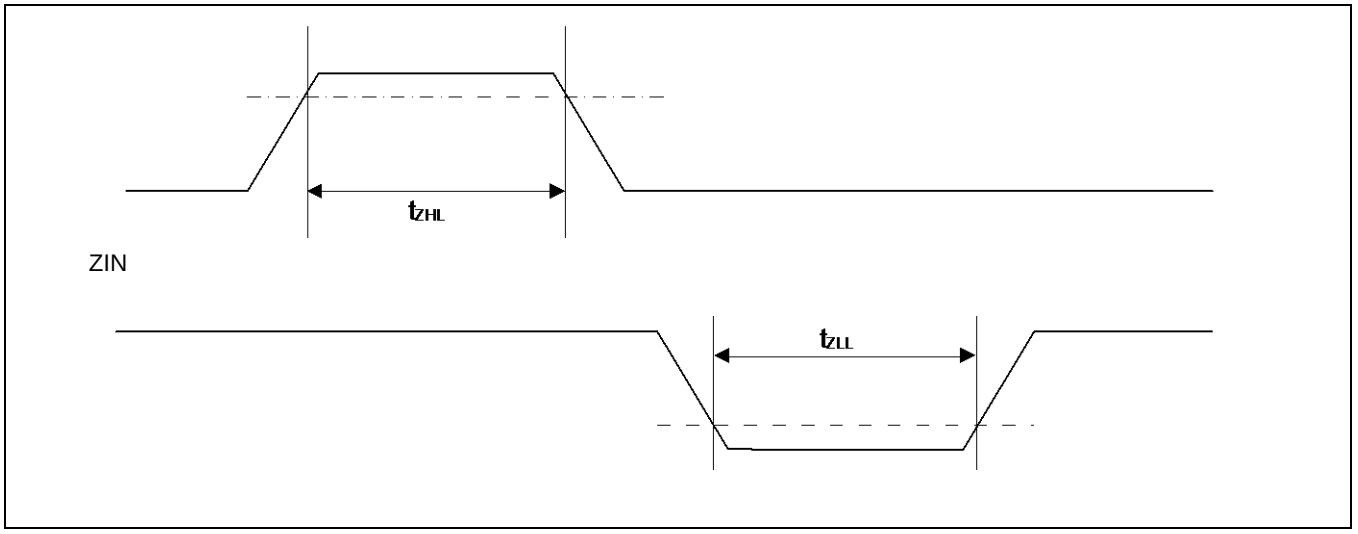
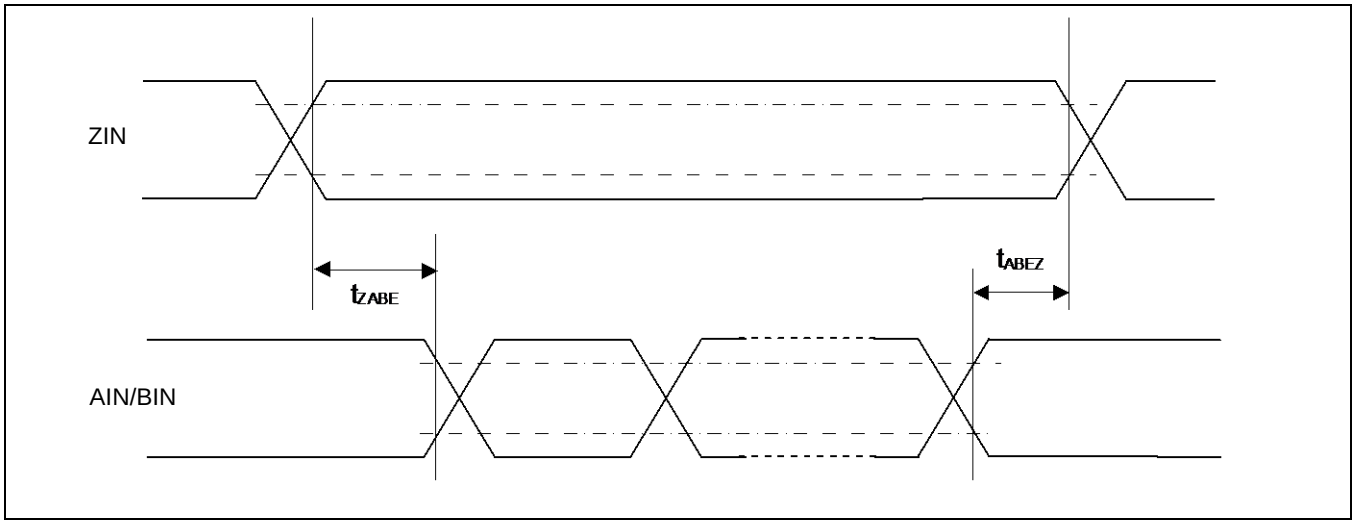
AIN
tAHL
tALL


tZHL
ZIN
tZLL


ZIN
tZABE
tABEZ
AIN/BIN

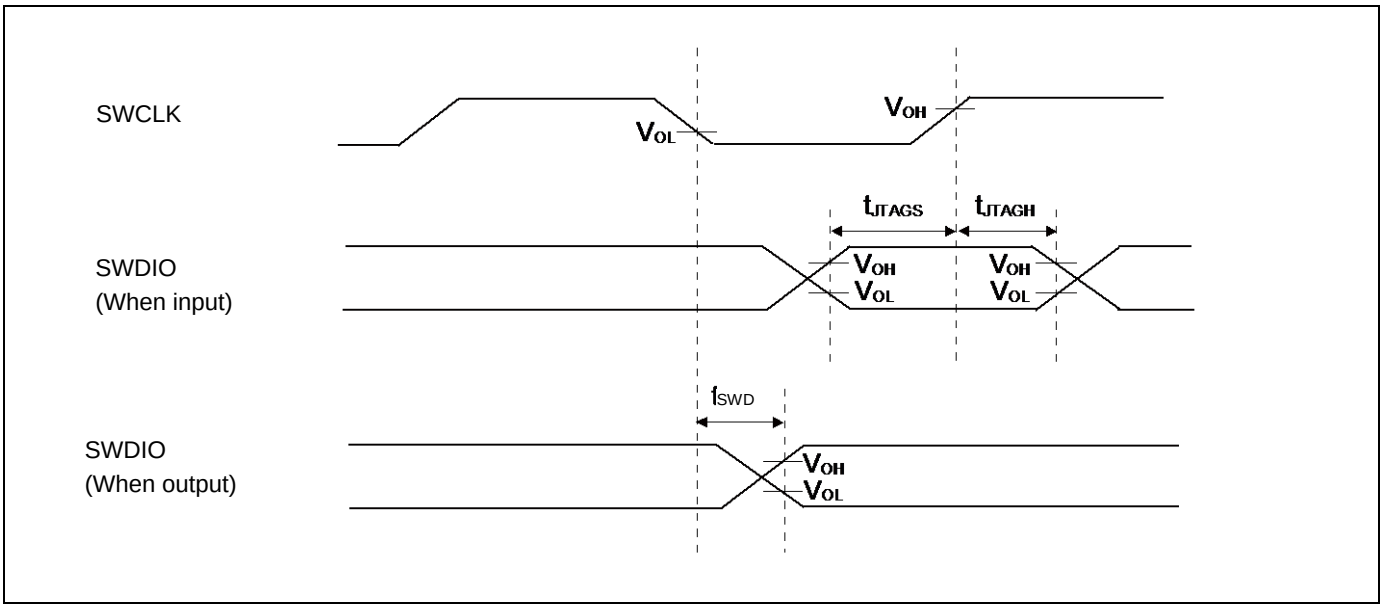
12.4.13 SW-DP Timing

(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SWDIO setup time	t_{SWS}	SWCLK, SWDIO	-	15	-	ns	
SWDIO hold time	t_{SWH}	SWCLK, SWDIO	-	15	-	ns	
SWDIO delay time	t_{SWD}	SWCLK, SWDIO	-	-	45	ns	

Note:

- External load capacitance C_L = 30 pF



12.6.2 Low-voltage Detection Interrupt

(Ta = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHI = 00011	2.58	2.80	3.02	V	When voltage drops
Released voltage	VDH		2.67	2.90	3.13	V	When voltage rises
Detected voltage	VDL	SVHI = 00100	2.76	3.00	3.24	V	When voltage drops
Released voltage	VDH		2.85	3.10	3.35	V	When voltage rises
Detected voltage	VDL	SVHI = 00101	2.94	3.20	3.46	V	When voltage drops
Released voltage	VDH		3.04	3.30	3.56	V	When voltage rises
Detected voltage	VDL	SVHI = 00110	3.31	3.60	3.89	V	When voltage drops
Released voltage	VDH		3.40	3.70	4.00	V	When voltage rises
Detected voltage	VDL	SVHI = 00111	3.40	3.70	4.00	V	When voltage drops
Released voltage	VDH		3.50	3.80	4.10	V	When voltage rises
Detected voltage	VDL	SVHI = 01000	3.68	4.00	4.32	V	When voltage drops
Released voltage	VDH		3.77	4.10	4.43	V	When voltage rises
Detected voltage	VDL	SVHI = 01001	3.77	4.10	4.43	V	When voltage drops
Released voltage	VDH		3.86	4.20	4.54	V	When voltage rises
Detected voltage	VDL	SVHI = 01010	3.86	4.20	4.54	V	When voltage drops
Released voltage	VDH		3.96	4.30	4.64	V	When voltage rises
LVD stabilization wait time	T_{LVDW}	-	-	-	8160 × t_{CYCP}*	µs	
LVD detection delay time	T_{LVDDL}	-	-	-	200	µs	

*:t_{CYCP} represents the APB1 bus clock cycle time.

12.7 Flash Memory Write/Erase Characteristics

(V_{CC} = 2.7 V to 5.5 V, Ta = - 40°C to + 105°C)

Parameter		Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	Large sector	-	0.7	2.2	s	The sector erase time includes the time of writing prior to internal erase.
	Small sector		0.3	0.9		
Halfword (16-bit) write time		-	30	528	µs	The halfword (16-bit) write time excludes the system-level overhead.
Chip erase time		-	2.6	8	s	The chip erase time includes the time of writing prior to internal erase.

Write/erase cycle and data hold time

Write/erase cycle	Data hold time (year)	Remarks
1,000	20*	
10,000	10*	

*: This value was converted from the result of a technology reliability assessment. (This value was converted from the result of a high temperature accelerated test using the Arrhenius equation with the average temperature value being + 85°C).