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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	1024
Total RAM Bits	-
Number of I/O	64
Number of Gates	6000
Voltage - Supply	4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TC)
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at6002-4jc

Devices range in size from 4,000 to 30,000 usable gates, and 1024 to 6400 registers. Pin locations are consistent throughout the AT6000 Series for easy design migration. High-I/O versions are available for the lower gate count devices.

AT6000 Series FPGAs utilize a reliable 0.6 µm single-poly, double-metal CMOS process and are 100% factory-tested.

Atmel's PC- and workstation-based Integrated Development System is used to create AT6000 Series designs. Multiple design entry methods are supported.

The Atmel architecture was developed to provide the highest levels of performance, functional density and design flexibility in an FPGA. The cells in the Atmel array are small, very efficient and contain the most important and most commonly used logic and wiring functions. The cell's small size leads to arrays with large numbers of cells, greatly multiplying the functionality in each cell. A simple, high-speed busing network provides fast, efficient communication over medium and long distances.

The Symmetrical Array

At the heart of the Atmel architecture is a symmetrical array of identical cells (Figure 1). The array is continuous and completely uninterrupted from one edge to the other, except for bus *repeaters* spaced every eight cells (Figure 2).

In addition to logic and storage, cells can also be used as wires to connect functions together over short distances and are useful for routing in tight spaces.

The Busing Network

There are two kinds of buses: local and express (see Figures 2 and 3).

Local buses are the link between the array of cells and the busing network. There are two local buses – North-South 1 and 2 (NS1 and NS2) – for every column of cells, and two local buses – East-West 1 and 2 (EW1 and EW2) – for every row of cells. In a sector (an 8 x 8 array of cells enclosed by repeaters) each local bus is connected to every cell in its column or row, thus providing every cell in the array with read/write access to two North-South and two East-West buses.

Figure 1. Symmetrical Array Surrounded by I/O

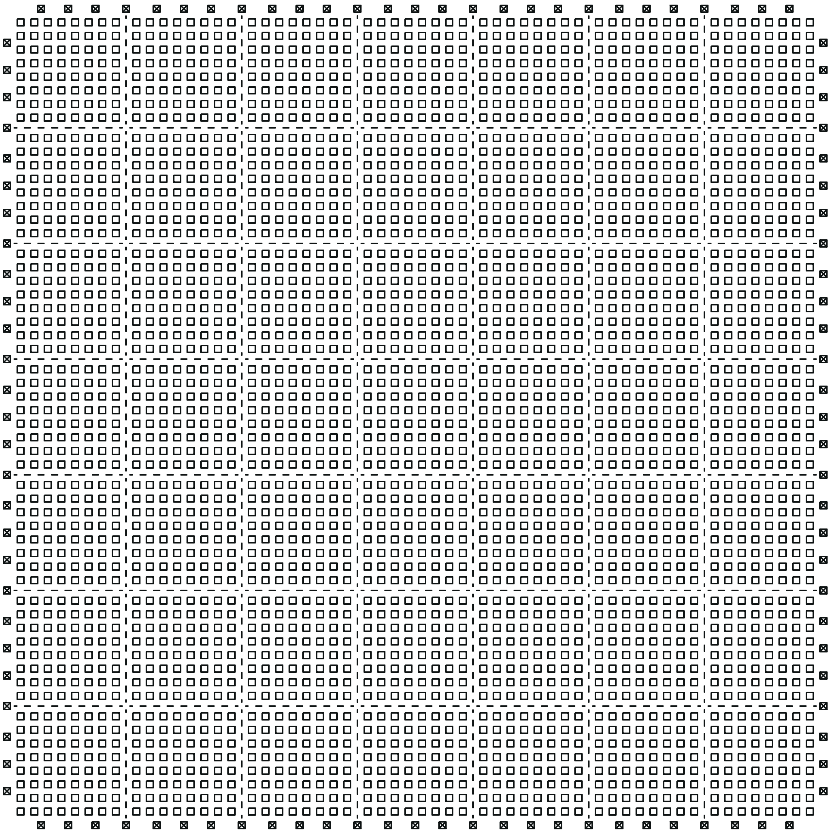


Figure 2. Busing Network (one sector)

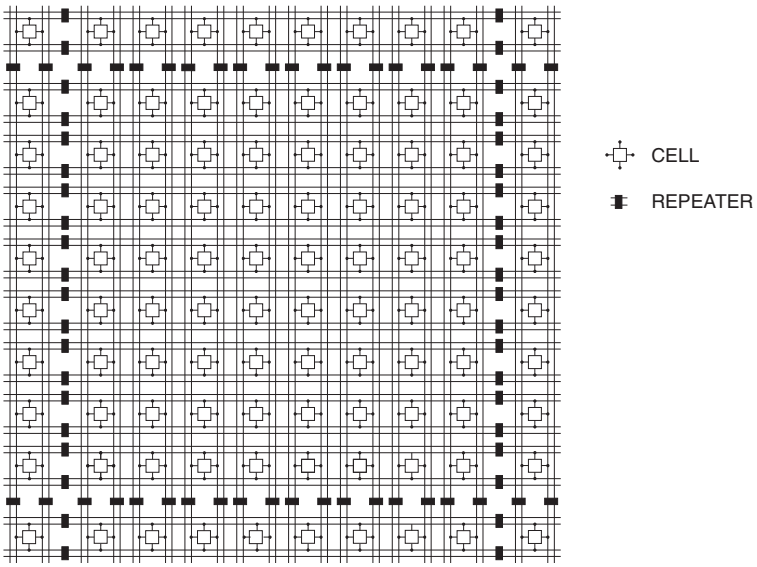
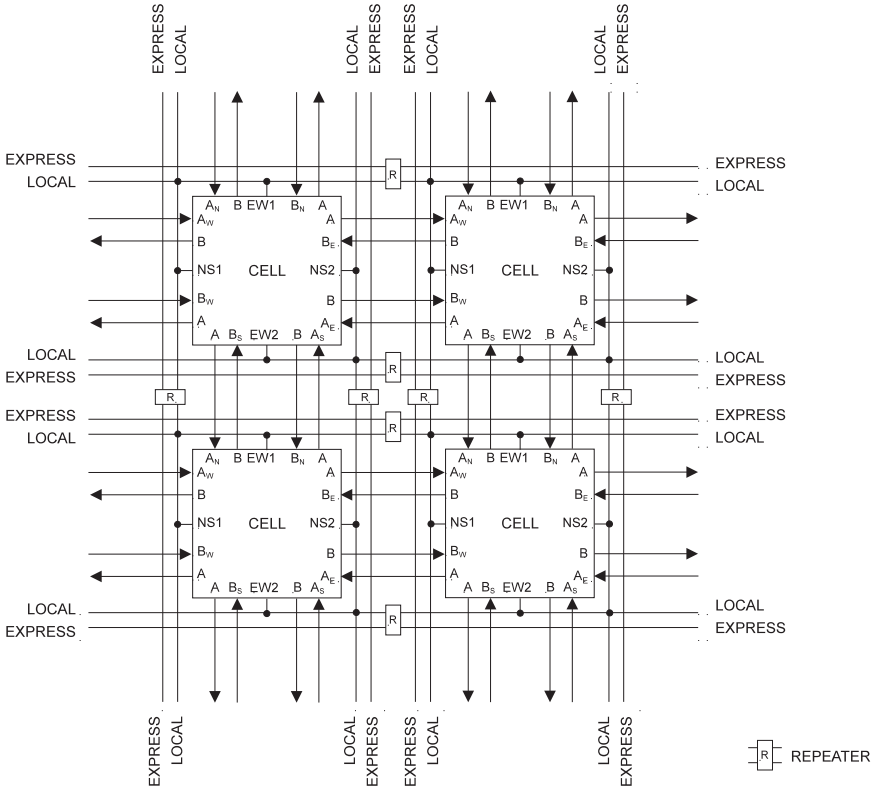


Figure 3. Cell-to-cell and Bus-to-bus Connections



Each cell, in addition, provides the ability to route a signal on a 90° turn between the NS1 bus and EW1 bus and between the NS2 bus and EW2 bus.

Express buses are not connected directly to cells, and thus provide higher speeds. They are the fastest way to cover long, straight-line distances within the array.

Each express bus is paired with a local bus, so there are two express buses for every column and two express buses for every row of cells.

Connective units, called repeaters, spaced every eight cells, divide each bus, both local and express, into segments spanning eight cells. Repeaters are aligned in rows and columns thereby partitioning the array into 8 x 8 sectors of cells. Each repeater is associated with a local/express pair, and on each side of the repeater are connections to a local-bus segment and an express-bus segment. The repeater can be programmed to provide any one of twenty-one connecting functions. These functions are symmetric with respect to both the two repeater sides and the two types of buses.

Among the functions provided are the ability to:

- Isolate bus segments from one another
- Connect two local-bus segments
- Connect two express-bus segments
- Implement a local/express transfer

In all of these cases, each connection provides signal regeneration and is thus unidirectional. For bidirectional connections, the basic repeater function for the NS2 and EW2 repeaters is augmented with a special programmable connection allowing bidirectional communication between local-bus segments. This option is primarily used to implement long, tristate buses.

The Cell Structure

The Atmel cell (Figure 4) is simple and small and yet can be programmed to perform all the logic and wiring functions needed to implement any digital circuit. Its four sides are functionally identical, so each cell is completely symmetrical.

Read/write access to the four local buses – NS1, EW1, NS2 and EW2 – is controlled, in part, by four bidirectional pass gates connected directly to the buses. To read a local bus, the pass gate for that bus is turned on and the three-input multiplexer is set accordingly. To write to a local bus, the pass gate for that bus and the pass gate for the associated tristate driver are both turned on. The two-input multiplexer supplying the control signal to the drivers permits either: (1) active drive, or (2) dynamic tristating controlled by the B input. Turning between L_{NS1} and L_{EW1} or between L_{NS2} and L_{EW2} is accomplished by turning on the two associated pass gates. The operations of reading, writing and turning are subject to the restriction that each bus can be involved in no more than a ***single*** operation.

Figure 4. Cell Structure

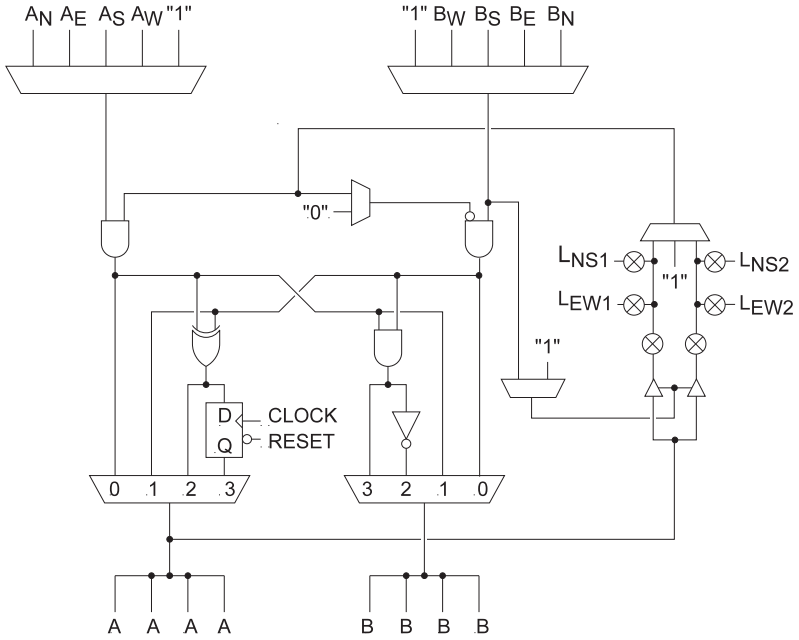


Figure 5. Combinatorial Physical States

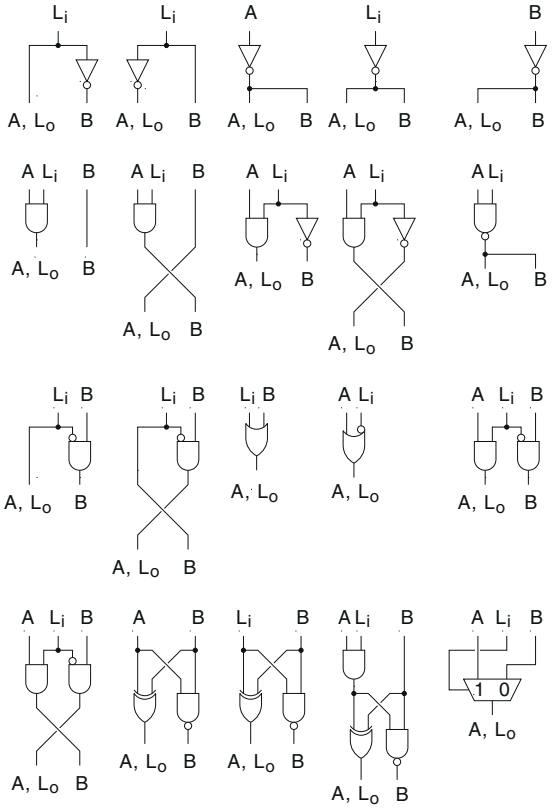


Figure 6. Register States

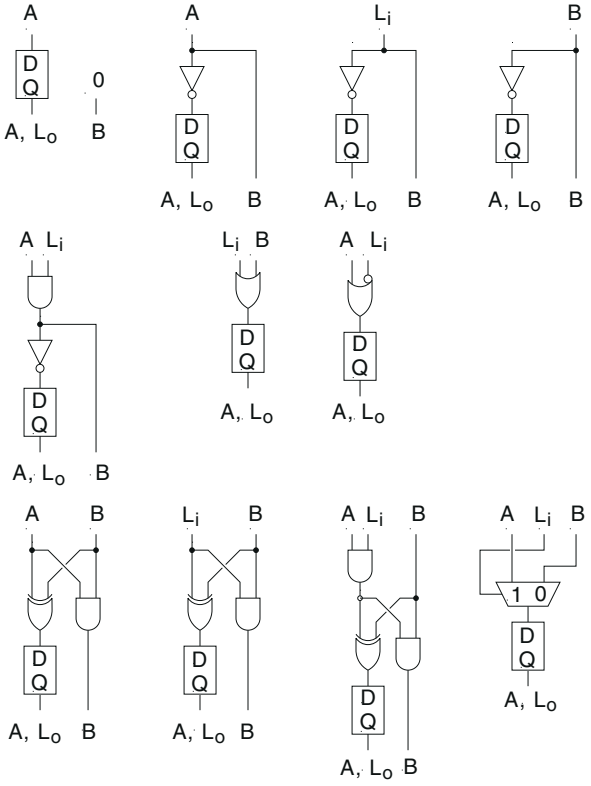


Figure 7. Physical Constants

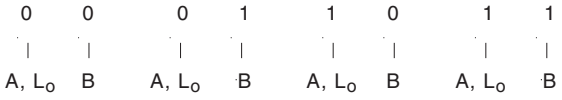


Figure 8. Two-input AND Feeding XOR

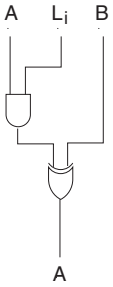
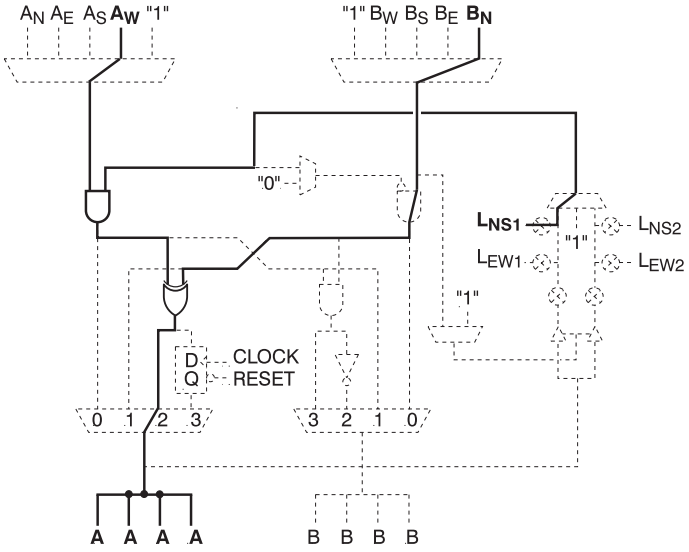


Figure 9. Cell Configuration (A•L) XOR B



The devices can be partially reconfigured while in operation. Portions of the device not being modified remain operational during reconfiguration. Simultaneous configuration of more than one device is also possible. Full configuration takes as little as a millisecond, partial configuration is even faster.

Refer to the Pin Function Description section following for a brief summary of the pins used in configuration. For more information about configuration, refer to the AT6000 Series Configuration data sheet.

Pin Function Description

This section provides abbreviated descriptions of the various AT6000 Series pins. For more complete descriptions, refer to the AT6000 Series Configuration data sheet.

Pinout tables for the AT6000 series of devices follow.

Power Pins

V_{CC}, V_{DD}, GND, V_{SS}

V_{CC} and GND are the I/O supply pins, V_{DD} and V_{SS} are the internal logic supply pins. V_{CC} and V_{DD} should be tied to the same trace on the printed circuit board. GND and V_{SS} should be tied to the same trace on the printed circuit board.

Input/Output Pins

All I/O pins can be used in the same way (refer to the I/O section of the architecture description). Some I/O pins are dual-function pins used during configuration of the array. When not being used for configuration, dual-function I/Os are fully functional as normal I/O pins. On initial power-up, all I/Os are configured as TTL inputs with a pull-up.

Dedicated Timing and Control Pins

$\overline{CON}$

Configuration-in-process pin. After power-up, $\overline{CON}$ staysLow until power-up initialization is complete, at which time $\overline{CON}$ is then released. $\overline{CON}$ is an open collector signal. After power-up initialization, forcing $\overline{CON}$ low begins the configuration process.

$\overline{CS}$

Configuration enable pin. All configuration pins are ignored if $\overline{CS}$ is high. $\overline{CS}$ must be held low throughout the configuration process. $\overline{CS}$ is a TTL input pin.

M0, M1, M2

Configuration mode pins are used to determine the configuration mode. All three are TTL input pins.

CCLK

Configuration clock pin. CCLK is a TTL input or a CMOS output depending on the mode of operation. In modes 1, 2, 3, and 6 it is an input. In modes 4 and 5 it is an output with a typical frequency of 1 MHz. In all modes, the rising edge of the CCLK signal is used to sample inputs and change outputs.

CLOCK

External logic source used to drive the internal global clock line. Registers toggle on the rising edge of CLOCK. The CLOCK signal is neither used nor affected by the configuration modes. It is always a TTL input.

$\overline{RESET}$

Array register asynchronous reset. $\overline{RESET}$ drives the internal global reset. The $\overline{RESET}$ signal is neither used nor affected by the configuration modes. It is always a TTL input.

Dual-function Pins

When $\overline{CON}$ is high, dual-function I/O pins act as device I/Os; when $\overline{CON}$ is low, dual-function pins are used as configuration control or data signals as determined by the configuration modes. Care must be taken when using these pins to ensure that configuration activity does not interfere with other circuitry connected to these pins in the application.

D0 or I/O

Serial configuration modes use D0 as the serial data input pin. Parallel configuration modes use D0 as the least-significant bit. Input data must meet setup and hold requirements with respect to the rising edge of CCLK. D0 is a TTL input during configuration.

D1 to D7 or I/O

Parallel configuration modes use these pins as inputs. Serial configuration modes do not use them. Data must meet setup and hold requirements with respect to the rising edge of CCLK. D1 - D7 are TTL inputs during configuration.

A0 to A16 or I/O

During configuration in modes 1, 2 and 5, these pins are CMOS outputs and act as the address pins for a parallel EPROM. A0 - A16 eliminates the need for an external address counter when using an external parallel nonvolatile

memory to configure the FPGA. Addresses change after the rising edge of the CCLK signal.

$\overline{\text{CSOUT}}$ or I/O

When cascading devices, $\overline{\text{CSOUT}}$ is an output used to enable other devices. $\overline{\text{CSOUT}}$ should be connected to the $\overline{\text{CS}}$ input of the downstream device. The $\overline{\text{CSOUT}}$ function is optional and can be disabled during initial programming when cascading is not used. When cascading devices, $\overline{\text{CSOUT}}$ should be dedicated to configuration and not used as a configurable I/O.

$\overline{\text{CHECK}}$ or I/O

During configuration, $\overline{\text{CHECK}}$ is a TTL input that can be used to enable the data check function at the beginning of a configuration cycle. No data is written to the device while $\overline{\text{CHECK}}$ is low. Instead, the configuration file being applied to D0 (or D0 - D7, in parallel mode) is compared with the current contents of the internal configuration RAM. If a mismatch is detected between the data being loaded and the data already in the RAM, the $\overline{\text{ERR}}$ pin goes low. The $\overline{\text{CHECK}}$ function is optional and can be disabled during initial programming.

$\overline{\text{ERR}}$ or I/O

During configuration, $\overline{\text{ERR}}$ is an output. When the $\overline{\text{CHECK}}$ function is activated and a mismatch is detected between the current configuration data stream and the data already loaded in the configuration RAM, $\overline{\text{ERR}}$ goes low. The $\overline{\text{ERR}}$ ouput is a registered signal. Once a mismatch is found, the signal is set and is only reset after the configuration cycle is restarted. $\overline{\text{ERR}}$ is also asserted for configuration file errors. The $\overline{\text{ERR}}$ function is optional and can be disabled during initial programming.

Device Pinout Selection (Max. Number of User I/O)

	AT6002[1]	AT6003[1]	AT6005	AT6010
84 PLCC[1]	64 I/O	64 I/O	64 I/O	-
100 VQFP	80 I/O	80 I/O	80 I/O	-
132 PQFP[1]	96 I/O	108 I/O	-	-
144 TQFP	95 I/O	120 I/O	108 I/O	120 I/O
208 PQFP[1]	-	-	-	-
240 PQFP	-	-	-	204 I/O

Bit-stream Sizes

Mode(s)	Type	Beginning Sequence	AT6002[1]	AT6003[1]	AT6005	AT6010
1	Parallel	Preamble	2677	4153	8077	16393
2	Parallel	Preamble	2677	4153	8077	16393
3	Serial	Null Byte/Preamble	2678	4154	8078	16394
4	Serial	Null Byte/Preamble	2678	4154	8078	16394
5	Parallel	Preamble	2677	4153	8077	16393
6	Parallel	Preamble/Preamble	2678	4154	8078	16394

Note: 1. Obsolete. Not recommended for new design.

Pinout Assignment

Left Side (Top to Bottom)										
AT6002[3]	AT6003[3]	AT6005	AT6010	84[3] PLCC	100 VQFP	132[3] PQFP	144 TQFP	180[3] CPGA	208[3] PQFP	240[3] PQFP
-	-	-	I/O51(A)	-	-	-	-	B1	1	1
I/O24(A) or A7	I/O30(A) or A7	I/O27(A) or A7	I/O50(A) or A7	12	1	18	1	C1	2	2
-	I/O29(B)	-	I/O49(A)	-	-	-	2	D1	3	3
-	-	-	I/O48(B)	-	-	-	-	-	-	4
-	-	-	VCC	-	-	-	-	PWR[1]	4	5
-	-	-	I/O47(A)	-	-	-	-	E1	5	6
-	-	-	GND	-	-	-	-	GND[2]	6	7
-	I/O28(A)	I/O26(A)	I/O46(A)	-	-	19	3	G1	7	8
I/O23(A) or A6	I/O27(A) or A6	I/O25(A) or A6	I/O45(A) or A6	13	2	20	4	H1	8	9
-	-	-	I/O44(B)	-	-	-	-	-	-	10
-	-	-	I/O43(A)	-	-	-	-	C2	9	11
I/O22(B)	I/O26(A)	I/O24(A)	I/O42(A)	-	-	21	5	D2	10	12
I/O21(A) or A5	I/O25(A) or A5	I/O23(A) or A5	I/O41(A) or A5	14	3	22	6	E2	11	13
-	-	-	I/O40(B)	-	-	-	-	-	-	14
-	-	-	I/O39(A)	-	-	-	-	F2	12	15
I/O20(B)	I/O24(B)	I/O22(A)	I/O38(A)	-	4	23	7	G2	13	16
I/O19(A) or A4	I/O23(A) or A4	I/O21(A) or A4	I/O37(A) or A4	15	5	24	8	H2	14	17
-	-	-	I/O36(B)	-	-	-	-	-	-	18
I/O18(B)	I/O22(B)	I/O20(A)	I/O35(A)	-	-	25	9	D3	15	19
I/O17(A) or A3	I/O21(A) or A3	I/O19(A) or A3	I/O34(A) or A3	16	6	26	10	E3	16	20
I/O16(B)	I/O20(B)	I/O18(A)	I/O33(A)	-	7	27	11	F3	17	21
-	-	-	I/O32(B)	-	-	-	-	-	18	22
I/O15(A) or A2	I/O19(A) or A2	I/O17(A) or A2	I/O31(A) or A2	17	8	28	12	G3	19	23
-	I/O18(B)	I/O16(A)	I/O30(A)	-	-	29	13	H3	20	24
GND	GND	GND	GND	18	9	30	14	GND[2]	21	25
VSS	VSS	VSS	VSS	19	10	31	15	GND[2]	22	26
I/O14(A) or A1	I/O17(A) or A1	I/O15(A) or A1	I/O29(A) or A1	20	11	32	16	F4	23	27
-	-	-	I/O28(B)	-	-	-	-	-	24	28
-	I/O16(B)	-	I/O27(A)	-	-	-	17	G4	25	29
I/O13(A) or A0	I/O15(A) or A0	I/O14(A) or A0	I/O26(A) or A0	21	12	33	18	H4	26	30
I/O12(B) or D7	I/O14(A) or D7	I/O13(A) or D7	I/O25(B) or D7	22	13	34	19	H5	27	31
-	-	-	I/O24(B)	-	-	-	-	-	28	32
I/O11(A) or D6	I/O13(A) or D6	I/O12(A) or D6	I/O23(A) or D6	23	14	35	20	J4	29	33

Notes: 1. PWR = Pins connected to power plane = F1, E4/E5, L2, R4, K15, L12, E14, A12.
2. GND = Pins connected to ground plane = L4, M4, N9, N10, E12, D12, C7, C6.
3. Obsolete. Not recommended for new design.

Pinout Assignment (Continued)

Left Side (Top to Bottom)										
AT6002[3]	**AT6003[3]**	**AT6005**	**AT6010**	**84[3] PLCC**	**100 VQFP**	**132[3] PQFP**	**144 TQFP**	**180[3] CPGA**	**208[3] PQFP**	**240[3] PQFP**
I/O10(A) or D5	I/O12(A) or D5	I/O11(A) or D5	I/O22(A) or D5	24	15	36	21	K4	30	34
VDD	VDD	VDD	VDD	25	16	37	22	PWR[1]	31	35
VCC	VCC	VCC	VCC	26	17	38	23	PWR[1]	32	36
I/O9(B)	I/O11(B)	I/O10(A)	I/O21(A)	-	-	39	24	J3	33	37
-	-	-	I/O20(B)	-	-	-	-	-	34	38
I/O8(A) or D4	I/O10(A) or D4	I/O9(A) or D4	I/O19(A) or D4	27	18	40	25	K3	35	39
I/O7(B)	I/O9(B)	I/O8(A)	I/O18(A)	-	19	41	26	L3	36	40
-	-	-	I/O17(A)	-	-	-	-	M3	37	41
-	-	-	I/O16(B)	-	-	-	-	-	-	42
I/O6(A) or D3	I/O8(A) or D3	I/O7(A) or D3	I/O15(A) or D3	28	20	42	27	N3	38	43
-	I/O7(B)	I/O6(A)	I/O14(A)	-	-	43	28	J2	39	44
-	-	-	I/O13(A)	-	-	-	-	K2	40	45
GND	GND	GND	GND	-	-	44	29	GND[2]	41	46
-	-	-	VSS	-	-	-	-	GND[2]	42	47
-	-	-	I/O12(B)	-	-	-	-	-	-	48
I/O5(A) or D2	I/O6(A) or D2	I/O5(A) or D2	I/O11(A) or D2	29	21	45	30	M2	43	49
I/O4(B)	I/O5(B)	I/O4(A)	I/O10(A)	-	22	46	31	N2	44	50
-	-	-	I/O9(A)	-	-	-	-	P2	45	51
-	-	-	I/O8(B)	-	-	-	-	-	-	52
I/O3(A) or D1	I/O4(A) or D1	I/O3(A) or D1	I/O7(A) or D1	30	23	47	32	J1	46	53
I/O2(B)	I/O3(A)	I/O2(A)	I/O6(A)	-	-	48	33	K1	47	54
-	-	-	I/O5(A)	-	-	-	-	L1	48	55
-	-	-	I/O4(B)	-	-	-	-	-	-	56
-	I/O2(B)	-	I/O3(A)	-	-	-	34	M1	49	57
I/O1(A) or D0	I/O1(A) or D0	I/O1(A) or D0	I/O2(A) or D0	31	24	49	35	N1	50	58
-	-	-	I/O1(A)	-	-	-	-	P1	51	59
CCLK	CCLK	CCLK	CCLK	32	25	50	36	R1	52	60

Notes: 1. PWR = Pins connected to power plane = F1, E4/E5, L2, R4, K15, L12, E14, A12.
2. GND = Pins connected to ground plane = L4, M4, N9, N10, E12, D12, C7, C6.
3. Obsolete. Not recommended for new design.

Pinout Assignment

Bottom Side (Left to Right)										
AT6002[3]	AT6003[3]	AT6005	AT6010	84[3] PLCC	100 VQFP	132[3] PQFP	144 TQFP	180[3] CPGA	208[3] PQFP	240[3] PQFP
$\overline{CON}$	$\overline{CON}$	$\overline{CON}$	$\overline{CON}$	33	26	51	37	M5	53	61
-	-	-	I/O204(A)	-	-	-	-	M6	54	62
I/O96(A)	I/O120(A)	I/O108(A)	I/O203(A)	34	27	52	38	M7	55	63
-	I/O119(B)	-	I/O202(A)	-	-	-	39	R2	56	64
-	-	-	I/O201(B)	-	-	-	-	-	-	65
-	-	-	VCC	-	-	-	-	PWR[1]	57	66
-	-	-	I/O200(A)	-	-	-	-	R3	58	67
-	-	-	GND	-	-	-	-	GND[2]	59	68
-	I/O118(A)	I/O107(A)	I/O199(A)	-	-	53	40	R5	60	69
I/O95(A) or $\overline{CSOUT}$	I/O117(A) or $\overline{CSOUT}$	I/O106(A) or $\overline{CSOUT}$	I/O198(A) or $\overline{CSOUT}$	35	28	54	41	R6	61	70
-	-	-	I/O197(B)	-	-	-	-	-	-	71
-	-	-	I/O196(A)	-	-	-	-	R7	62	72
I/O94(B)	I/O116(A)	I/O105(A)	I/O195(A)	-	-	55	42	P3	63	73
I/O93(A)	I/O115(A)	I/O104(A)	I/O194(A)	36	29	56	43	P4	64	74
-	-	-	I/O193(B)	-	-	-	-	-	-	75
-	-	-	I/O192(A)	-	-	-	-	P5	65	76
I/O92(B)	I/O114(B)	I/O103(A)	I/O191(A)	-	30	57	44	P6	66	77
I/O91(A) or $\overline{CHECK}$	I/O113(A) or $\overline{CHECK}$	I/O102(A) or $\overline{CHECK}$	I/O190(A) or $\overline{CHECK}$	37	31	58	45	P7	67	78
-	-	-	I/O189(B)	-	-	-	-	-	-	79
I/O90(B)	I/O112(B)	I/O101(A)	I/O188(A)	-	-	59	46	N4	68	80
I/O89(A) or $\overline{ERR}$	I/O111(A) or $\overline{ERR}$	I/O100(A) or $\overline{ERR}$	I/O187(A) or $\overline{ERR}$	38	32	60	47	N5	69	81
I/O88(B)	I/O110(B)	I/O99(A)	I/O186(A)	-	33	61	48	N6	70	82
-	-	-	I/O185(B)	-	-	-	-	-	71	83
I/O87(A)	I/O109(A)	I/O98(A)	I/O184(A)	39	34	62	49	N7	72	84
-	I/O108(B)	I/O97(A)	I/O183(A)	-	-	63	50	M8	73	85
GND	GND	GND	GND	40	35	64	51	GND[2]	74	86
I/O86(A)	I/O107(A)	I/O96(A)	I/O182(A)	41	36	65	52	M9	75	87
-	-	-	I/O181(B)	-	-	-	-	-	76	88
-	I/O106(B)	-	I/O180(A)	-	-	-	53	M10	77	89
I/O85(A)	I/O105(A)	I/O95(A)	I/O179(A)	42	37	66	54	M11	78	90
$\overline{CS}$	$\overline{CS}$	$\overline{CS}$	$\overline{CS}$	43	38	67	55	L8	79	91
I/O84(B)	I/O104(A)	I/O94(A)	I/O178(A)	44	39	68	56	M12	80	92

Notes: 1. PWR = Pins connected to power plane = F1, E4/E5, L2, R4, K15, L12, E14, A12.
2. GND = Pins connected to ground plane = L4, M4, N9, N10, E12, D12, C7, C6.
3. Obsolete. Not recommended for new design.

Pinout Assignment (Continued)

Bottom Side (Left to Right)										
AT6002[3]	**AT6003[3]**	**AT6005**	**AT6010**	**84[3] PLCC**	**100 VQFP**	**132[3] PQFP**	**144 TQFP**	**180[3] CPGA**	**208[3] PQFP**	**240[3] PQFP**
-	-	-	I/O177(B)	-	-	-	-	-	81	93
I/O83(A)	I/O103(A)	I/O93(A)	I/O176(A)	45	40	69	57	N8	82	94
-	-	-	VDD	-	-	-	-	PWR[1]	83	95
VCC	VCC	VCC	VCC	46	41	70	58	PWR[1]	84	96
I/O82(A)	I/O102(A)	I/O92(A)	I/O175(A)	47	42	71	59	N11	85	97
I/O81(B)	I/O101(B)	I/O91(A)	I/O174(A)	-	-	72	60	N12	86	98
-	-	-	I/O173(B)	-	-	-	-	-	87	99
I/O80(A)	I/O100(A)	I/O90(A)	I/O172(A)	48	43	73	61	N13	88	100
I/O79(B)	I/O99(B)	I/O89(A)	I/O171(A)	-	44	74	62	P8	89	101
-	-	-	I/O170(A)	-	-	-	-	P9	90	102
-	-	-	I/O169(B)	-	-	-	-	-	-	103
I/O78(A)	I/O98(A)	I/O88(A)	I/O168(A)	49	45	75	63	P10	91	104
-	I/O97(B)	I/O87(A)	I/O167(A)	-	-	76	64	P11	92	105
-	-	-	I/O166(A)	-	-	-	-	P12	93	106
GND	GND	GND	GND	-	-	77	65	GND[2]	94	107
-	-	-	I/O165(B)	-	-	-	-	-	-	108
I/O77(A)	I/O96(A)	I/O86(A)	I/O164(A)	50	46	78	66	P13	95	109
I/O76(B)	I/O95(B)	I/O85(A)	I/O163(A)	-	47	79	67	P14	96	110
-	-	-	I/O162(A)	-	-	-	-	P8	97	111
-	-	-	I/O161(B)	-	-	-	-	-	-	112
I/O75(A)	I/O94(A)	I/O84(A)	I/O160(A)	51	48	80	68	R9	98	113
I/O74(B)	I/O93(A)	I/O83(A)	I/O159(A)	-	-	81	69	R10	99	114
-	-	-	I/O158(A)	-	-	-	-	R11	100	115
-	-	-	I/O157(B)	-	-	-	-	-	-	116
-	I/O92(B)	-	I/O156(A)	-	-	-	70	R12	101	117
I/O73(A)	I/O91(A)	I/O82(A)	I/O155(A)	52	49	82	71	R13	102	118
-	-	-	I/O154(A)	-	-	-	-	R14	103	119
$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	53	50	83	72	R15	104	120

Notes:
1. PWR = Pins connected to power plane = F1, E4/E5, L2, R4, K15, L12, E14, A12.
2. GND = Pins connected to ground plane = L4, M4, N9, N10, E12, D12, C7, C6.
3. Obsolete. Not recommended for new design.

Pinout Assignment

Right Side (Bottom to Top)										
AT6002[5]	**AT6003[5]**	**AT6005**	**AT6010**	**84[5] PLCC**	**100 VQFP**	**132[5] PQFP**	**144 TQFP**	**180[5] CPGA**	**208[5] PQFP**	**240[5] PQFP**
-	-	-	I/O153(A)	-	-	-	-	P15	105	121
I/O72(A)	I/O90(A)	I/O81(A)	I/O152(A)	54	51	84	73	N15	106	122
-	I/O89(B)	I/O80(A)	I/O151(A)	-	-	85[3]	74	M15	107	123
-	-	-	I/O150(B)	-	-	-	-	-	-	124
-	-	-	VCC	-	-	-	-	PWR[1]	108	125
-	-	-	I/O149(A)	-	-	-	-	L15	109	126
-	-	-	GND	-	-	-	-	GND[2]	110	127
-	I/O88(A)	-	I/O148(A)	-	-	85[4]	75	J15	111	128
I/O71(A)	I/O87(A)	I/O79(A)	I/O147(A)	55	52	86	76	H15	112	129
-	-	-	I/O146(B)	-	-	-	-	-	-	130
-	-	-	I/O145(A)	-	-	-	-	N14	113	131
I/O70(B)	I/O86(A)	I/O78(A)	I/O144(A)	-	-	87	77	M14	114	132
I/O69(A)	I/O85(A)	I/O77(A)	I/O143(A)	56	53	88	78	L14	115	133
-	-	-	I/O142(B)	-	-	-	-	-	-	134
-	-	-	I/O141(A)	-	-	-	-	K14	116	135
I/O68(B)	I/O84(B)	I/O76(A)	I/O140(A)	-	54	89	79	J14	117	136
I/O67(A)	I/O83(A)	I/O75(A)	I/O139(A)	57	55	90	80	H14	118	137
-	-	-	I/O138B	-	-	-	-	-	-	138
I/O66(B)	I/O82(B)	I/O74(A)	I/O137(A)	-	-	91	81	M13	119	139
I/O65(A)	I/O81(A)	I/O73(A)	I/O136(A)	58	56	92	82	L13	120	140
I/O64(B)	I/O80(B)	I/O72(A)	I/O135(A)	-	57	93	83	K13	121	141
-	-	-	I/O134(B)	-	-	-	-	-	122	142
I/O63(A)	I/O79(A)	I/O71(A	I/O133(A)	59	58	94	84	J13	123	143
-	I/O78(B)	I/O70(A)	I/O132(A)	-	-	95	85	H13	124	144
GND	GND	GND	GND	60	59	96	86	GND[2]	125	145
VSS	VSS	VSS	VSS	61	60	97	87	GND[2]	126	146
I/O62(A)	I/O77(A)	I/O69(A)	I/O131(A)	62	61	98	88	K12	127	147
-	-	-	I/O130(B)	-	-	-	-	-	128	148
-	I/O76(B)	-	I/O129(A)	-	-	-	89	J12	129	149
I/O61(A)	I/O75(A)	I/O68(A)	I/O128(A)	63	62	99	90	H12	130	150
I/O60(B)	I/O74(A)	I/O67(A)	I/O127(A)	64	63	100	91	H11	131	151
-	-	-	I/O126(B)	-	-	-	-	-	132	152

Notes:
1. PWR = Pins connected to power plane = F1, E4/E5, L2, R4, K15, L12, E14, A12.
2. GND = Pins connected to ground plane = L4, M4, N9, N10, E12, D12, C7, C6.
3. 85 = Pin 85 on AT6005.
4. 85 = Pin 85 on AT6003 and AT6010.
5. Obsolete. Not recommended for new design.

Pinout Assignment (Continued)

Top Side (Right to Left)										
AT6002[3]	**AT6003[3]**	**AT6005**	**AT6010**	**84[3] PLCC**	**100 VQFP**	**132[3] PQFP**	**144 TQFP**	**180[3] CPGA**	**208[3] PQFP**	**240[3] PQFP**
-	-	-	I/O75(B)	-	-	-	-	-	185	213
I/O35(A) or A14	I/O43(A) or A14	I/O39(A) or A14	I/O74(A) or A14	3	90	3	129	C8	186	214
-	-	-	VDD	-	-	-	-	PWR[1]	187	215
VCC	VCC	VCC	VCC	4	91	4	130	PWR[1]	188	216
I/O34(A) or A13	I/O42(A) or A13	I/O38(A) or A13	I/O73(A) or A13	5	92	5	131	C5	189	217
I/O33(B)	I/O41(B)	I/O37(A)	I/O72(A)	-	-	6	132	C4	190	218
-	-	-	I/O71(B)	-	-	-	-	-	191	219
I/O32(A) or A12	I/O40(A) or A12	I/O36(A) or A12	I/O70(A) or A12	6	93	7	133	C3	192	220
I/O31(B)	I/O39(B)	I/O35(A)	I/O69(A)	-	94	8	134	B8	193	221
-	-	-	I/O68(A)	-	-	-	-	B7	194	222
-	-	-	I/O67(B)	-	-	-	-	-	-	223
I/O30(A) or A11	I/O38(A) or A11	I/O34(A) or A11	I/O66(A) or A11	7	95	9	135	B6	195	224
-	I/O37(B)	I/O33(A)	I/O65(A)	-	-	10	136	B5	196	225
-	-	-	I/O64(A)	-	-	-	-	B4	197	226
GND	GND	GND	GND	-	-	11	137	GND[2]	198	227
-	-	-	I/O63(B)	-	-	-	-	-	-	228
I/O29(A) or A10	I/O36(A) or A10	I/O32(A) or A10	I/O62(A) or A10	8	96	12	138	B3	199	229
I/O28(B)	I/O35(B)	I/O31(A)	I/O61(A)	-	97	13	139	B2	200	230
-	-	-	I/O60(A)	-	-	-	-	A8	201	231
-	-	-	I/O59(B)	-	-	-	-	-	-	232
I/O27(A) or A9	I/O34(A) or A9	I/O30(A) or A9	I/O58(A) or A9	9	98	14	140	A7	202	233
I/O26(B)	I/O33(A)	I/O29(A)	I/O57(A)	-	-	15	141	A6	203	234
-	-	-	I/O56(A)	-	-	-	-	A5	204	235
-	-	-	I/O55(B)	-	-	-	-	-	-	236
-	I/O32(B)	-	I/O54(A)	-	-	-	142	A4	205	237
I/O25(A) or A8	I/O31(A) or A8	I/O28(A) or A8	I/O53(A) or A8	10	99	16	143	A3	206	238
-	-	-	I/O52(A)	-	-	-	-	A2	-207	239
M0	M0	M0	M0	11	100	17	144	A1	208	240

Notes:
1. PWR = Pins connected to power plane = F1, E4/E5, L2, R4, K15, L12, E14, A12.
2. GND = Pins connected to ground plane = L4, M4, N9, N10, E12, D12, C7, C6.
3. Obsolete. Not recommended for new design.

AC Timing Characteristics – 5V Operation

Delays are based on fixed load. Loads for each type of device are described in the notes. Delays are in nanoseconds. Worst case: V_{CC} = 4.75V to 5.25V. Temperature = 0°C to 70°C.

Cell Function	Parameter	From	To	Load Definition(7)	-1	-2	-4	Units
Wire(4)	t_{PD} (max)(4)	A, B, L	A, B	1	0.8	1.2	1.8	ns
NAND	t_{PD} (max)	A, B, L	B	1	1.6	2.2	3.2	ns
XOR	t_{PD} (max)	A, B, L	A	1	1.8	2.4	4.0	ns
AND	t_{PD} (max)	A, B, L	B	1	1.7	2.2	3.2	ns
MUX	t_{PD} (max)	A, B	A	1	1.7	2.3	4.0	ns
		L	A	1	2.1	3.0	4.9	ns
D-Flip-flop(5)	t_{setup} (min)	A, B, L	CLK	-	1.5	2.0	3.0	ns
D-Flip-flop(5)	t_{hold} (min)	CLK	A, B, L	-	0	0	0	ns
D-Flip-flop	t_{PD} (max)	CLK	A	1	1.5	2.0	3.0	ns
Bus Driver	t_{PD} (max)	A	L	2	2.0	2.6	4.0	ns
Repeater	t_{PD} (max)	L, E	E	3	1.3	1.6	2.3	ns
		L, E	L	2	1.7	2.1	3.0	ns
Column Clock	t_{PD} (max)	GCLK, A, ES	CLK	3	1.8	2.4	3.0	ns
Column Reset	t_{PD} (max)	GRES, A, EN	RES	3	1.8	2.4	3.0	ns
Clock Buffer(5)	t_{PD} (max)	CLOCK PIN	GCLK	-	1.6	2.0	2.9	ns
Reset Buffer(5)	t_{PD} (max)	RESET PIN	GRES	-	1.5	1.9	2.8	ns
TTL Input(1)	t_{PD} (max)	I/O	A	3	1.0	1.2	1.5	ns
CMOS Input(2)	t_{PD} (max)	I/O	A	3	1.3	1.4	2.3	ns
Fast Output(3)	t_{PD} (max)	A	I/O PIN	4	3.3	3.5	6.0	ns
Slow Output(3)	t_{PD} (max)	A	I/O PIN	4	7.5	8.0	12.0	ns
Output Disable(5)	t_{PXZ} (max)	L	I/O PIN	4	3.1	3.3	5.5	ns
Fast Enable(3)(5)	t_{PXZ} (max)	L	I/O PIN	4	3.8	4.0	6.5	ns
Slow Enable(3)(5)	t_{PXZ} (max)	L	I/O PIN	4	8.2	8.5	12.5	ns

Device	Cell Types	Outputs	I_{CC} (max)
Cell(6)	Wire, XWire, Half-adder, Flip-flop	A, B	4.5 µA/MHz
Bus(6)	Wire, XWire, Half-adder, Flip-flop, Repeater	L	2.5 µA/MHz
Column Clock(6)	Column Clock Driver	CLK	40 µA/MHz

Notes:
1. TTL buffer delays are measured from a V_{IH} of 1.5V at the pad to the internal V_{IH} at A. The input buffer load is constant.
2. CMOS buffer delays are measured from a V_{IH} of 1/2 V_{CC} at the apd to the internal V_{IH} at A. The input buffer load is constant.
3. Buffer delay is to a pad voltage of 1.5V with one output switching.
4. Max specifications are the average of mas t_{PDLH} and t_{PDHL}.
5. Parameter based on characterization and simulation; not tested in production
6. Exact power calculation is available in an Atmel application note.
7. Load Definition: 1 = Load of one A or B input; 2 = Load of one L input; 3 = Constant Load; 4 = Tester Load of 50 pF.

AC Timing Characteristics – 3.3V Operation (8)

Delays are based on fixed load. Loads for each type of device are described in the notes. Delays are in nanoseconds. Worst case: V_{CC} = 3.0V to 3.6V. Temperature = 0°C to 70°C.

Cell Function	Parameter	From	To	Load Definition(7)	-4	Units
Wire(4)	t_{PD} (max)(4)	A, B, L	A, B	1	1.8	ns
NAND	t_{PD} (max)	A, B, L	B	1	3.2	ns
XOR	t_{PD} (max)	A, B, L	A	1	4.0	ns
AND	t_{PD} (max)	A, B, L	B	1	3.2	ns
MUX	t_{PD} (max)	A, B	A	1	4.0	ns
		L	A	1	4.9	ns
D-Flip-flop(5)	t_{setup} (min)	A, B, L	CLK	-	3.0	ns
D-Flip-flop(5)	t_{hold} (min)	CLK	A, B, L	-	0	ns
D-Flip-flop	t_{PD} (max)	CLK	A	1	3.0	ns
Bus Driver	t_{PD} (max)	A	L	2	4.0	ns
Repeater	t_{PD} (max)	L, E	E	3	2.3	ns
		L, E	L	2	3.0	ns
Column Clock	t_{PD} (max)	GCLK, A, ES	CLK	3	3.0	ns
Column Reset	t_{PD} (max)	GRES, A, EN	RES	3	3.0	ns
Clock Buffer(5)	t_{PD} (max)	CLOCK PIN	GCLK	4	2.9	ns
Reset Buffer(5)	t_{PD} (max)	RESET PIN	GRES	5	2.8	ns
TTL Input(1)	t_{PD} (max)	I/O	A	3	1.5	ns
CMOS Input(2)	t_{PD} (max)	I/O	A	3	2.3	ns
Fast Output(3)	t_{PD} (max)	A	I/O PIN	6	6.0	ns
Slow Output(3)	t_{PD} (max)	A	I/O PIN	6	12.0	ns
Output Disable(5)	t_{PXZ} (max)	L	I/O PIN	6	5.5	ns
Fast Enable(3)(5)	t_{PXZ} (max)	L	I/O PIN	6	6.5	ns
Slow Enable(3)(5)	t_{PXZ} (max)	L	I/O PIN	6	12.5	ns

Device	Cell Types	Outputs	I_{CC} (max)
Cell(6)	Wire, XWire, Half-adder, Flip-flop	A, B	2.3 µA/MHz
Bus(6)	Wire, XWire, Half-adder, Flip-flop, Repeater	L	1.3 µA/MHz
Column Clock(6)	Column Clock Driver	CLK	20 µA/MHz

Notes:
1. TTL buffer delays are measured from a V_{IH} of 1.5V at the pad to the internal V_{IH} at A. The input buffer load is constant.
2. CMOS buffer delays are measured from a V_{IH} of 1/2 V_{CC} at the apd to the internal V_{IH} at A. The input buffer load is constant.
3. Buffer delay is to a pad voltage of 1.5V with one output switching.
4. Max specifications are the average of mas t_{PDLH} and t_{PDHL}.
5. Parameter based on characterization and simulation; not tested in production
6. Exact power calculation is available in an Atmel application note.
7. Load Definition: 1 = Load of one A or B input; 2 = Load of one L input; 3 = Constant Load; 4 = Load of 28 Clock Columns; 5 = Load of 28 Reset Columns; 6 = Tester Load of 50 pF.
8. Obsolete. Not recommended for new design.

Absolute Maximum Ratings*

Supply Voltage (V_{CC})	-0.5V to + 7.0V
DC Input Voltage (V_{IN})	-0.5V to V_{CC} + 0.5V
DC Output Voltage (V_{ON})	-0.5V to V_{CC} + 0.5V
Storage Temperature Range (TSTG)	-65 °C to +150°C
Power Dissipation (PD)	1500 mW
Lead Temperature (T_L) (Soldering, 10 sec.)	260°C
ESD (R_{ZAP} = 1.5K, C_{ZAP} = 100 pF)	2000V

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress rating only and functional operation of the device at these or any other conditions beyond those listed under operating conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

DC and AC Operating Rage – 5V Operation

		AT6002-2/4(1) AT6003-2/4(1) AT6005-2/4(1) AT6010-2/4(1) Commercial(1)	**AT6002-2/4(1) AT6003-2/4(1) AT6005-2/4 AT6010-2/4 Industrial**	**AT6002-2/4(1) AT6003-2/4(1) AT6005-2/4(1) AT6010-2/4(1) Military(1)**
Operating Temperature (Case)		0°C - 70°C	-40°C - 85°C	-55°C - 125°C
V_{CC} Power Supply		5V ± 5%	5V ± 10%	5V ± 10%
Input Voltage Level (TTL)	High (V_{IHT})	2.0V - V_{CC}	2.0V - V_{CC}	2.0V - V_{CC}
	Low (V_{ILT})	0V - 0.8V	0V - 0.8V	0V - 0.8V
Input Voltage Level (CMOS)	High (V_{IHC})	70% - 100% V_{CC}	70% - 100% V_{CC}	70% - 100% V_{CC}
	Low (V_{ILC})	0 - 30% V_{CC}	0 - 30% V_{CC}	0 - 30% V_{CC}
Input Signal Transition Time (T_{IN})		50 ns (max)	50 ns (max)	50 ns (max)

DC and AC Operating Rage – 3.3V Operation(1)

		AT6002-2/4(1), AT6003-2/4(1) AT6005-2/4(1), AT6010-2/4(1) Commercial
Operating Temperature (Case)		0°C - 70°C
V_{CC} Power Supply		3.3V ± 5%
Input Voltage Level (TTL)	High (V_{IHT})	2.0V - V_{CC}
	Low (V_{ILT})	0V - 0.8V
Input Voltage Level (CMOS)	High (V_{IHC})	70% - 100% V_{CC}
	Low (V_{ILC})	0 - 30% V_{CC}
Input Signal Transition Time (T_{IN})		50 ns (max)

Note: 1. Obsolete. Not recommended for new design.

DC Characteristics – 5V Operation

Symbol	Parameter	Conditions		Min	Max	Units
V_{IH}	High-level Input Voltage	Commercial	CMOS	70% V_{CC}	V_{CC}	V
			TTL	2.0	V_{CC}	V
V_{IL}	Low-level Input Voltage	Commercial	CMOS	0	30% V_{CC}	V
			TTL	0	0.8	V
V_{OH}	High-level Output Voltage	Commercial	I_{OH} = -4 mA, V_{CC} min	3.9		V
			I_{OH} = -16 mA, V_{CC} min	3.0		V
V_{OL}	Low-level Output Voltage	Commercial	I_{OL} = 4 mA, V_{CC} min		0.4	V
			I_{OL} = 16 mA, V_{CC} min		0.5	V
I_{OZH}	High-level Tristate Output Leakage Current	$V_O = V_{CC}$ (max)			10	µA
I_{OZL}	High-level Tristate	Without Pull-up, $V_O = V_{SS}$		-10		µA
	Output Leakage Current	With Pull-up, $V_O = V_{SS}$		-500		µA
I_{IH}	High-level Input Current	$V_{IN} = V_{CC}$ (max)			10	µA
I_{IL}	Low-level Input Current	Without Pull-up, $V_{IN} = V_{SS}$		-10		µA
		With Pull-up, $V_{IN} = V_{SS}$		-500		µA
I_{CC}	Power Consumption	Without Internal Oscillator (Standby)			500	µA
C_{IN}	Input Capacitance	All Pins			10	pF

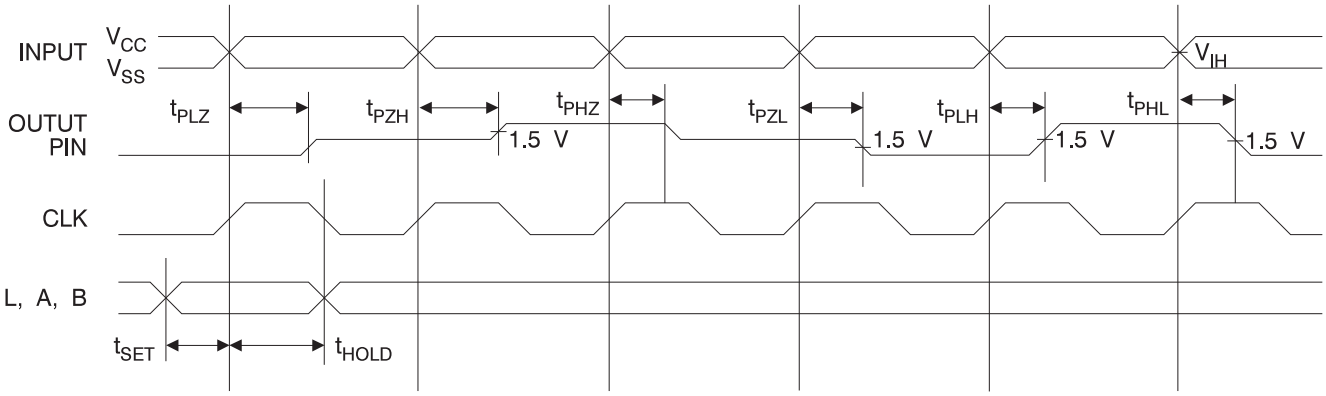
Note: 1. Obsolete. Not recommended for new design.

DC Characteristics – 3.3V Operation(2)

Symbol	Parameter	Conditions		Min	Max	Units
V_{IH}	High-level Input Voltage	Commercial	CMOS	70% V_{CC}	V_{CC}	V
			TTL	2.0	V_{CC}	V
V_{IL}	Low-level Input Voltage	Commercial	CMOS	0	30% V_{CC}	V
			TTL	0	0.8	V
V_{OH}	High-level Output Voltage	Commercial	I_{OH} = -2 mA, V_{CC} min	2.4		V
			I_{OH} = -6 mA, V_{CC} min	2.0		V
V_{OL}	Low-level Output Voltage	Commercial	I_{OL} = +2 mA, V_{CC} min		0.4	V
			I_{OL} = +6 mA, V_{CC} min		0.5	V
I_{OZH}	High-level Tristate Output Leakage Current	$V_O = V_{CC}$ (max)			10	µA
I_{OZL}	High-level Tristate	Without Pull-up, $V_O = V_{SS}$		-10		µA
	Output Leakage Current	With Pull-up, $V_O = V_{SS}$		-500		µA
I_{IH}	High-level Input Current	$V_{IN} = V_{CC}$ (max)			10	µA
I_{IL}	Low-level Input Current	Without Pull-up, $V_{IN} = V_{SS}$		-10		µA
		With Pull-up, $V_{IN} = V_{SS}$		-500		µA
I_{CC}	Power Consumption	Without Internal Oscillator (Standby)			200	µA
C_{IN}(1)	Input Capacitance	All Pins			10	pF

Notes: 1. Parameter based on characterization and simulation; it is not tested in production.
2. Obsolete. Not recommended for new design.

Device Timing: During Operation



Ordering Information – AT6003[1]

Usable Gates	Speed Grade (ns)	Ordering Code	Package	Operation Range
9,000	2	AT6003-2AC AT6003A-2AC AT6003-2JC AT6003-2QC	100A 144A 84J 132Q	5V Commercial (0°C to 70°C)
		AT6003-2AI AT6003A-2AI AT6003-2JI AT6003-2QI	100A 144A 84J 132Q	Industrial (-40°C to 85°C)
9,000	4	AT6003-4AC AT6003A-4AC AT6003-4JC AT6003-4QC	100A 144A 84J 132Q	5V Commercial (0°C to 70°C)
		AT6003LV-4AC AT6003ALV-4AC AT6003LV-4JC AT6003LV-4QC	100A 144A 84J 132Q	3.3V Commercial (0°C to 70°C)
		AT6003-4AI AT6003A-4AI AT6003-4JI AT6003-4QI	100A 144A 84J 132Q	5V Industrial (-40°C to 85°C)

Note: 1. Obsolete. Not recommended for new design.

Package Type	
84J	84-lead, Plastic J-leaded Chip Carrier (PLCC)
100A	100-lead, Very Thin (1.0 mm) Plastic Gull-Wing Quad Flat Package (VQFP)
132Q	132-lead, Bumpered Plastic Gull-Wing Quad Flat Package (BQFP)
144A	144-lead, Thin (1.4 mm) Plastic Gull-Wing Quad Flat Package (TQFP)
208Q	208-lead, Plastic Gull-Wing Quad Flat Package (PQFP)
240Q	240-lead, Plastic Gull-Wing Quad Flat Package (PQFP)

Ordering Information – AT6005

Usable Gates	Speed Grade (ns)	Ordering Code	Package	Operation Range
15,000	2	AT6005-2AU	100A	5V Industrial Temperature (-40°C to 85°C)
15,000	2	AT6005-2AC AT6005A-2AC AT6005-2JC AT6005-2QC AT6005A-2QC	100A 144A 84J 132Q 208Q	5V Commercial (0°C to 70°C)
		AT6005-2AI AT6005A-2AI AT6005-2JI AT6005-2QI AT6005A-2QI	100A 144A 84J 132Q 208Q	Industrial (-40°C to 85°C)
15,000	4	AT6005-4AC AT6005A-4AC AT6005-4JC AT6005-4QC AT6005A-4QC	100A 144A 84J 132Q 208Q	5V Commercial (0°C to 70°C)
		AT6005LV-4AC AT6005ALV-4AC AT6005LV-4JC AT6005LV-4QC AT6005ALV-4QC	100A 144A 84J 132Q 208Q	3.3V Commercial (0°C to 70°C)
		AT6005-4AI AT6005A-4AI AT6005-4JI AT6005-4QI AT6005A-4QI	100A 144A 84J 132Q 208Q	5V Commercial (-40°C to 85°C)

Note: 1 Obsolete. Package options are not recommended for new design.

Package Type	
84J	84-lead, Plastic J-leaded Chip Carrier (PLCC)
100A	100-lead, Very Thin (1.0 mm) Plastic Gull-Wing Quad Flat Package (VQFP)
132Q	132-lead, Bumpered Plastic Gull-Wing Quad Flat Package (BQFP)
144A	144-lead, Thin (1.4 mm) Plastic Gull-Wing Quad Flat Package (TQFP)
208Q	208-lead, Plastic Gull-Wing Quad Flat Package (PQFP)
240Q	240-lead, Plastic Gull-Wing Quad Flat Package (PQFP)

Ordering Information – AT6010

Usable Gates	Speed Grade (ns)	Ordering Code	Package	Operation Range
30,000	2	AT6010A-2AU	144A	5V Industrial Temperature (-40°C to 85°C)
30,000	2	AT6010-2JC AT6010A-2AC AT6010-2QC AT6010A-2QC AT6010H-2QC	84J 144A 132Q 208Q 240Q	5V Commercial (0°C to 70°C)
		AT6010-2JI AT6010A-2AI AT6010-2QI AT6010A-2QI AT6010H-2QI	84J 144A 132Q 208Q 240Q	Industrial (-40°C to 85°C)
30,000	4	AT6010A-4AC AT6010-4QC AT6010-4JC AT6010A-4QC AT6010H-4QC	144A 132Q 84J 208Q 240Q	5V Commercial (0°C to 70°C)
		AT6010ALV-4AC AT6010LV-4QC AT6010LV-4JC AT6010ALV-4QC AT6010HLV-4QC	144A 132Q 84J 208Q 240Q	3.3V Commercial (0°C to 70°C)
		AT6010A-4AI AT6010-4QI AT6010-4JI AT6010A-4QI AT6010H-4QI	144A 132Q 84J 208Q 240Q	5V Industrial (-40°C to 85°C)

Note: 1 Obsolete. Package options are not recommended for new design.

Package Type	
84J	84-lead, Plastic J-leaded Chip Carrier (PLCC)
100A	100-lead, Very Thin (1.0 mm) Plastic Gull-Wing Quad Flat Package (VQFP)
132Q	132-lead, Bumpered Plastic Gull-Wing Quad Flat Package (BQFP)
144A	144-lead, Thin (1.4 mm) Plastic Gull-Wing Quad Flat Package (TQFP)
208Q	208-lead, Plastic Gull-Wing Quad Flat Package (PQFP)
240Q	240-lead, Plastic Gull-Wing Quad Flat Package (PQFP)