



Welcome to [E-XFL.COM](https://www.e-xfl.com)

### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	6400
Total RAM Bits	-
Number of I/O	120
Number of Gates	30000
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TC)
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/at6010a-2au">https://www.e-xfl.com/product-detail/microchip-technology/at6010a-2au</a>

Devices range in size from 4,000 to 30,000 usable gates, and 1024 to 6400 registers. Pin locations are consistent throughout the AT6000 Series for easy design migration. High-I/O versions are available for the lower gate count devices.

AT6000 Series FPGAs utilize a reliable 0.6  $\mu\text{m}$  single-poly, double-metal CMOS process and are 100% factory-tested.

Atmel's PC- and workstation-based Integrated Development System is used to create AT6000 Series designs. Multiple design entry methods are supported.

The Atmel architecture was developed to provide the highest levels of performance, functional density and design flexibility in an FPGA. The cells in the Atmel array are small, very efficient and contain the most important and most commonly used logic and wiring functions. The cell's small size leads to arrays with large numbers of cells, greatly multiplying the functionality in each cell. A simple, high-speed busing network provides fast, efficient communication over medium and long distances.

## The Symmetrical Array

At the heart of the Atmel architecture is a symmetrical array of identical cells (Figure 1). The array is continuous and completely uninterrupted from one edge to the other, except for bus *repeaters* spaced every eight cells (Figure 2).

In addition to logic and storage, cells can also be used as wires to connect functions together over short distances and are useful for routing in tight spaces.

## The Busing Network

There are two kinds of buses: local and express (see Figures 2 and 3).

Local buses are the link between the array of cells and the busing network. There are two local buses – North-South 1 and 2 (NS1 and NS2) – for every column of cells, and two local buses – East-West 1 and 2 (EW1 and EW2) – for every row of cells. In a sector (an 8 x 8 array of cells enclosed by repeaters) each local bus is connected to every cell in its column or row, thus providing every cell in the array with read/write access to two North-South and two East-West buses.

**Figure 1.** Symmetrical Array Surrounded by I/O



**Figure 2. Busing Network (one sector)**



**Figure 3. Cell-to-cell and Bus-to-bus Connections**



Each cell, in addition, provides the ability to route a signal on a 90° turn between the NS1 bus and EW1 bus and between the NS2 bus and EW2 bus.

Express buses are not connected directly to cells, and thus provide higher speeds. They are the fastest way to cover long, straight-line distances within the array.

Each express bus is paired with a local bus, so there are two express buses for every column and two express buses for every row of cells.

Connective units, called repeaters, spaced every eight cells, divide each bus, both local and express, into segments spanning eight cells. Repeaters are aligned in rows and columns thereby partitioning the array into 8 x 8 sectors of cells. Each repeater is associated with a local/express pair, and on each side of the repeater are connections to a local-bus segment and an express-bus segment. The repeater can be programmed to provide any one of twenty-one connecting functions. These functions are symmetric with respect to both the two repeater sides and the two types of buses.

Among the functions provided are the ability to:

- Isolate bus segments from one another
- Connect two local-bus segments
- Connect two express-bus segments
- Implement a local/express transfer

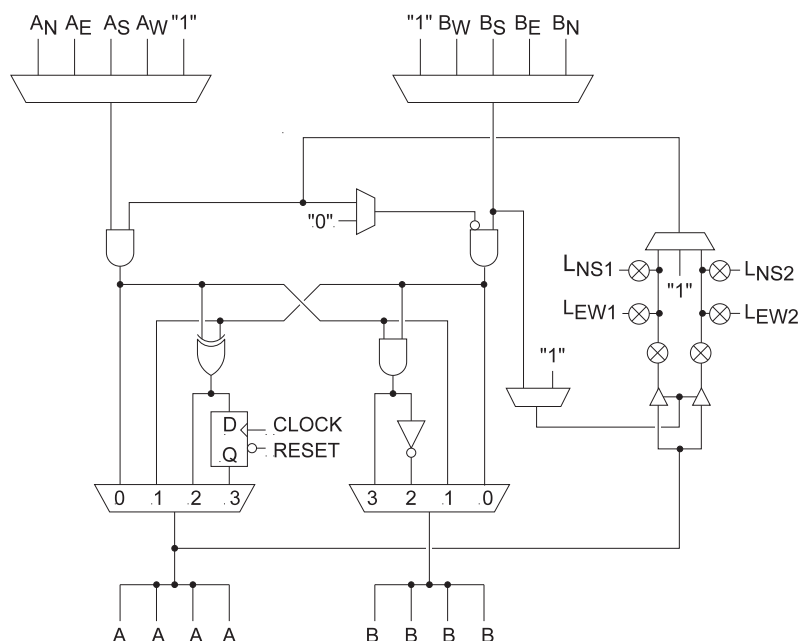
In all of these cases, each connection provides signal regeneration and is thus unidirectional. For bidirectional connections, the basic repeater function for the NS2 and EW2 repeaters is augmented with a special programmable connection allowing bidirectional communication between local-bus segments. This option is primarily used to implement long, tristate buses.

## The Cell Structure

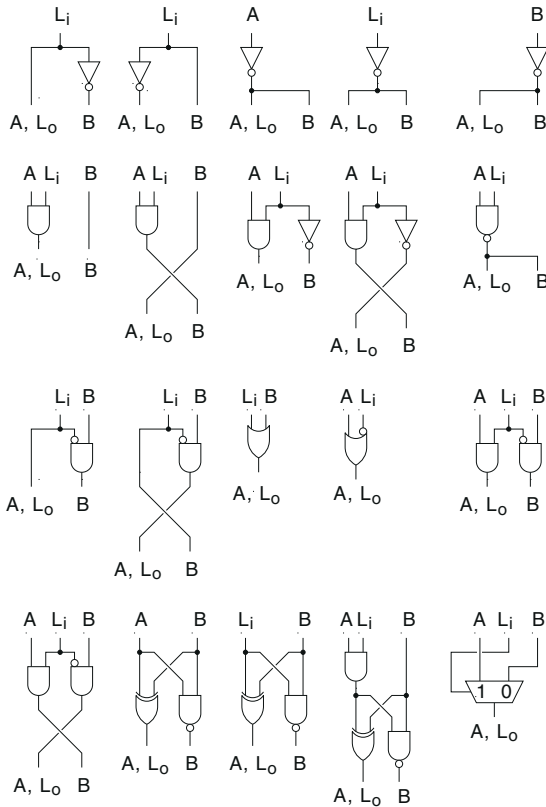
The Atmel cell (Figure 4) is simple and small and yet can be programmed to perform all the logic and wiring functions needed to implement any digital circuit. Its four sides are functionally identical, so each cell is completely symmetrical.

Read/write access to the four local buses – NS1, EW1, NS2 and EW2 – is controlled, in part, by four bidirectional pass gates connected directly to the buses. To read a local bus, the pass gate for that bus is turned on and the three-input multiplexer is set accordingly. To write to a local bus, the pass gate for that bus and the pass gate for the associated tristate driver are both turned on. The two-input multiplexer supplying the control signal to the drivers permits either: (1) active drive, or (2) dynamic tristating controlled by the B input. Turning between  $L_{NS1}$  and  $L_{EW1}$  or between  $L_{NS2}$  and  $L_{EW2}$  is accomplished by turning on the two associated pass gates. The operations of reading, writing and turning are subject to the restriction that each bus can be involved in no more than a **single** operation.

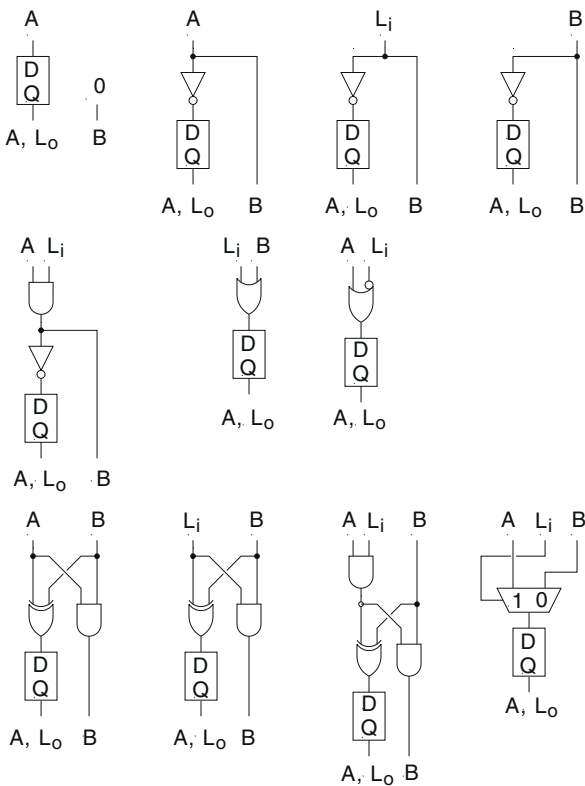
Figure 4. Cell Structure



**Figure 5. Combinatorial Physical States**



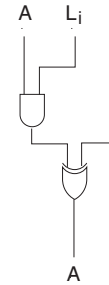
**Figure 6. Register States**



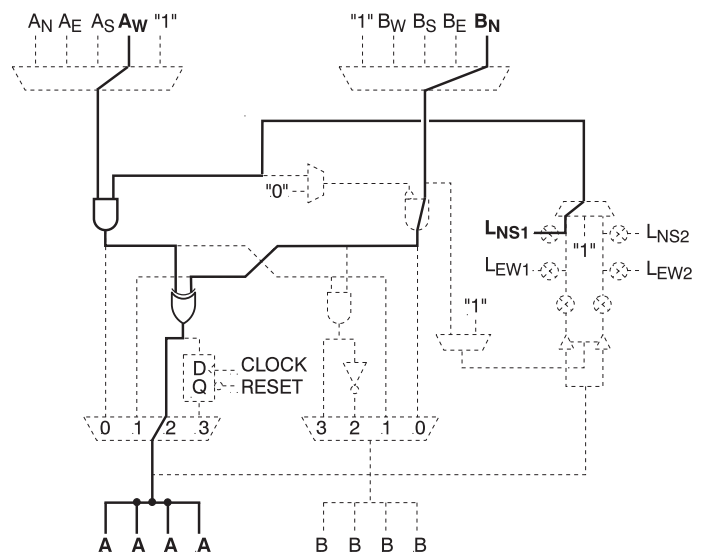
**Figure 7. Physical Constants**

0	0	0	1	1	0	1	1
A, L <sub>0</sub>	B	A, L <sub>0</sub>	B	A, L <sub>0</sub>	B	A, L <sub>0</sub>	B

**Figure 8. Two-input AND Feeding XOR**



**Figure 9. Cell Configuration (A•L) XOR B**



The devices can be partially reconfigured while in operation. Portions of the device not being modified remain operational during reconfiguration. Simultaneous configuration of more than one device is also possible. Full configuration takes as little as a millisecond, partial configuration is even faster.

Refer to the Pin Function Description section following for a brief summary of the pins used in configuration. For more information about configuration, refer to the AT6000 Series Configuration data sheet.

## Pin Function Description

This section provides abbreviated descriptions of the various AT6000 Series pins. For more complete descriptions, refer to the AT6000 Series Configuration data sheet.

Pinout tables for the AT6000 series of devices follow.

### Power Pins

#### $V_{CC}$ , $V_{DD}$ , GND, $V_{SS}$

$V_{CC}$  and GND are the I/O supply pins,  $V_{DD}$  and  $V_{SS}$  are the internal logic supply pins.  $V_{CC}$  and  $V_{DD}$  should be tied to the same trace on the printed circuit board. GND and  $V_{SS}$  should be tied to the same trace on the printed circuit board.

### Input/Output Pins

All I/O pins can be used in the same way (refer to the I/O section of the architecture description). Some I/O pins are dual-function pins used during configuration of the array. When not being used for configuration, dual-function I/Os are fully functional as normal I/O pins. On initial power-up, all I/Os are configured as TTL inputs with a pull-up.

### Dedicated Timing and Control Pins

#### $\overline{CON}$

Configuration-in-process pin. After power-up,  $\overline{CON}$  stays low until power-up initialization is complete, at which time  $\overline{CON}$  is then released.  $\overline{CON}$  is an open collector signal. After power-up initialization, forcing  $\overline{CON}$  low begins the configuration process.

#### $\overline{CS}$

Configuration enable pin. All configuration pins are ignored if  $\overline{CS}$  is high.  $\overline{CS}$  must be held low throughout the configuration process.  $\overline{CS}$  is a TTL input pin.

#### M0, M1, M2

Configuration mode pins are used to determine the configuration mode. All three are TTL input pins.

#### CCLK

Configuration clock pin. CCLK is a TTL input or a CMOS output depending on the mode of operation. In modes 1, 2, 3, and 6 it is an input. In modes 4 and 5 it is an output with a typical frequency of 1 MHz. In all modes, the rising edge of the CCLK signal is used to sample inputs and change outputs.

#### CLOCK

External logic source used to drive the internal global clock line. Registers toggle on the rising edge of CLOCK. The CLOCK signal is neither used nor affected by the configuration modes. It is always a TTL input.

#### $\overline{RESET}$

Array register asynchronous reset.  $\overline{RESET}$  drives the internal global reset. The  $\overline{RESET}$  signal is neither used nor affected by the configuration modes. It is always a TTL input.

#### Dual-function Pins

When  $\overline{CON}$  is high, dual-function I/O pins act as device I/Os; when  $\overline{CON}$  is low, dual-function pins are used as configuration control or data signals as determined by the configuration modes. Care must be taken when using these pins to ensure that configuration activity does not interfere with other circuitry connected to these pins in the application.

#### D0 or I/O

Serial configuration modes use D0 as the serial data input pin. Parallel configuration modes use D0 as the least-significant bit. Input data must meet setup and hold requirements with respect to the rising edge of CCLK. D0 is a TTL input during configuration.

#### D1 to D7 or I/O


Parallel configuration modes use these pins as inputs. Serial configuration modes do not use them. Data must meet setup and hold requirements with respect to the rising edge of CCLK. D1 - D7 are TTL inputs during configuration.

#### A0 to A16 or I/O

During configuration in modes 1, 2 and 5, these pins are CMOS outputs and act as the address pins for a parallel EPROM. A0 - A16 eliminates the need for an external address counter when using an external parallel nonvolatile

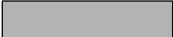
## Pinout Assignment

Left Side (Top to Bottom)										
AT6002 <sup>(3)</sup>	AT6003 <sup>(3)</sup>	AT6005	AT6010	84 <sup>(3)</sup> PLCC	100 VQFP	132 <sup>(3)</sup> PQFP	144 TQFP	180 <sup>(3)</sup> CPGA	208 <sup>(3)</sup> PQFP	240 <sup>(3)</sup> PQFP
-	-	-	I/O51(A)	-	-	-	-	B1	1	1
I/O24(A) or A7	I/O30(A) or A7	I/O27(A) or A7	I/O50(A) or A7	12	1	18	1	C1	2	2
-	I/O29(B)	-	I/O49(A)	-	-	-	2	D1	3	3
-	-	-	I/O48(B)	-	-	-	-	-	-	4
-	-	-	VCC	-	-	-	-	PWR <sup>(1)</sup>	4	5
-	-	-	I/O47(A)	-	-	-	-	E1	5	6
-	-	-	GND	-	-	-	-	GND <sup>(2)</sup>	6	7
-	I/O28(A)	I/O26(A)	I/O46(A)	-	-	19	3	G1	7	8
I/O23(A) or A6	I/O27(A) or A6	I/O25(A) or A6	I/O45(A) or A6	13	2	20	4	H1	8	9
-	-	-	I/O44(B)	-	-	-	-	-	-	10
-	-	-	I/O43(A)	-	-	-	-	C2	9	11
I/O22(B)	I/O26(A)	I/O24(A)	I/O42(A)	-	-	21	5	D2	10	12
I/O21(A) or A5	I/O25(A) or A5	I/O23(A) or A5	I/O41(A) or A5	14	3	22	6	E2	11	13
-	-	-	I/O40(B)	-	-	-	-	-	-	14
-	-	-	I/O39(A)	-	-	-	-	F2	12	15
I/O20(B)	I/O24(B)	I/O22(A)	I/O38(A)	-	4	23	7	G2	13	16
I/O19(A) or A4	I/O23(A) or A4	I/O21(A) or A4	I/O37(A) or A4	15	5	24	8	H2	14	17
-	-	-	I/O36(B)	-	-	-	-	-	-	18
I/O18(B)	I/O22(B)	I/O20(A)	I/O35(A)	-	-	25	9	D3	15	19
I/O17(A) or A3	I/O21(A) or A3	I/O19(A) or A3	I/O34(A) or A3	16	6	26	10	E3	16	20
I/O16(B)	I/O20(B)	I/O18(A)	I/O33(A)	-	7	27	11	F3	17	21
-	-	-	I/O32(B)	-	-	-	-	-	18	22
I/O15(A) or A2	I/O19(A) or A2	I/O17(A) or A2	I/O31(A) or A2	17	8	28	12	G3	19	23
-	I/O18(B)	I/O16(A)	I/O30(A)	-	-	29	13	H3	20	24
GND	GND	GND	GND	18	9	30	14	GND <sup>(2)</sup>	21	25
VSS	VSS	VSS	VSS	19	10	31	15	GND <sup>(2)</sup>	22	26
I/O14(A) or A1	I/O17(A) or A1	I/O15(A) or A1	I/O29(A) or A1	20	11	32	16	F4	23	27
-	-	-	I/O28(B)	-	-	-	-	-	24	28
-	I/O16(B)	-	I/O27(A)	-	-	-	17	G4	25	29
I/O13(A) or A0	I/O15(A) or A0	I/O14(A) or A0	I/O26(A) or A0	21	12	33	18	H4	26	30
I/O12(B) or D7	I/O14(A) or D7	I/O13(A) or D7	I/O25(B) or D7	22	13	34	19	H5	27	31
-	-	-	I/O24(B)	-	-	-	-	-	28	32
I/O11(A) or D6	I/O13(A) or D6	I/O12(A) or D6	I/O23(A) or D6	23	14	35	20	J4	29	33

- Notes:
1. PWR = Pins connected to power plane = F1, E4/E5, L2, R4, K15, L12, E14, A12.
  2. GND = Pins connected to ground plane = L4, M4, N9, N10, E12, D12, C7, C6.
  3.  Obsolete. Not recommended for new design.

## Pinout Assignment (Continued)

Left Side (Top to Bottom)										
AT6002 <sup>(3)</sup>	AT6003 <sup>(3)</sup>	AT6005	AT6010	84 <sup>(3)</sup> PLCC	100 VQFP	132 <sup>(3)</sup> PQFP	144 TQFP	180 <sup>(3)</sup> CPGA	208 <sup>(3)</sup> PQFP	240 <sup>(3)</sup> PQFP
I/O10(A) or D5	I/O12(A) or D5	I/O11(A) or D5	I/O22(A) or D5	24	15	36	21	K4	30	34
VDD	VDD	VDD	VDD	25	16	37	22	PWR <sup>(1)</sup>	31	35
VCC	VCC	VCC	VCC	26	17	38	23	PWR <sup>(1)</sup>	32	36
I/O9(B)	I/O11(B)	I/O10(A)	I/O21(A)	-	-	39	24	J3	33	37
-	-	-	I/O20(B)	-	-	-	-	-	34	38
I/O8(A) or D4	I/O10(A) or D4	I/O9(A) or D4	I/O19(A) or D4	27	18	40	25	K3	35	39
I/O7(B)	I/O9(B)	I/O8(A)	I/O18(A)	-	19	41	26	L3	36	40
-	-	-	I/O17(A)	-	-	-	-	M3	37	41
-	-	-	I/O16(B)	-	-	-	-	-	-	42
I/O6(A) or D3	I/O8(A) or D3	I/O7(A) or D3	I/O15(A) or D3	28	20	42	27	N3	38	43
-	I/O7(B)	I/O6(A)	I/O14(A)	-	-	43	28	J2	39	44
-	-	-	I/O13(A)	-	-	-	-	K2	40	45
GND	GND	GND	GND	-	-	44	29	GND <sup>(2)</sup>	41	46
-	-	-	VSS	-	-	-	-	GND <sup>(2)</sup>	42	47
-	-	-	I/O12(B)	-	-	-	-	-	-	48
I/O5(A) or D2	I/O6(A) or D2	I/O5(A) or D2	I/O11(A) or D2	29	21	45	30	M2	43	49
I/O4(B)	I/O5(B)	I/O4(A)	I/O10(A)	-	22	46	31	N2	44	50
-	-	-	I/O9(A)	-	-	-	-	P2	45	51
-	-	-	I/O8(B)	-	-	-	-	-	-	52
I/O3(A) or D1	I/O4(A) or D1	I/O3(A) or D1	I/O7(A) or D1	30	23	47	32	J1	46	53
I/O2(B)	I/O3(A)	I/O2(A)	I/O6(A)	-	-	48	33	K1	47	54
-	-	-	I/O5(A)	-	-	-	-	L1	48	55
-	-	-	I/O4(B)	-	-	-	-	-	-	56
-	I/O2(B)	-	I/O3(A)	-	-	-	34	M1	49	57
I/O1(A) or D0	I/O1(A) or D0	I/O1(A) or D0	I/O2(A) or D0	31	24	49	35	N1	50	58
-	-	-	I/O1(A)	-	-	-	-	P1	51	59
CCLK	CCLK	CCLK	CCLK	32	25	50	36	R1	52	60

- Notes:
1. PWR = Pins connected to power plane = F1, E4/E5, L2, R4, K15, L12, E14, A12.
  2. GND = Pins connected to ground plane = L4, M4, N9, N10, E12, D12, C7, C6.
  3.  Obsolete. Not recommended for new design.




## Pinout Assignment

Bottom Side (Left to Right)										
AT6002 <sup>(3)</sup>	AT6003 <sup>(3)</sup>	AT6005	AT6010	84 <sup>(3)</sup> PLCC	100 VQFP	132 <sup>(3)</sup> PQFP	144 TQFP	180 <sup>(3)</sup> CPGA	208 <sup>(3)</sup> PQFP	240 <sup>(3)</sup> PQFP
CON	CON	CON	CON	33	26	51	37	M5	53	61
-	-	-	I/O204(A)	-	-	-	-	M6	54	62
I/O96(A)	I/O120(A)	I/O108(A)	I/O203(A)	34	27	52	38	M7	55	63
-	I/O119(B)	-	I/O202(A)	-	-	-	39	R2	56	64
-	-	-	I/O201(B)	-	-	-	-	-	-	65
-	-	-	VCC	-	-	-	-	PWR <sup>(1)</sup>	57	66
-	-	-	I/O200(A)	-	-	-	-	R3	58	67
-	-	-	GND	-	-	-	-	GND <sup>(2)</sup>	59	68
-	I/O118(A)	I/O107(A)	I/O199(A)	-	-	53	40	R5	60	69
I/O95(A) or CSOUT	I/O117(A) or CSOUT	I/O106(A) or CSOUT	I/O198(A) or CSOUT	35	28	54	41	R6	61	70
-	-	-	I/O197(B)	-	-	-	-	-	-	71
-	-	-	I/O196(A)	-	-	-	-	R7	62	72
I/O94(B)	I/O116(A)	I/O105(A)	I/O195(A)	-	-	55	42	P3	63	73
I/O93(A)	I/O115(A)	I/O104(A)	I/O194(A)	36	29	56	43	P4	64	74
-	-	-	I/O193(B)	-	-	-	-	-	-	75
-	-	-	I/O192(A)	-	-	-	-	P5	65	76
I/O92(B)	I/O114(B)	I/O103(A)	I/O191(A)	-	30	57	44	P6	66	77
I/O91(A) or CHECK	I/O113(A) or CHECK	I/O102(A) or CHECK	I/O190(A) or CHECK	37	31	58	45	P7	67	78
-	-	-	I/O189(B)	-	-	-	-	-	-	79
I/O90(B)	I/O112(B)	I/O101(A)	I/O188(A)	-	-	59	46	N4	68	80
I/O89(A) or ERR	I/O111(A) or ERR	I/O100(A) or ERR	I/O187(A) or ERR	38	32	60	47	N5	69	81
I/O88(B)	I/O110(B)	I/O99(A)	I/O186(A)	-	33	61	48	N6	70	82
-	-	-	I/O185(B)	-	-	-	-	-	71	83
I/O87(A)	I/O109(A)	I/O98(A)	I/O184(A)	39	34	62	49	N7	72	84
-	I/O108(B)	I/O97(A)	I/O183(A)	-	-	63	50	M8	73	85
GND	GND	GND	GND	40	35	64	51	GND <sup>(2)</sup>	74	86
I/O86(A)	I/O107(A)	I/O96(A)	I/O182(A)	41	36	65	52	M9	75	87
-	-	-	I/O181(B)	-	-	-	-	-	76	88
-	I/O106(B)	-	I/O180(A)	-	-	-	53	M10	77	89
I/O85(A)	I/O105(A)	I/O95(A)	I/O179(A)	42	37	66	54	M11	78	90
CS	CS	CS	CS	43	38	67	55	L8	79	91
I/O84(B)	I/O104(A)	I/O94(A)	I/O178(A)	44	39	68	56	M12	80	92

Notes: 1. PWR = Pins connected to power plane = F1, E4/E5, L2, R4, K15, L12, E14, A12.

2. GND = Pins connected to ground plane = L4, M4, N9, N10, E12, D12, C7, C6.

3.  Obsolete. Not recommended for new design.

## Pinout Assignment


Right Side (Bottom to Top)										
AT6002 <sup>(5)</sup>	AT6003 <sup>(5)</sup>	AT6005	AT6010	84 <sup>(5)</sup> PLCC	100 VQFP	132 <sup>(5)</sup> PQFP	144 TQFP	180 <sup>(5)</sup> CPGA	208 <sup>(5)</sup> PQFP	240 <sup>(5)</sup> PQFP
-	-	-	I/O153(A)	-	-	-	-	P15	105	121
I/O72(A)	I/O90(A)	I/O81(A)	I/O152(A)	54	51	84	73	N15	106	122
-	I/O89(B)	I/O80(A)	I/O151(A)	-	-	85 <sup>(3)</sup>	74	M15	107	123
-	-	-	I/O150(B)	-	-	-	-	-	-	124
-	-	-	VCC	-	-	-	-	PWR <sup>(1)</sup>	108	125
-	-	-	I/O149(A)	-	-	-	-	L15	109	126
-	-	-	GND	-	-	-	-	GND <sup>(2)</sup>	110	127
-	I/O88(A)	-	I/O148(A)	-	-	85 <sup>(4)</sup>	75	J15	111	128
I/O71(A)	I/O87(A)	I/O79(A)	I/O147(A)	55	52	86	76	H15	112	129
-	-	-	I/O146(B)	-	-	-	-	-	-	130
-	-	-	I/O145(A)	-	-	-	-	N14	113	131
I/O70(B)	I/O86(A)	I/O78(A)	I/O144(A)	-	-	87	77	M14	114	132
I/O69(A)	I/O85(A)	I/O77(A)	I/O143(A)	56	53	88	78	L14	115	133
-	-	-	I/O142(B)	-	-	-	-	-	-	134
-	-	-	I/O141(A)	-	-	-	-	K14	116	135
I/O68(B)	I/O84(B)	I/O76(A)	I/O140(A)	-	54	89	79	J14	117	136
I/O67(A)	I/O83(A)	I/O75(A)	I/O139(A)	57	55	90	80	H14	118	137
-	-	-	I/O138B	-	-	-	-	-	-	138
I/O66(B)	I/O82(B)	I/O74(A)	I/O137(A)	-	-	91	81	M13	119	139
I/O65(A)	I/O81(A)	I/O73(A)	I/O136(A)	58	56	92	82	L13	120	140
I/O64(B)	I/O80(B)	I/O72(A)	I/O135(A)	-	57	93	83	K13	121	141
-	-	-	I/O134(B)	-	-	-	-	-	122	142
I/O63(A)	I/O79(A)	I/O71(A)	I/O133(A)	59	58	94	84	J13	123	143
-	I/O78(B)	I/O70(A)	I/O132(A)	-	-	95	85	H13	124	144
GND	GND	GND	GND	60	59	96	86	GND <sup>(2)</sup>	125	145
VSS	VSS	VSS	VSS	61	60	97	87	GND <sup>(2)</sup>	126	146
I/O62(A)	I/O77(A)	I/O69(A)	I/O131(A)	62	61	98	88	K12	127	147
-	-	-	I/O130(B)	-	-	-	-	-	128	148
-	I/O76(B)	-	I/O129(A)	-	-	-	89	J12	129	149
I/O61(A)	I/O75(A)	I/O68(A)	I/O128(A)	63	62	99	90	H12	130	150
I/O60(B)	I/O74(A)	I/O67(A)	I/O127(A)	64	63	100	91	H11	131	151
-	-	-	I/O126(B)	-	-	-	-	-	132	152

Notes: 1. PWR = Pins connected to power plane = F1, E4/E5, L2, R4, K15, L12, E14, A12.

2. GND = Pins connected to ground plane = L4, M4, N9, N10, E12, D12, C7, C6.

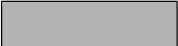
3. 85 = Pin 85 on AT6005.

4. 85 = Pin 85 on AT6003 and AT6010.

5.  Obsolete. Not recommended for new design.

## Pinout Assignment (Continued)

Right Side (Bottom to Top)										
AT6002 <sup>(5)</sup>	AT6003 <sup>(5)</sup>	AT6005	AT6010	84 <sup>(5)</sup> PLCC	100 VQFP	132 <sup>(5)</sup> PQFP	144 TQFP	180 <sup>(5)</sup> CPGA	208 <sup>(5)</sup> PQFP	240 <sup>(5)</sup> PQFP
I/O59(A)	I/O73(A)	I/O66(A)	I/O125(A)	65	64	101	92	G12	133	153
I/O58(A)	I/O72(A)	I/O65(A)	I/O124(A)	66	65	102	93	F12	134	154
VDD	VDD	VDD	VDD	67	66	103	94	PWR <sup>(1)</sup>	135	155
VCC	VCC	VCC	VCC	68	67	104	95	PWR <sup>(1)</sup>	136	156
I/O57(B)	I/O71(B)	I/O64(A)	I/O123(A)	-	-	105	96	G13	137	157
-	-	-	I/O122(B)	-	-	-	-	-	138	158
I/O56(A)	I/O70(A)	I/O63(A)	I/O121(A)	69	68	106	97	F13	139	159
I/O55(B)	I/O69(B)	I/O62(A)	I/O120(A)	-	69	107	98	E13	140	160
-	-	-	I/O119(A)	-	-	-	-	D13	141	161
-	-	-	I/O118(B)	-	-	-	-	-	-	162
I/O54(A)	I/O68(A)	I/O61(A)	I/O117(A)	70	70	108	99	C13	142	163
-	I/O67(B)	I/O60(A)	I/O116(A)	-	-	109	100	G14	143	164
-	-	-	I/O115(A)	-	-	-	-	F14	144	165
GND	GND	GND	GND	-	-	110	101	GND <sup>(2)</sup>	145	166
-	-	-	VSS	-	-	-	-	GND <sup>(2)</sup>	146	167
-	-	-	I/O114(B)	-	-	-	-	-	-	168
I/O53(A)	I/O66(A)	I/O59(A)	I/O113(A)	71	71	111	102	D14	147	169
I/O52(B)	I/O65(B)	I/O58(A)	I/O112(A)	-	72	112	103	C14	148	170
-	-	-	I/O111(A)	-	-	-	-	B14	149	171
-	-	-	I/O110(B)	-	-	-	-	-	-	172
I/O51(A)	I/O64(A)	I/O57(A)	I/O109(A)	72	73	113	104	G15	150	173
I/O50(B)	I/O63(A)	I/O56(A)	I/O108(A)	-	-	114	105	F15	151	174
-	-	-	I/O107(A)	-	-	-	-	E15	152	175
-	-	-	I/O106(B)	-	-	-	-	-	-	176
-	I/O62(B)	-	I/O105(A)	-	-	-	106	D15	153	177
I/O49(A)	I/O61(A)	I/O55(A)	I/O104(A)	73	74	115	107	C15	154	178'
-	-	-	I/O103(A)	-	-	-	-	B15	155	179
M2	M2	M2	M2	74	75	116	108	A15	156	180

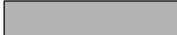
- Notes:
1. PWR = Pins connected to power plane = F1, E4/E5, L2, R4, K15, L12, E14, A12.
  2. GND = Pins connected to ground plane = L4, M4, N9, N10, E12, D12, C7, C6.
  3. 85 = Pin 85 on AT6005.
  4. 85 = Pin 85 on AT6003 and AT6010.
  5.  Obsolete. Not recommended for new design.

## Pinout Assignment

Top Side (Right to Left)										
AT6002 <sup>(3)</sup>	AT6003 <sup>(3)</sup>	AT6005	AT6010	84 <sup>(3)</sup> PLCC	100 VQFP	132 <sup>(3)</sup> PQFP	144 TQFP	180 <sup>(3)</sup> CPGA	208 <sup>(3)</sup> PQFP	240 <sup>(3)</sup> PQFP
M1	M1	M1	M1	75	76	117	109	D11	157	181
-	-	-	I/O102(A)	-	-	-	-	D10	158	182
I/O48(A)	I/O60(A)	I/O54(A)	I/O101(A)	76	77	118	110	D9	159	183
-	I/O59(B)	-	I/O100(A)	-	-	-	111	A14	160	184
-	-	-	I/O99(B)	-	-	-	-	-	-	185
-	-	-	VCC	-	-	-	-	PWR <sup>(1)</sup>	161	186
-	-	-	I/O98(A)	-	-	-	-	A13	162	187
-	-	-	GND	-	-	-	-	GND <sup>(2)</sup>	163	188
-	I/O58(A)	I/O53(A)	I/O97(A)	-	-	119	112	A11	164	189
I/O47(A)	I/O57(A)	I/O52(A)	I/O96(A)	77	78	120	113	A10	165	190
-	-	-	I/O95(B)	-	-	-	-	-	-	191
-	-	-	I/O94(A)	-	-	-	-	A9	166	192
I/O46(B)	I/O56(A)	I/O51(A)	I/O93(A)	-	-	121	114	B13	167	193
I/O45(A)	I/O55(A)	I/O50(A)	I/O92(A)	78	79	122	115	B12	168	194
-	-	-	I/O91(B)	-	-	-	-	-	-	195
-	-	-	I/O90(A)	-	-	-	-	B11	169	196
I/O44(B)	I/O54(B)	I/O49(A)	I/O89(A)	-	80	123	116	B10	170	197
I/O43(A)	I/O53(A)	I/O48(A)	I/O88(A)	79	81	124	117	B9	171	198
-	-	-	I/O87(B)	-	-	-	-	-	-	199
I/O42(B)	I/O52(B)	I/O47(A)	I/O86(A)	-	-	125	118	C12	172	200
I/O41(A)	I/O51(A)	I/O46(A)	I/O85(A)	80	82	126	119	C11	173	201
I/O40(B)	I/O50(B)	I/O45(A)	I/O84(A)	-	83	127	120	C10	174	202
-	-	-	I/O83(B)	-	-	-	-	-	175	203
I/O39(A)	I/O49(A)	I/O44(A)	I/O82(A)	81	84	128	121	C9	176	204
-	I/O48(B)	I/O43(A)	I/O81(A)	-	-	129	122	D8	177	205
GND	GND	GND	GND	82	85	130	123	GND <sup>(2)</sup>	178	206
I/O38(A)	I/O47(A)	I/O42(A)	I/O80(A)	83	86	131	124	D7	179	207
-	-	-	I/O79(B)	-	-	-	-	-	180	208
-	I/O46(B)	-	I/O78(A)	-	-	-	125	D6	181	209
I/O37(A) or A16	I/O45(A) or A16	I/O41(A) or A16	I/O77(A) or A16	84	87	132	126	D5	182	210
CLOCK	CLOCK	CLOCK	CLOCK	1	88	1	127	E8	183	211
I/O36(B) or A15	I/O44(B) or A15	I/O40(A) or A15	I/O76(A) or A15	2	89	2	128	D4	184	212

Notes: 1. PWR = Pins connected to power plane = F1, E4/E5, L2, R4, K15, L12, E14, A12.

2. GND = Pins connected to ground plane = L4, M4, N9, N10, E12, D12, C7, C6.

3.  Obsolete. Not recommended for new design.

## AC Timing Characteristics – 5V Operation

Delays are based on fixed load. Loads for each type of device are described in the notes. Delays are in nanoseconds. Worst case:  $V_{CC} = 4.75V$  to  $5.25V$ . Temperature =  $0^{\circ}C$  to  $70^{\circ}C$ .

Cell Function	Parameter	From	To	Load Definition <sup>(7)</sup>	-1	-2	-4	Units
Wire <sup>(4)</sup>	$t_{PD} (max)^{(4)}$	A, B, L	A, B	1	0.8	1.2	1.8	ns
NAND	$t_{PD} (max)$	A, B, L	B	1	1.6	2.2	3.2	ns
XOR	$t_{PD} (max)$	A, B, L	A	1	1.8	2.4	4.0	ns
AND	$t_{PD} (max)$	A, B, L	B	1	1.7	2.2	3.2	ns
MUX	$t_{PD} (max)$	A, B	A	1	1.7	2.3	4.0	ns
		L	A	1	2.1	3.0	4.9	ns
D-Flip-flop <sup>(5)</sup>	$t_{setup} (min)$	A, B, L	CLK	-	1.5	2.0	3.0	ns
D-Flip-flop <sup>(5)</sup>	$t_{hold} (min)$	CLK	A, B, L	-	0	0	0	ns
D-Flip-flop	$t_{PD} (max)$	CLK	A	1	1.5	2.0	3.0	ns
Bus Driver	$t_{PD} (max)$	A	L	2	2.0	2.6	4.0	ns
Repeater	$t_{PD} (max)$	L, E	E	3	1.3	1.6	2.3	ns
		L, E	L	2	1.7	2.1	3.0	ns
Column Clock	$t_{PD} (max)$	GCLK, A, ES	CLK	3	1.8	2.4	3.0	ns
Column Reset	$t_{PD} (max)$	GRES, A, EN	RES	3	1.8	2.4	3.0	ns
Clock Buffer <sup>(5)</sup>	$t_{PD} (max)$	CLOCK PIN	GCLK	-	1.6	2.0	2.9	ns
Reset Buffer <sup>(5)</sup>	$t_{PD} (max)$	RESET PIN	GRES	-	1.5	1.9	2.8	ns
TTL Input <sup>(1)</sup>	$t_{PD} (max)$	I/O	A	3	1.0	1.2	1.5	ns
CMOS Input <sup>(2)</sup>	$t_{PD} (max)$	I/O	A	3	1.3	1.4	2.3	ns
Fast Output <sup>(3)</sup>	$t_{PD} (max)$	A	I/O PIN	4	3.3	3.5	6.0	ns
Slow Output <sup>(3)</sup>	$t_{PD} (max)$	A	I/O PIN	4	7.5	8.0	12.0	ns
Output Disable <sup>(5)</sup>	$t_{PXZ} (max)$	L	I/O PIN	4	3.1	3.3	5.5	ns
Fast Enable <sup>(3)(5)</sup>	$t_{PXZ} (max)$	L	I/O PIN	4	3.8	4.0	6.5	ns
Slow Enable <sup>(3)(5)</sup>	$t_{PXZ} (max)$	L	I/O PIN	4	8.2	8.5	12.5	ns

Device	Cell Types	Outputs	$I_{CC} (max)$
Cell <sup>(6)</sup>	Wire, XWire, Half-adder, Flip-flop	A, B	4.5 $\mu A/MHz$
Bus <sup>(6)</sup>	Wire, XWire, Half-adder, Flip-flop, Repeater	L	2.5 $\mu A/MHz$
Column Clock <sup>(6)</sup>	Column Clock Driver	CLK	40 $\mu A/MHz$

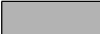
- Notes:
1. TTL buffer delays are measured from a  $V_{IH}$  of 1.5V at the pad to the internal  $V_{IH}$  at A. The input buffer load is constant.
  2. CMOS buffer delays are measured from a  $V_{IH}$  of 1/2  $V_{CC}$  at the pad to the internal  $V_{IH}$  at A. The input buffer load is constant.
  3. Buffer delay is to a pad voltage of 1.5V with one output switching.
  4. Max specifications are the average of  $t_{PDLH}$  and  $t_{PDHL}$ .
  5. Parameter based on characterization and simulation; not tested in production
  6. Exact power calculation is available in an Atmel application note.
  7. Load Definition: 1 = Load of one A or B input; 2 = Load of one L input; 3 = Constant Load; 4 = Tester Load of 50 pF.

## AC Timing Characteristics – 3.3V Operation <sup>(8)</sup>

Delays are based on fixed load. Loads for each type of device are described in the notes. Delays are in nanoseconds. Worst case:  $V_{CC} = 3.0V$  to  $3.6V$ . Temperature =  $0^{\circ}C$  to  $70^{\circ}C$ .

Cell Function	Parameter	From	To	Load Definition <sup>(7)</sup>	-4	Units
Wire <sup>(4)</sup>	$t_{PD} (max)^{(4)}$	A, B, L	A, B	1	1.8	ns
NAND	$t_{PD} (max)$	A, B, L	B	1	3.2	ns
XOR	$t_{PD} (max)$	A, B, L	A	1	4.0	ns
AND	$t_{PD} (max)$	A, B, L	B	1	3.2	ns
MUX	$t_{PD} (max)$	A, B	A	1	4.0	ns
		L	A	1	4.9	ns
D-Flip-flop <sup>(5)</sup>	$t_{setup} (min)$	A, B, L	CLK	-	3.0	ns
D-Flip-flop <sup>(5)</sup>	$t_{hold} (min)$	CLK	A, B, L	-	0	ns
D-Flip-flop	$t_{PD} (max)$	CLK	A	1	3.0	ns
Bus Driver	$t_{PD} (max)$	A	L	2	4.0	ns
Repeater	$t_{PD} (max)$	L, E	E	3	2.3	ns
		L, E	L	2	3.0	ns
Column Clock	$t_{PD} (max)$	GCLK, A, ES	CLK	3	3.0	ns
Column Reset	$t_{PD} (max)$	GRES, A, EN	RES	3	3.0	ns
Clock Buffer <sup>(5)</sup>	$t_{PD} (max)$	CLOCK PIN	GCLK	4	2.9	ns
Reset Buffer <sup>(5)</sup>	$t_{PD} (max)$	RESET PIN	GRES	5	2.8	ns
TTL Input <sup>(1)</sup>	$t_{PD} (max)$	I/O	A	3	1.5	ns
CMOS Input <sup>(2)</sup>	$t_{PD} (max)$	I/O	A	3	2.3	ns
Fast Output <sup>(3)</sup>	$t_{PD} (max)$	A	I/O PIN	6	6.0	ns
Slow Output <sup>(3)</sup>	$t_{PD} (max)$	A	I/O PIN	6	12.0	ns
Output Disable <sup>(5)</sup>	$t_{PXZ} (max)$	L	I/O PIN	6	5.5	ns
Fast Enable <sup>(3)(5)</sup>	$t_{PXZ} (max)$	L	I/O PIN	6	6.5	ns
Slow Enable <sup>(3)(5)</sup>	$t_{PXZ} (max)$	L	I/O PIN	6	12.5	ns

Device	Cell Types	Outputs	$I_{CC} (max)$
Cell <sup>(6)</sup>	Wire, XWire, Half-adder, Flip-flop	A, B	2.3 $\mu A/MHz$
Bus <sup>(6)</sup>	Wire, XWire, Half-adder, Flip-flop, Repeater	L	1.3 $\mu A/MHz$
Column Clock <sup>(6)</sup>	Column Clock Driver	CLK	20 $\mu A/MHz$

- Notes:
1. TTL buffer delays are measured from a  $V_{IH}$  of 1.5V at the pad to the internal  $V_{IH}$  at A. The input buffer load is constant.
  2. CMOS buffer delays are measured from a  $V_{IH}$  of 1/2  $V_{CC}$  at the pad to the internal  $V_{IH}$  at A. The input buffer load is constant.
  3. Buffer delay is to a pad voltage of 1.5V with one output switching.
  4. Max specifications are the average of  $t_{PDLH}$  and  $t_{PDHL}$ .
  5. Parameter based on characterization and simulation; not tested in production
  6. Exact power calculation is available in an Atmel application note.
  7. Load Definition: 1 = Load of one A or B input; 2 = Load of one L input; 3 = Constant Load; 4 = Load of 28 Clock Columns; 5 = Load of 28 Reset Columns; 6 = Tester Load of 50 pF.
  8.  Obsolete. Not recommended for new design.

## Absolute Maximum Ratings\*

Supply Voltage ( $V_{CC}$ )	-0.5V to + 7.0V
DC Input Voltage ( $V_{IN}$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Voltage ( $V_{ON}$ )	-0.5V to $V_{CC} + 0.5V$
Storage Temperature Range (TSTG)	-65°C to +150°C
Power Dissipation (PD)	1500 mW
Lead Temperature ( $T_L$ ) (Soldering, 10 sec.)	260°C
ESD ( $R_{ZAP} = 1.5K$ , $C_{ZAP} = 100$ pF)	2000V

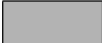
\*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress rating only and functional operation of the device at these or any other conditions beyond those listed under operating conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

## DC and AC Operating Range – 5V Operation

		AT6002-2/4 <sup>(1)</sup> AT6003-2/4 <sup>(1)</sup> AT6005-2/4 <sup>(1)</sup> AT6010-2/4 <sup>(1)</sup> Commercial <sup>(1)</sup>	AT6002-2/4 <sup>(1)</sup> AT6003-2/4 <sup>(1)</sup> AT6005-2/4 <sup>(1)</sup> AT6010-2/4 <sup>(1)</sup> Industrial	AT6002-2/4 <sup>(1)</sup> AT6003-2/4 <sup>(1)</sup> AT6005-2/4 <sup>(1)</sup> AT6010-2/4 <sup>(1)</sup> Military <sup>(1)</sup>
Operating Temperature (Case)		0°C - 70°C	-40°C - 85°C	-55°C - 125°C
$V_{CC}$ Power Supply		5V ± 5%	5V ± 10%	5V ± 10%
Input Voltage Level (TTL)	High ( $V_{IHT}$ )	2.0V - $V_{CC}$	2.0V - $V_{CC}$	2.0V - $V_{CC}$
	Low ( $V_{ILT}$ )	0V - 0.8V	0V - 0.8V	0V - 0.8V
Input Voltage Level (CMOS)	High ( $V_{IHC}$ )	70% - 100% $V_{CC}$	70% - 100% $V_{CC}$	70% - 100% $V_{CC}$
	Low ( $V_{ILC}$ )	0 - 30% $V_{CC}$	0 - 30% $V_{CC}$	0 - 30% $V_{CC}$
Input Signal Transition Time ( $T_{IN}$ )		50 ns (max)	50 ns (max)	50 ns (max)

## DC and AC Operating Range – 3.3V Operation<sup>(1)</sup>

		AT6002-2/4 <sup>(1)</sup> , AT6003-2/4 <sup>(1)</sup> AT6005-2/4 <sup>(1)</sup> , AT6010-2/4 <sup>(1)</sup> Commercial
Operating Temperature (Case)		0°C - 70°C
$V_{CC}$ Power Supply		3.3V ± 5%
Input Voltage Level (TTL)	High ( $V_{IHT}$ )	2.0V - $V_{CC}$
	Low ( $V_{ILT}$ )	0V - 0.8V
Input Voltage Level (CMOS)	High ( $V_{IHC}$ )	70% - 100% $V_{CC}$
	Low ( $V_{ILC}$ )	0 - 30% $V_{CC}$
Input Signal Transition Time ( $T_{IN}$ )		50 ns (max)

Note: 1.  Obsolete. Not recommended for new design.

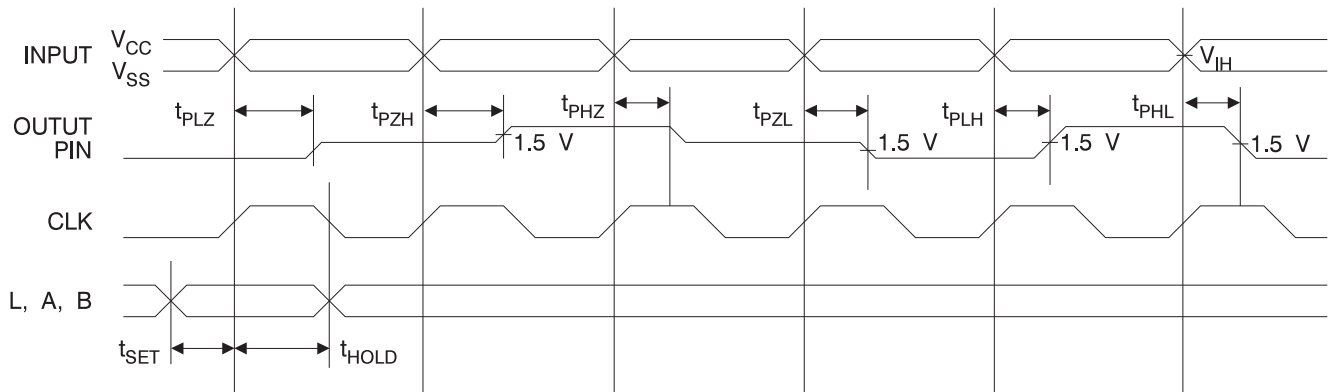
## DC Characteristics – 3.3V Operation<sup>(2)</sup>

Symbol	Parameter	Conditions	Min	Max	Units
$V_{IH}$	High-level Input Voltage	Commercial	CMOS	$70\% V_{CC}$	V
			TTL	2.0	V
$V_{IL}$	Low-level Input Voltage	Commercial	CMOS	0	$30\% V_{CC}$
			TTL	0	0.8
$V_{OH}$	High-level Output Voltage	Commercial	$I_{OH} = -2 \text{ mA}, V_{CC} \text{ min}$	2.4	V
			$I_{OH} = -6 \text{ mA}, V_{CC} \text{ min}$	2.0	V
$V_{OL}$	Low-level Output Voltage	Commercial	$I_{OL} = +2 \text{ mA}, V_{CC} \text{ min}$	0.4	V
			$I_{OL} = +6 \text{ mA}, V_{CC} \text{ min}$	0.5	V
$I_{OZH}$	High-level Tristate	$V_O = V_{CC} \text{ (max)}$		10	$\mu\text{A}$
	Output Leakage Current				
$I_{OZL}$	High-level Tristate	Without Pull-up, $V_O = V_{SS}$	-10		$\mu\text{A}$
	Output Leakage Current	With Pull-up, $V_O = V_{SS}$	-500		$\mu\text{A}$
$I_{IH}$	High-level Input Current	$V_{IN} = V_{CC} \text{ (max)}$		10	$\mu\text{A}$
$I_{IL}$	Low-level Input Current	Without Pull-up, $V_{IN} = V_{SS}$	-10		$\mu\text{A}$
		With Pull-up, $V_{IN} = V_{SS}$	-500		$\mu\text{A}$
$I_{CC}$	Power Consumption	Without Internal Oscillator (Standby)		200	$\mu\text{A}$
$C_{IN}^{(1)}$	Input Capacitance	All Pins		10	pF

Notes: 1. Parameter based on characterization and simulation; it is not tested in production.

2.   Obsolete. Not recommended for new design.


## Device Timing: During Operation





## Ordering Information – AT6002<sup>(1)</sup>


Usable Gates	Speed Grade (ns)	Ordering Code	Package	Operation Range
6,000	2	AT6002-2AC	100A	5V Commercial (0°C to 70°C)
		AT6002A-2AC	144A	
		AT6002-2JC	84J	
		AT6002-2QC	132Q	
		AT6002-2AI	100A	5V Industrial (-40°C to 85°C)
		AT6002A-2AI	144A	
		AT6002-2JI	84J	
		AT6002-2QI	132Q	
6,000	4	AT6002-4AC	100A	5V Commercial (0°C to 70°C)
		AT6002A-4AC	144A	
		AT6002-4JC	84J	
		AT6002-4QC	132Q	
		AT6002LV-4AC	100A	3.3V Commercial (0°C to 70°C)
		AT6002ALV-4AC	144A	
		AT6002LV-4JC	84J	
		AT6002LV-4QC	132Q	
		AT6002-4AI	100A	5V Industrial (-40°C to 85°C)
		AT6002A-4AI	144A	
		AT6002-4JI	84J	
		AT6002-4QI	132Q	

Note: 1.  Obsolete. Not recommended for new design.

Package Type	
<b>84J</b>	84-lead, Plastic J-leaded Chip Carrier (PLCC)
<b>100A</b>	100-lead, Very Thin (1.0 mm) Plastic Gull-Wing Quad Flat Package (VQFP)
<b>132Q</b>	132-lead, Bumped Plastic Gull-Wing Quad Flat Package (BQFP)
<b>144A</b>	144-lead, Thin (1.4 mm) Plastic Gull-Wing Quad Flat Package (TQFP)
<b>208Q</b>	208-lead, Plastic Gull-Wing Quad Flat Package (PQFP)
<b>240Q</b>	240-lead, Plastic Gull-Wing Quad Flat Package (PQFP)

## Ordering Information – AT6005


Usable Gates	Speed Grade (ns)	Ordering Code	Package	Operation Range
15,000	2	AT6005-2AU	100A	5V Industrial Temperature (-40°C to 85°C)
15,000	2	AT6005-2AC	100A	5V Commercial (0°C to 70°C)
		AT6005A-2AC	144A	
		AT6005-2JC	84J	
		AT6005-2QC	132Q	
		AT6005A-2QC	208Q	
		AT6005-2AI	100A	Industrial (-40°C to 85°C)
		AT6005A-2AI	144A	
		AT6005-2JI	84J	
		AT6005-2QI	132Q	
		AT6005A-2QI	208Q	
15,000	4	AT6005-4AC	100A	5V Commercial (0°C to 70°C)
		AT6005A-4AC	144A	
		AT6005-4JC	84J	
		AT6005-4QC	132Q	
		AT6005A-4QC	208Q	
		AT6005LV-4AC	100A	3.3V Commercial (0°C to 70°C)
		AT6005ALV-4AC	144A	
		AT6005LV-4JC	84J	
		AT6005LV-4QC	132Q	
		AT6005ALV-4QC	208Q	
		AT6005-4AI	100A	5V Commercial (-40°C to 85°C)
		AT6005A-4AI	144A	
		AT6005-4JI	84J	
		AT6005-4QI	132Q	
		AT6005A-4QI	208Q	

Note: 1  Obsolete. Package options are not recommended for new design.

Package Type	
<b>84J</b>	84-lead, Plastic J-leaded Chip Carrier (PLCC)
<b>100A</b>	100-lead, Very Thin (1.0 mm) Plastic Gull-Wing Quad Flat Package (VQFP)
<b>132Q</b>	132-lead, Bumped Plastic Gull-Wing Quad Flat Package (BQFP)
<b>144A</b>	144-lead, Thin (1.4 mm) Plastic Gull-Wing Quad Flat Package (TQFP)
<b>208Q</b>	208-lead, Plastic Gull-Wing Quad Flat Package (PQFP)
<b>240Q</b>	240-lead, Plastic Gull-Wing Quad Flat Package (PQFP)

## Ordering Information – AT6010

Usable Gates	Speed Grade (ns)	Ordering Code	Package	Operation Range
30,000	2	AT6010A-2AU	144A	5V Industrial Temperature (-40°C to 85°C)
30,000	2	AT6010-2JC	84J	5V Commercial (0°C to 70°C)
		AT6010A-2AC	144A	
		AT6010-2QC	132Q	
		AT6010A-2QC	208Q	
		AT6010H-2QC	240Q	
		AT6010-2JI	84J	Industrial (-40°C to 85°C)
		AT6010A-2AI	144A	
		AT6010-2QI	132Q	
		AT6010A-2QI	208Q	
		AT6010H-2QI	240Q	
30,000	4	AT6010A-4AC	144A	5V Commercial (0°C to 70°C)
		AT6010-4QC	132Q	
		AT6010-4JC	84J	
		AT6010A-4QC	208Q	
		AT6010H-4QC	240Q	
		AT6010ALV-4AC	144A	3.3V Commercial (0°C to 70°C)
		AT6010LV-4QC	132Q	
		AT6010LV-4JC	84J	
		AT6010ALV-4QC	208Q	
		AT6010HLV-4QC	240Q	
		AT6010A-4AI	144A	5V Industrial (-40°C to 85°C)
		AT6010-4QI	132Q	
		AT6010-4JI	84J	
		AT6010A-4QI	208Q	
		AT6010H-4QI	240Q	

Note: 1  Obsolete. Package options are not recommended for new design.

Package Type	
<b>84J</b>	84-lead, Plastic J-leaded Chip Carrier (PLCC)
<b>100A</b>	100-lead, Very Thin (1.0 mm) Plastic Gull-Wing Quad Flat Package (VQFP)
<b>132Q</b>	132-lead, Bumped Plastic Gull-Wing Quad Flat Package (BQFP)
<b>144A</b>	144-lead, Thin (1.4 mm) Plastic Gull-Wing Quad Flat Package (TQFP)
<b>208Q</b>	208-lead, Plastic Gull-Wing Quad Flat Package (PQFP)
<b>240Q</b>	240-lead, Plastic Gull-Wing Quad Flat Package (PQFP)

## Revision History

Doc. No.	Date	Description
0264G	04/2015	Obsoleted AT6002, AT6003, and all AT6K low voltage (LV) devices and the AT6005 and AT6010A lead based packages. Added lead free packages options for AT6005 and AT6010A devices.
0264F	10/2009	



**Atmel Corporation** 1600 Technology Drive, San Jose, CA 95110 USA T: (+1)(408) 441.0311 F: (+1)(408) 436.4200 | **www.atmel.com**

© 2015 Atmel Corporation. / Rev.: Atmel-0264G-FPGA-AT6000(LV)-Datasheet\_042015.

Atmel®, Atmel logo and combinations thereof, Enabling Unlimited Possibilities, and others are registered trademarks or trademarks of Atmel Corporation in U.S. and other countries. Other terms and product names may be trademarks of others.

**DISCLAIMER:** The information in this document is provided in connection with Atmel products. No license, express or implied, by estoppel or otherwise, to any intellectual property right is granted by this document or in connection with the sale of Atmel products. EXCEPT AS SET FORTH IN THE ATMEL TERMS AND CONDITIONS OF SALES LOCATED ON THE ATMEL WEBSITE, ATMEL ASSUMES NO LIABILITY WHATSOEVER AND DISCLAIMS ANY EXPRESS, IMPLIED OR STATUTORY WARRANTY RELATING TO ITS PRODUCTS INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT. IN NO EVENT SHALL ATMEL BE LIABLE FOR ANY DIRECT, INDIRECT, CONSEQUENTIAL, PUNITIVE, SPECIAL OR INCIDENTAL DAMAGES (INCLUDING, WITHOUT LIMITATION, DAMAGES FOR LOSS AND PROFITS, BUSINESS INTERRUPTION, OR LOSS OF INFORMATION) ARISING OUT OF THE USE OR INABILITY TO USE THIS DOCUMENT, EVEN IF ATMEL HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. Atmel makes no representations or warranties with respect to the accuracy or completeness of the contents of this document and reserves the right to make changes to specifications and products descriptions at any time without notice. Atmel does not make any commitment to update the information contained herein. Unless specifically provided otherwise, Atmel products are not suitable for, and shall not be used in, automotive applications. Atmel products are not intended, authorized, or warranted for use as components in applications intended to support or sustain life.

**SAFETY-CRITICAL, MILITARY, AND AUTOMOTIVE APPLICATIONS DISCLAIMER:** Atmel products are not designed for and will not be used in connection with any applications where the failure of such products would reasonably be expected to result in significant personal injury or death ("Safety-Critical Applications") without an Atmel officer's specific written consent. Safety-Critical Applications include, without limitation, life support devices and systems, equipment or systems for the operation of nuclear facilities and weapons systems. Atmel products are not designed nor intended for use in military or aerospace applications or environments unless specifically designated by Atmel as military-grade. Atmel products are not designed nor intended for use in automotive applications unless specifically designated by Atmel as automotive-grade.