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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	6400
Total RAM Bits	-
Number of I/O	120
Number of Gates	30000
Voltage - Supply	3.135V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at6010alv-4ac

Devices range in size from 4,000 to 30,000 usable gates, and 1024 to 6400 registers. Pin locations are consistent throughout the AT6000 Series for easy design migration. High-I/O versions are available for the lower gate count devices.

AT6000 Series FPGAs utilize a reliable 0.6 µm single-poly, double-metal CMOS process and are 100% factory-tested.

Atmel's PC- and workstation-based Integrated Development System is used to create AT6000 Series designs. Multiple design entry methods are supported.

The Atmel architecture was developed to provide the highest levels of performance, functional density and design flexibility in an FPGA. The cells in the Atmel array are small, very efficient and contain the most important and most commonly used logic and wiring functions. The cell's small size leads to arrays with large numbers of cells, greatly multiplying the functionality in each cell. A simple, high-speed busing network provides fast, efficient communication over medium and long distances.

The Symmetrical Array

At the heart of the Atmel architecture is a symmetrical array of identical cells (Figure 1). The array is continuous and completely uninterrupted from one edge to the other, except for bus *repeaters* spaced every eight cells (Figure 2).

In addition to logic and storage, cells can also be used as wires to connect functions together over short distances and are useful for routing in tight spaces.

The Busing Network

There are two kinds of buses: local and express (see Figures 2 and 3).

Local buses are the link between the array of cells and the busing network. There are two local buses – North-South 1 and 2 (NS1 and NS2) – for every column of cells, and two local buses – East-West 1 and 2 (EW1 and EW2) – for every row of cells. In a sector (an 8 x 8 array of cells enclosed by repeaters) each local bus is connected to every cell in its column or row, thus providing every cell in the array with read/write access to two North-South and two East-West buses.

Figure 1. Symmetrical Array Surrounded by I/O

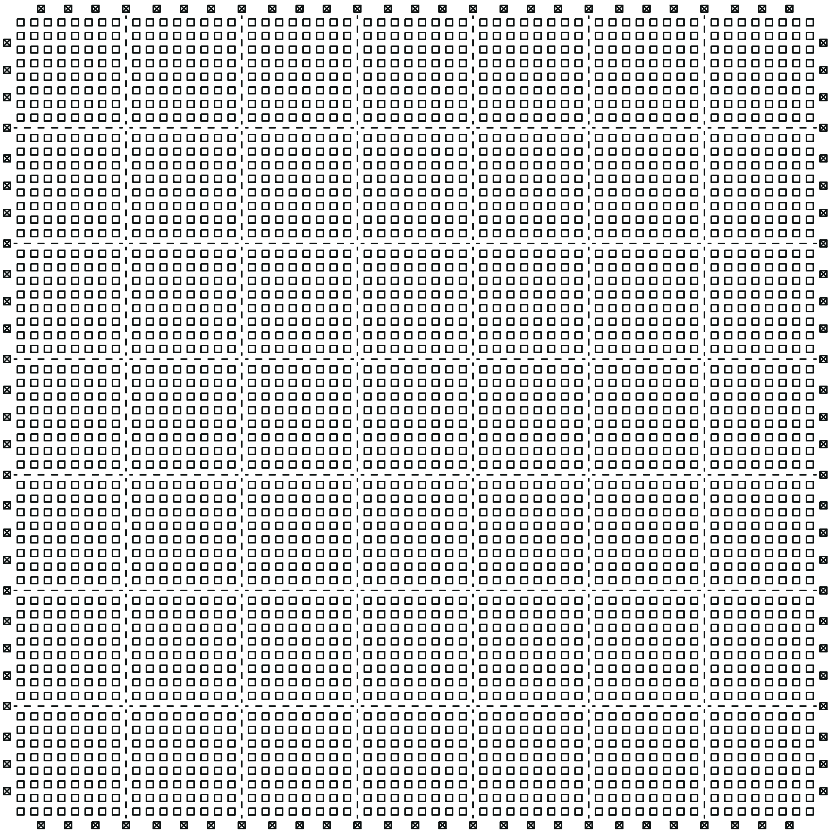


Figure 2. Busing Network (one sector)

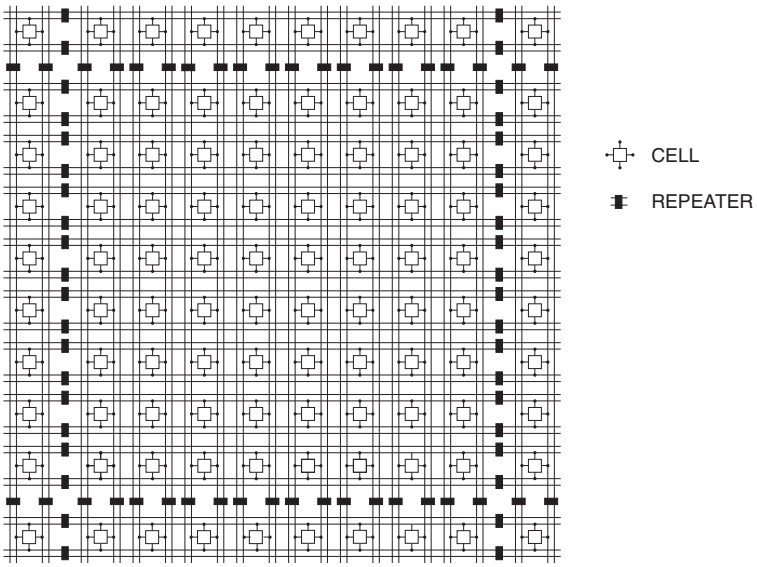
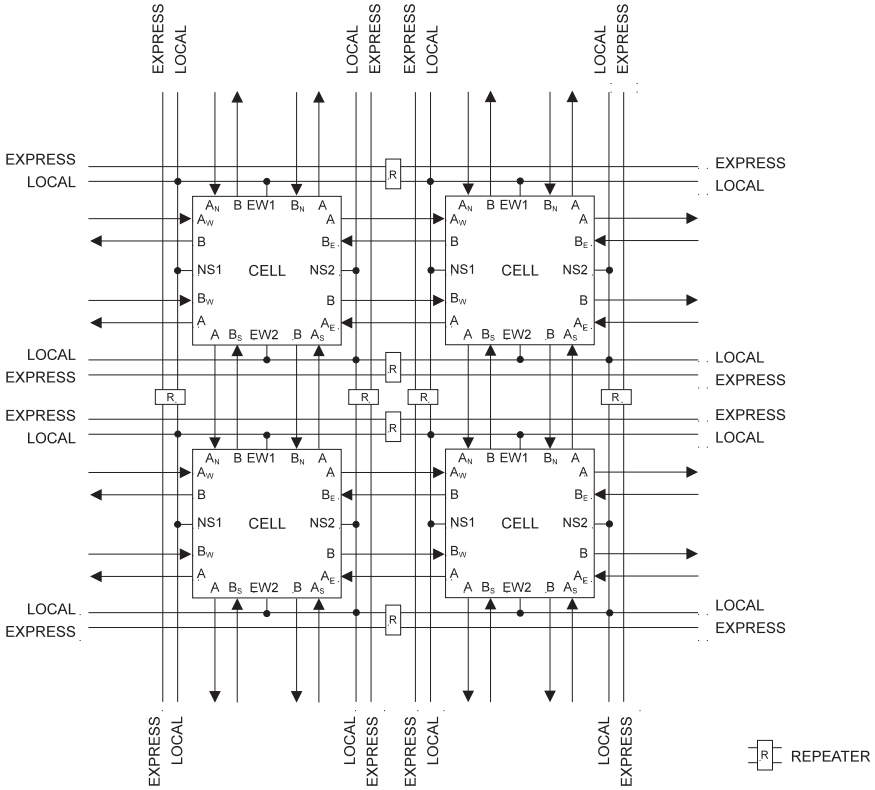


Figure 3. Cell-to-cell and Bus-to-bus Connections



Each cell, in addition, provides the ability to route a signal on a 90° turn between the NS1 bus and EW1 bus and between the NS2 bus and EW2 bus.

Express buses are not connected directly to cells, and thus provide higher speeds. They are the fastest way to cover long, straight-line distances within the array.

Each express bus is paired with a local bus, so there are two express buses for every column and two express buses for every row of cells.

Connective units, called repeaters, spaced every eight cells, divide each bus, both local and express, into segments spanning eight cells. Repeaters are aligned in rows and columns thereby partitioning the array into 8 x 8 sectors of cells. Each repeater is associated with a local/express pair, and on each side of the repeater are connections to a local-bus segment and an express-bus segment. The repeater can be programmed to provide any one of twenty-one connecting functions. These functions are symmetric with respect to both the two repeater sides and the two types of buses.

Among the functions provided are the ability to:

- Isolate bus segments from one another
- Connect two local-bus segments
- Connect two express-bus segments
- Implement a local/express transfer

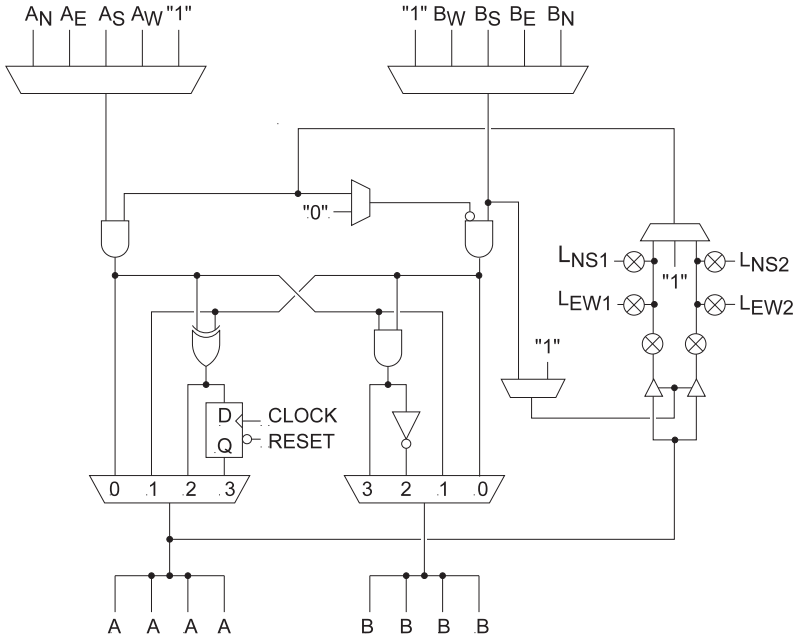
In all of these cases, each connection provides signal regeneration and is thus unidirectional. For bidirectional connections, the basic repeater function for the NS2 and EW2 repeaters is augmented with a special programmable connection allowing bidirectional communication between local-bus segments. This option is primarily used to implement long, tristate buses.

The Cell Structure

The Atmel cell (Figure 4) is simple and small and yet can be programmed to perform all the logic and wiring functions needed to implement any digital circuit. Its four sides are functionally identical, so each cell is completely symmetrical.

Read/write access to the four local buses – NS1, EW1, NS2 and EW2 – is controlled, in part, by four bidirectional pass gates connected directly to the buses. To read a local bus, the pass gate for that bus is turned on and the three-input multiplexer is set accordingly. To write to a local bus, the pass gate for that bus and the pass gate for the associated tristate driver are both turned on. The two-input multiplexer supplying the control signal to the drivers permits either: (1) active drive, or (2) dynamic tristating controlled by the B input. Turning between L_{NS1} and L_{EW1} or between L_{NS2} and L_{EW2} is accomplished by turning on the two associated pass gates. The operations of reading, writing and turning are subject to the restriction that each bus can be involved in no more than a ***single*** operation.

Figure 4. Cell Structure



In addition to the four local-bus connections, a cell receives two inputs and provides two outputs to each of its North (N), South (S), East (E) and West (W) neighbors. These inputs and outputs are divided into two classes: “A” and “B”. There is an A input and a B input from each neighboring cell and an A output and a B output driving all four neighbors. Between cells, an A output is always connected to an A input and a B output to a B input.

Within the cell, the four A inputs and the four B inputs enter two separate, independently configurable multiplexers. Cell flexibility is enhanced by allowing each multiplexer to select also the logical constant “1”. The two multiplexer outputs enter the two upstream AND gates.

Downstream from these two AND gates are an Exclusive-OR (XOR) gate, a register, an AND gate, an inverter and two four-input multiplexers producing the A and B outputs. These multiplexers are controlled in tandem (unlike the A and B input multiplexers) and determine the function of the cell.

- In State 0 – corresponding to the “0” inputs of the multiplexers – the output of the left-hand upstream AND gate is connected to the cell’s A output, and the output of the right-hand upstream AND gate is connected to the cell’s B output.
- In State 1 – corresponding to the “1” inputs of the multiplexers – the output of the left-hand upstream AND gate is connected to the cell’s B output, the output of the right-hand upstream AND gate is connected to the cell’s A output.
- In State 2 – corresponding to the “2” inputs of the multiplexers – the XOR of the outputs from the two upstream AND gates is provided to the cell’s A output, while the NAND of these two outputs is provided to the cell’s B output.
- In State 3 – corresponding to the “3” inputs of the multiplexers – the XOR function of State 2 is provided to the D input of a D-type flip-flop, the Q output of which is connected to the cell’s A output. Clock and asynchronous reset signals are supplied externally as described later. The AND of the outputs from the two upstream AND gates is provided to the cell's B output.

Logic States

The Atmel cell implements a rich and powerful set of logic functions, stemming from 44 logical cell states which permutate into 72 physical states. Some states use both A and B inputs. Other states are created by selecting the “1” input on either or both of the input multiplexers.

There are 28 combinatorial primitives created from the cell’s tristate capabilities and the 20 physical states represented in Figure 5. Five logical primitives are derived from the physical constants shown in Figure 7. More complex functions are created by using cells in combination.

A two-input AND feeding an XOR (Figure 8) is produced using a single cell (Figure 9). A two-to-one multiplexer selects the logical constant “0” and feeds it to the right-hand AND gate. The AND gate acts as a feed-through, letting the B input pass through to the XOR. The three-to-one multiplexer on the right side selects the local-bus input, LNS1, and passes it to the left-hand AND gate. The A and LNS1 signals are the inputs to the AND gate. The output of the AND gate feeds into the XOR, producing the logic state (A●L) XOR B.

Figure 5. Combinatorial Physical States

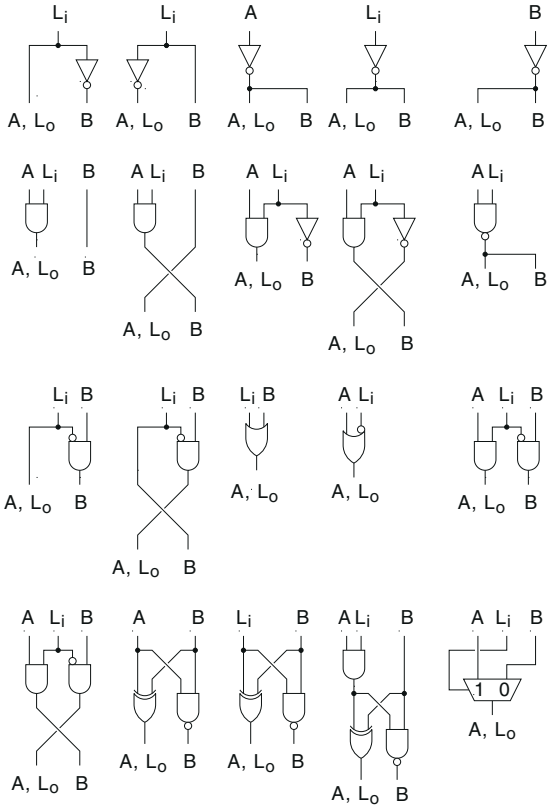


Figure 6. Register States

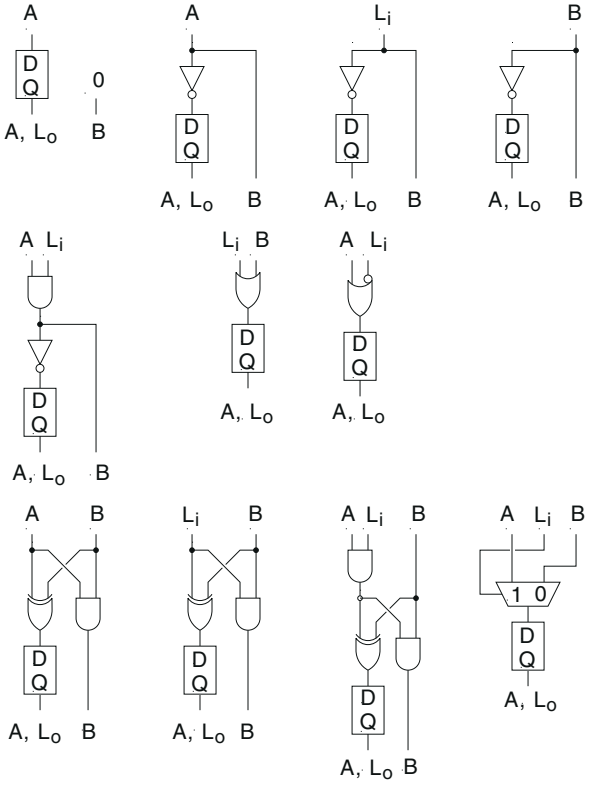


Figure 7. Physical Constants

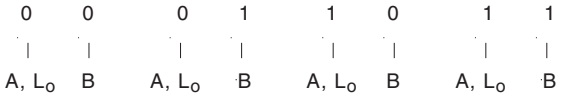


Figure 8. Two-input AND Feeding XOR

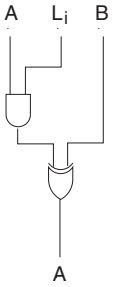
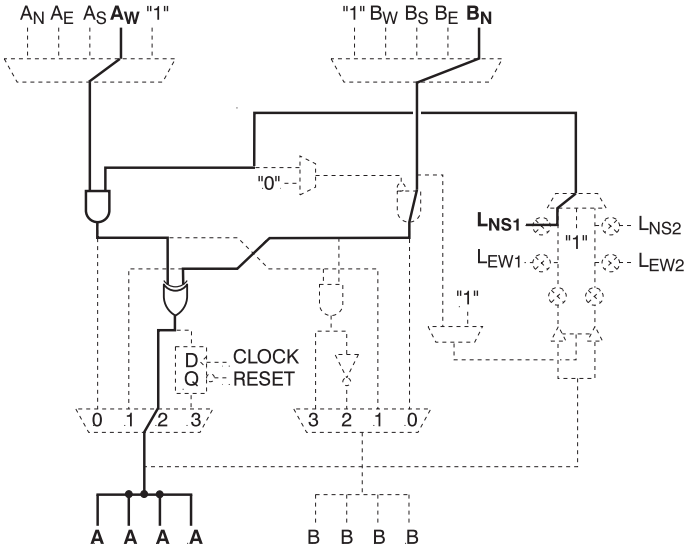


Figure 9. Cell Configuration (A•L) XOR B



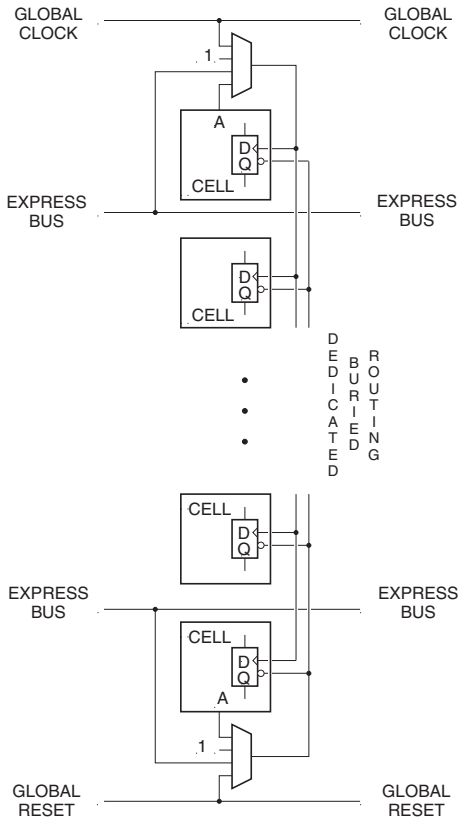
Clock Distribution

Along the top edge of the array is logic for distributing clock signals to the D flip-flop in each logic cell (Figure 10). The distribution network is organized by column and permits columns of cells to be independently clocked. At the head of each column is a user-configurable multiplexer providing the clock signal for that column. It has four inputs:

- Global clock supplied through the CLOCK pin
- Express bus adjacent to the distribution logic
- "A" output of the cell at the head of the column
- Logical constant "1" to conserve power (no clock)

Through the global clock, the network provides low-skew distribution of an externally supplied clock to any or all of the columns of the array. The global clock pin is also connected directly to the array via the A input of the upper left and right corner cells (AW on the left, and AN on the right). The express bus is useful in distributing a secondary clock to multiple columns when the global clock line is used as a primary clock. The A output of a cell is useful in providing a clock signal to a single column. The constant "1" is used to reduce power dissipation in columns using no registers.

Figure 10. Column Clock and Column Reset



Asynchronous Reset

Along the bottom edge of the array is logic for asynchronously resetting the D flip-flops in the logic cells (Figure 10). Like the clock network, the asynchronous reset network is organized by column and permits columns to be independently reset. At the bottom of each column is a user-configurable multiplexer providing the reset signal for that column. It has four inputs:

- Global asynchronous reset supplied through the $\overline{\text{RESET}}$ pin
- Express bus adjacent to the distribution logic
- "A" output of the cell at the foot of the column
- Logical constant "1" to conserve power

The asynchronous reset logic uses these four inputs in the same way that the clock distribution logic does. Through the global asynchronous reset, any or all columns can be reset by an externally supplied signal. The global asynchronous reset pin is also connected directly to the array via the A input of the lower left and right corner cells (AS on the left, and AE on the right). The express bus can be used to distribute a secondary reset to multiple columns when the global reset line is used as a primary reset, the A output of a cell can also provide an asynchronous reset signal to a single column, and the constant "1" is used by columns with registers requiring no reset. All registers are reset during power-up.

Input/Output

The Atmel architecture provides a flexible interface between the logic array, the configuration control logic and the I/O pins.

Two adjacent cells – an "exit" and an "entrance" cell – on the perimeter of the logic array are associated with each I/O pin.

There are two types of I/Os: A-type (Figure 11) and B-type (Figure 12). For A-type I/Os, the edge-facing A output of an exit cell is connected to an output driver, and the edge-facing A input of the adjacent entrance cell is connected to an input buffer. The output of the output driver and the input of the input buffer are connected to a common pin.

B-type I/Os are the same as A-type I/Os, but use the B inputs and outputs of their respective entrance and exit cells. A- and B-type I/Os alternate around the array Control of the I/O logic is provided by user-configurable memory bits.

Figure 11. A-type I/O Logic

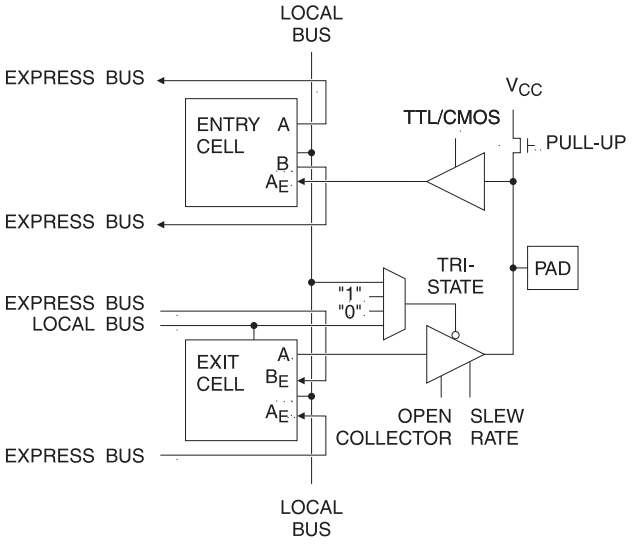
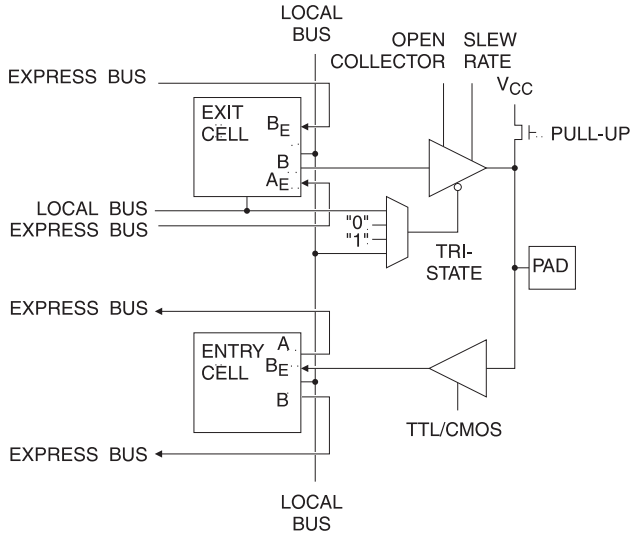


Figure 12. B-type I/O Logic



TTL/CMOS Inputs

A user-configurable bit determines the threshold level – TTL or CMOS – of the input buffer.

Open Collector/Tristate Outputs

A user-configurable bit which enables or disables the active pull-up of the output device.

Slew Rate Control

A user-configurable bit controls the slew rate – fast or slow – of the output buffer. A slow slew rate, which reduces noise and ground bounce, is recommended for outputs that are not speed-critical. Fast and slow slew rates have the same DC-current sinking capabilities, but the rate at which each allows the output devices to reach full drive differs.

Pull-up

A user-configurable bit controls the pull-up transistor in the I/O pin. It's primary function is to provide a logical "1" to unused input pins. When on, it is approximately equivalent to a 25K resistor to V_{CC}.

Enable Select

User-configurable bits determine the output-enable for the output driver. The output driver can be static – always on or always off – or dynamically controlled by a signal generated in the array. Four options are available from the array: (1) the control is low and always driving; (2) the control is high and never driving; (3) the control is connected to a vertical local bus associated with the output cell; or (4) the control is connected to a horizontal local bus associated with the output cell. On power-up, the user I/Os are configured as inputs with pull-up resistors.

In addition to the functionality provided by the I/O logic, the entrance and exit cells provide the ability to register both inputs and outputs. Also, these perimeter cells (unlike interior cells) are connected directly to express buses: the edge-facing A and B outputs of the entrance cell are connected to express buses, as are the edge-facing A and B inputs of the exit cell. These buses are perpendicular to the edge, and provide a rapid means of bringing I/O signals to and from the array interior and the opposite edge of the chip.

Chip Configuration

The Integrated Development System generates the SRAM bit pattern required to configure a AT6000 Series device. A PC parallel port, microprocessor, EPROM or serial configuration memory can be used to download configuration patterns.

Users select from several configuration modes. Many factors, including board area, configuration speed and the number of designs implemented in parallel can influence the user's final choice.

Configuration is controlled by dedicated configuration pins and dual-function pins that double as I/O pins when the device is in operation. The number of dual-function pins required for each mode varies.

memory to configure the FPGA. Addresses change after the rising edge of the CCLK signal.

$\overline{\text{CSOUT}}$ or I/O

When cascading devices, $\overline{\text{CSOUT}}$ is an output used to enable other devices. $\overline{\text{CSOUT}}$ should be connected to the $\overline{\text{CS}}$ input of the downstream device. The $\overline{\text{CSOUT}}$ function is optional and can be disabled during initial programming when cascading is not used. When cascading devices, $\overline{\text{CSOUT}}$ should be dedicated to configuration and not used as a configurable I/O.

$\overline{\text{CHECK}}$ or I/O

During configuration, $\overline{\text{CHECK}}$ is a TTL input that can be used to enable the data check function at the beginning of a configuration cycle. No data is written to the device while $\overline{\text{CHECK}}$ is low. Instead, the configuration file being applied to D0 (or D0 - D7, in parallel mode) is compared with the current contents of the internal configuration RAM. If a mismatch is detected between the data being loaded and the data already in the RAM, the $\overline{\text{ERR}}$ pin goes low. The $\overline{\text{CHECK}}$ function is optional and can be disabled during initial programming.

$\overline{\text{ERR}}$ or I/O

During configuration, $\overline{\text{ERR}}$ is an output. When the $\overline{\text{CHECK}}$ function is activated and a mismatch is detected between the current configuration data stream and the data already loaded in the configuration RAM, $\overline{\text{ERR}}$ goes low. The $\overline{\text{ERR}}$ ouput is a registered signal. Once a mismatch is found, the signal is set and is only reset after the configuration cycle is restarted. $\overline{\text{ERR}}$ is also asserted for configuration file errors. The $\overline{\text{ERR}}$ function is optional and can be disabled during initial programming.

Device Pinout Selection (Max. Number of User I/O)

	AT6002[1]	AT6003[1]	AT6005	AT6010
84 PLCC[1]	64 I/O	64 I/O	64 I/O	-
100 VQFP	80 I/O	80 I/O	80 I/O	-
132 PQFP[1]	96 I/O	108 I/O	-	-
144 TQFP	95 I/O	120 I/O	108 I/O	120 I/O
208 PQFP[1]	-	-	-	-
240 PQFP	-	-	-	204 I/O

Bit-stream Sizes

Mode(s)	Type	Beginning Sequence	AT6002[1]	AT6003[1]	AT6005	AT6010
1	Parallel	Preamble	2677	4153	8077	16393
2	Parallel	Preamble	2677	4153	8077	16393
3	Serial	Null Byte/Preamble	2678	4154	8078	16394
4	Serial	Null Byte/Preamble	2678	4154	8078	16394
5	Parallel	Preamble	2677	4153	8077	16393
6	Parallel	Preamble/Preamble	2678	4154	8078	16394

Note: 1. Obsolete. Not recommended for new design.

Pinout Assignment

Left Side (Top to Bottom)										
AT6002[3]	AT6003[3]	AT6005	AT6010	84[3] PLCC	100 VQFP	132[3] PQFP	144 TQFP	180[3] CPGA	208[3] PQFP	240[3] PQFP
-	-	-	I/O51(A)	-	-	-	-	B1	1	1
I/O24(A) or A7	I/O30(A) or A7	I/O27(A) or A7	I/O50(A) or A7	12	1	18	1	C1	2	2
-	I/O29(B)	-	I/O49(A)	-	-	-	2	D1	3	3
-	-	-	I/O48(B)	-	-	-	-	-	-	4
-	-	-	VCC	-	-	-	-	PWR[1]	4	5
-	-	-	I/O47(A)	-	-	-	-	E1	5	6
-	-	-	GND	-	-	-	-	GND[2]	6	7
-	I/O28(A)	I/O26(A)	I/O46(A)	-	-	19	3	G1	7	8
I/O23(A) or A6	I/O27(A) or A6	I/O25(A) or A6	I/O45(A) or A6	13	2	20	4	H1	8	9
-	-	-	I/O44(B)	-	-	-	-	-	-	10
-	-	-	I/O43(A)	-	-	-	-	C2	9	11
I/O22(B)	I/O26(A)	I/O24(A)	I/O42(A)	-	-	21	5	D2	10	12
I/O21(A) or A5	I/O25(A) or A5	I/O23(A) or A5	I/O41(A) or A5	14	3	22	6	E2	11	13
-	-	-	I/O40(B)	-	-	-	-	-	-	14
-	-	-	I/O39(A)	-	-	-	-	F2	12	15
I/O20(B)	I/O24(B)	I/O22(A)	I/O38(A)	-	4	23	7	G2	13	16
I/O19(A) or A4	I/O23(A) or A4	I/O21(A) or A4	I/O37(A) or A4	15	5	24	8	H2	14	17
-	-	-	I/O36(B)	-	-	-	-	-	-	18
I/O18(B)	I/O22(B)	I/O20(A)	I/O35(A)	-	-	25	9	D3	15	19
I/O17(A) or A3	I/O21(A) or A3	I/O19(A) or A3	I/O34(A) or A3	16	6	26	10	E3	16	20
I/O16(B)	I/O20(B)	I/O18(A)	I/O33(A)	-	7	27	11	F3	17	21
-	-	-	I/O32(B)	-	-	-	-	-	18	22
I/O15(A) or A2	I/O19(A) or A2	I/O17(A) or A2	I/O31(A) or A2	17	8	28	12	G3	19	23
-	I/O18(B)	I/O16(A)	I/O30(A)	-	-	29	13	H3	20	24
GND	GND	GND	GND	18	9	30	14	GND[2]	21	25
VSS	VSS	VSS	VSS	19	10	31	15	GND[2]	22	26
I/O14(A) or A1	I/O17(A) or A1	I/O15(A) or A1	I/O29(A) or A1	20	11	32	16	F4	23	27
-	-	-	I/O28(B)	-	-	-	-	-	24	28
-	I/O16(B)	-	I/O27(A)	-	-	-	17	G4	25	29
I/O13(A) or A0	I/O15(A) or A0	I/O14(A) or A0	I/O26(A) or A0	21	12	33	18	H4	26	30
I/O12(B) or D7	I/O14(A) or D7	I/O13(A) or D7	I/O25(B) or D7	22	13	34	19	H5	27	31
-	-	-	I/O24(B)	-	-	-	-	-	28	32
I/O11(A) or D6	I/O13(A) or D6	I/O12(A) or D6	I/O23(A) or D6	23	14	35	20	J4	29	33

Notes: 1. PWR = Pins connected to power plane = F1, E4/E5, L2, R4, K15, L12, E14, A12.
2. GND = Pins connected to ground plane = L4, M4, N9, N10, E12, D12, C7, C6.
3. Obsolete. Not recommended for new design.

Pinout Assignment

Bottom Side (Left to Right)										
AT6002[3]	AT6003[3]	AT6005	AT6010	84[3] PLCC	100 VQFP	132[3] PQFP	144 TQFP	180[3] CPGA	208[3] PQFP	240[3] PQFP
$\overline{CON}$	$\overline{CON}$	$\overline{CON}$	$\overline{CON}$	33	26	51	37	M5	53	61
-	-	-	I/O204(A)	-	-	-	-	M6	54	62
I/O96(A)	I/O120(A)	I/O108(A)	I/O203(A)	34	27	52	38	M7	55	63
-	I/O119(B)	-	I/O202(A)	-	-	-	39	R2	56	64
-	-	-	I/O201(B)	-	-	-	-	-	-	65
-	-	-	VCC	-	-	-	-	PWR[1]	57	66
-	-	-	I/O200(A)	-	-	-	-	R3	58	67
-	-	-	GND	-	-	-	-	GND[2]	59	68
-	I/O118(A)	I/O107(A)	I/O199(A)	-	-	53	40	R5	60	69
I/O95(A) or $\overline{CSOUT}$	I/O117(A) or $\overline{CSOUT}$	I/O106(A) or $\overline{CSOUT}$	I/O198(A) or $\overline{CSOUT}$	35	28	54	41	R6	61	70
-	-	-	I/O197(B)	-	-	-	-	-	-	71
-	-	-	I/O196(A)	-	-	-	-	R7	62	72
I/O94(B)	I/O116(A)	I/O105(A)	I/O195(A)	-	-	55	42	P3	63	73
I/O93(A)	I/O115(A)	I/O104(A)	I/O194(A)	36	29	56	43	P4	64	74
-	-	-	I/O193(B)	-	-	-	-	-	-	75
-	-	-	I/O192(A)	-	-	-	-	P5	65	76
I/O92(B)	I/O114(B)	I/O103(A)	I/O191(A)	-	30	57	44	P6	66	77
I/O91(A) or $\overline{CHECK}$	I/O113(A) or $\overline{CHECK}$	I/O102(A) or $\overline{CHECK}$	I/O190(A) or $\overline{CHECK}$	37	31	58	45	P7	67	78
-	-	-	I/O189(B)	-	-	-	-	-	-	79
I/O90(B)	I/O112(B)	I/O101(A)	I/O188(A)	-	-	59	46	N4	68	80
I/O89(A) or $\overline{ERR}$	I/O111(A) or $\overline{ERR}$	I/O100(A) or $\overline{ERR}$	I/O187(A) or $\overline{ERR}$	38	32	60	47	N5	69	81
I/O88(B)	I/O110(B)	I/O99(A)	I/O186(A)	-	33	61	48	N6	70	82
-	-	-	I/O185(B)	-	-	-	-	-	71	83
I/O87(A)	I/O109(A)	I/O98(A)	I/O184(A)	39	34	62	49	N7	72	84
-	I/O108(B)	I/O97(A)	I/O183(A)	-	-	63	50	M8	73	85
GND	GND	GND	GND	40	35	64	51	GND[2]	74	86
I/O86(A)	I/O107(A)	I/O96(A)	I/O182(A)	41	36	65	52	M9	75	87
-	-	-	I/O181(B)	-	-	-	-	-	76	88
-	I/O106(B)	-	I/O180(A)	-	-	-	53	M10	77	89
I/O85(A)	I/O105(A)	I/O95(A)	I/O179(A)	42	37	66	54	M11	78	90
$\overline{CS}$	$\overline{CS}$	$\overline{CS}$	$\overline{CS}$	43	38	67	55	L8	79	91
I/O84(B)	I/O104(A)	I/O94(A)	I/O178(A)	44	39	68	56	M12	80	92

Notes: 1. PWR = Pins connected to power plane = F1, E4/E5, L2, R4, K15, L12, E14, A12.
2. GND = Pins connected to ground plane = L4, M4, N9, N10, E12, D12, C7, C6.
3. Obsolete. Not recommended for new design.

Pinout Assignment

Right Side (Bottom to Top)										
AT6002[5]	**AT6003[5]**	**AT6005**	**AT6010**	**84[5] PLCC**	**100 VQFP**	**132[5] PQFP**	**144 TQFP**	**180[5] CPGA**	**208[5] PQFP**	**240[5] PQFP**
-	-	-	I/O153(A)	-	-	-	-	P15	105	121
I/O72(A)	I/O90(A)	I/O81(A)	I/O152(A)	54	51	84	73	N15	106	122
-	I/O89(B)	I/O80(A)	I/O151(A)	-	-	85[3]	74	M15	107	123
-	-	-	I/O150(B)	-	-	-	-	-	-	124
-	-	-	VCC	-	-	-	-	PWR[1]	108	125
-	-	-	I/O149(A)	-	-	-	-	L15	109	126
-	-	-	GND	-	-	-	-	GND[2]	110	127
-	I/O88(A)	-	I/O148(A)	-	-	85[4]	75	J15	111	128
I/O71(A)	I/O87(A)	I/O79(A)	I/O147(A)	55	52	86	76	H15	112	129
-	-	-	I/O146(B)	-	-	-	-	-	-	130
-	-	-	I/O145(A)	-	-	-	-	N14	113	131
I/O70(B)	I/O86(A)	I/O78(A)	I/O144(A)	-	-	87	77	M14	114	132
I/O69(A)	I/O85(A)	I/O77(A)	I/O143(A)	56	53	88	78	L14	115	133
-	-	-	I/O142(B)	-	-	-	-	-	-	134
-	-	-	I/O141(A)	-	-	-	-	K14	116	135
I/O68(B)	I/O84(B)	I/O76(A)	I/O140(A)	-	54	89	79	J14	117	136
I/O67(A)	I/O83(A)	I/O75(A)	I/O139(A)	57	55	90	80	H14	118	137
-	-	-	I/O138B	-	-	-	-	-	-	138
I/O66(B)	I/O82(B)	I/O74(A)	I/O137(A)	-	-	91	81	M13	119	139
I/O65(A)	I/O81(A)	I/O73(A)	I/O136(A)	58	56	92	82	L13	120	140
I/O64(B)	I/O80(B)	I/O72(A)	I/O135(A)	-	57	93	83	K13	121	141
-	-	-	I/O134(B)	-	-	-	-	-	122	142
I/O63(A)	I/O79(A)	I/O71(A	I/O133(A)	59	58	94	84	J13	123	143
-	I/O78(B)	I/O70(A)	I/O132(A)	-	-	95	85	H13	124	144
GND	GND	GND	GND	60	59	96	86	GND[2]	125	145
VSS	VSS	VSS	VSS	61	60	97	87	GND[2]	126	146
I/O62(A)	I/O77(A)	I/O69(A)	I/O131(A)	62	61	98	88	K12	127	147
-	-	-	I/O130(B)	-	-	-	-	-	128	148
-	I/O76(B)	-	I/O129(A)	-	-	-	89	J12	129	149
I/O61(A)	I/O75(A)	I/O68(A)	I/O128(A)	63	62	99	90	H12	130	150
I/O60(B)	I/O74(A)	I/O67(A)	I/O127(A)	64	63	100	91	H11	131	151
-	-	-	I/O126(B)	-	-	-	-	-	132	152

Notes:
1. PWR = Pins connected to power plane = F1, E4/E5, L2, R4, K15, L12, E14, A12.
2. GND = Pins connected to ground plane = L4, M4, N9, N10, E12, D12, C7, C6.
3. 85 = Pin 85 on AT6005.
4. 85 = Pin 85 on AT6003 and AT6010.
5. Obsolete. Not recommended for new design.

Pinout Assignment

Top Side (Right to Left)										
AT6002[3]	**AT6003[3]**	**AT6005**	**AT6010**	**84[3] PLCC**	**100 VQFP**	**132[3] PQFP**	**144 TQFP**	**180[3] CPGA**	**208[3] PQFP**	**240[3] PQFP**
M1	M1	M1	M1	75	76	117	109	D11	157	181
-	-	-	I/O102(A)	-	-	-	-	D10	158	182
I/O48(A)	I/O60(A)	I/O54(A)	I/O101(A)	76	77	118	110	D9	159	183
-	I/O59(B)	-	I/O100(A)	-	-	-	111	A14	160	184
-	-	-	I/O99(B)	-	-	-	-	-	-	185
-	-	-	VCC	-	-	-	-	PWR[1]	161	186
-	-	-	I/O98(A)	-	-	-	-	A13	162	187
-	-	-	GND	-	-	-	-	GND[2]	163	188
-	I/O58(A)	I/O53(A)	I/O97(A)	-	-	119	112	A11	164	189
I/O47(A)	I/O57(A)	I/O52(A)	I/O96(A)	77	78	120	113	A10	165	190
-	-	-	I/O95(B)	-	-	-	-	-	-	191
-	-	-	I/O94(A)	-	-	-	-	A9	166	192
I/O46(B)	I/O56(A)	I/O51(A)	I/O93(A)	-	-	121	114	B13	167	193
I/O45(A)	I/O55(A)	I/O50(A)	I/O92(A)	78	79	122	115	B12	168	194
-	-	-	I/O91(B)	-	-	-	-	-	-	195
-	-	-	I/O90(A)	-	-	-	-	B11	169	196
I/O44(B)	I/O54(B)	I/O49(A)	I/O89(A)	-	80	123	116	B10	170	197
I/O43(A)	I/O53(A)	I/O48(A)	I/O88(A)	79	81	124	117	B9	171	198
-	-	-	I/O87(B)	-	-	-	-	-	-	199
I/O42(B)	I/O52(B)	I/O47(A)	I/O86(A)	-	-	125	118	C12	172	200
I/O41(A)	I/O51(A)	I/O46(A)	I/O85(A)	80	82	126	119	C11	173	201
I/O40(B)	I/O50(B)	I/O45(A)	I/O84(A)	-	83	127	120	C10	174	202
-	-	-	I/O83(B)	-	-	-	-	-	175	203
I/O39(A)	I/O49(A)	I/O44(A)	I/O82(A)	81	84	128	121	C9	176	204
-	I/O48(B)	I/O43(A)	I/O81(A)	-	-	129	122	D8	177	205
GND	GND	GND	GND	82	85	130	123	GND[2]	178	206
I/O38(A)	I/O47(A)	I/O42(A)	I/O80(A)	83	86	131	124	D7	179	207
-	-	-	I/O79(B)	-	-	-	-	-	180	208
-	I/O46(B)	-	I/O78(A)	-	-	-	125	D6	181	209
I/O37(A) or A16	I/O45(A) or A16	I/O41(A) or A16	I/O77(A) or A16	84	87	132	126	D5	182	210
CLOCK	CLOCK	CLOCK	CLOCK	1	88	1	127	E8	183	211
I/O36(B) or A15	I/O44(B) or A15	I/O40(A) or A15	I/O76(A) or A15	2	89	2	128	D4	184	212

Notes: 1. PWR = Pins connected to power plane = F1, E4/E5, L2, R4, K15, L12, E14, A12.
2. GND = Pins connected to ground plane = L4, M4, N9, N10, E12, D12, C7, C6.
3. Obsolete. Not recommended for new design.

AC Timing Characteristics – 5V Operation

Delays are based on fixed load. Loads for each type of device are described in the notes. Delays are in nanoseconds. Worst case: V_{CC} = 4.75V to 5.25V. Temperature = 0°C to 70°C.

Cell Function	Parameter	From	To	Load Definition(7)	-1	-2	-4	Units
Wire(4)	t_{PD} (max)(4)	A, B, L	A, B	1	0.8	1.2	1.8	ns
NAND	t_{PD} (max)	A, B, L	B	1	1.6	2.2	3.2	ns
XOR	t_{PD} (max)	A, B, L	A	1	1.8	2.4	4.0	ns
AND	t_{PD} (max)	A, B, L	B	1	1.7	2.2	3.2	ns
MUX	t_{PD} (max)	A, B	A	1	1.7	2.3	4.0	ns
		L	A	1	2.1	3.0	4.9	ns
D-Flip-flop(5)	t_{setup} (min)	A, B, L	CLK	-	1.5	2.0	3.0	ns
D-Flip-flop(5)	t_{hold} (min)	CLK	A, B, L	-	0	0	0	ns
D-Flip-flop	t_{PD} (max)	CLK	A	1	1.5	2.0	3.0	ns
Bus Driver	t_{PD} (max)	A	L	2	2.0	2.6	4.0	ns
Repeater	t_{PD} (max)	L, E	E	3	1.3	1.6	2.3	ns
		L, E	L	2	1.7	2.1	3.0	ns
Column Clock	t_{PD} (max)	GCLK, A, ES	CLK	3	1.8	2.4	3.0	ns
Column Reset	t_{PD} (max)	GRES, A, EN	RES	3	1.8	2.4	3.0	ns
Clock Buffer(5)	t_{PD} (max)	CLOCK PIN	GCLK	-	1.6	2.0	2.9	ns
Reset Buffer(5)	t_{PD} (max)	RESET PIN	GRES	-	1.5	1.9	2.8	ns
TTL Input(1)	t_{PD} (max)	I/O	A	3	1.0	1.2	1.5	ns
CMOS Input(2)	t_{PD} (max)	I/O	A	3	1.3	1.4	2.3	ns
Fast Output(3)	t_{PD} (max)	A	I/O PIN	4	3.3	3.5	6.0	ns
Slow Output(3)	t_{PD} (max)	A	I/O PIN	4	7.5	8.0	12.0	ns
Output Disable(5)	t_{PXZ} (max)	L	I/O PIN	4	3.1	3.3	5.5	ns
Fast Enable(3)(5)	t_{PXZ} (max)	L	I/O PIN	4	3.8	4.0	6.5	ns
Slow Enable(3)(5)	t_{PXZ} (max)	L	I/O PIN	4	8.2	8.5	12.5	ns

Device	Cell Types	Outputs	I_{CC} (max)
Cell(6)	Wire, XWire, Half-adder, Flip-flop	A, B	4.5 µA/MHz
Bus(6)	Wire, XWire, Half-adder, Flip-flop, Repeater	L	2.5 µA/MHz
Column Clock(6)	Column Clock Driver	CLK	40 µA/MHz

Notes:
1. TTL buffer delays are measured from a V_{IH} of 1.5V at the pad to the internal V_{IH} at A. The input buffer load is constant.
2. CMOS buffer delays are measured from a V_{IH} of 1/2 V_{CC} at the apd to the internal V_{IH} at A. The input buffer load is constant.
3. Buffer delay is to a pad voltage of 1.5V with one output switching.
4. Max specifications are the average of mas t_{PDLH} and t_{PDHL}.
5. Parameter based on characterization and simulation; not tested in production
6. Exact power calculation is available in an Atmel application note.
7. Load Definition: 1 = Load of one A or B input; 2 = Load of one L input; 3 = Constant Load; 4 = Tester Load of 50 pF.

AC Timing Characteristics – 3.3V Operation (8)

Delays are based on fixed load. Loads for each type of device are described in the notes. Delays are in nanoseconds. Worst case: V_{CC} = 3.0V to 3.6V. Temperature = 0°C to 70°C.

Cell Function	Parameter	From	To	Load Definition(7)	-4	Units
Wire(4)	t_{PD} (max)(4)	A, B, L	A, B	1	1.8	ns
NAND	t_{PD} (max)	A, B, L	B	1	3.2	ns
XOR	t_{PD} (max)	A, B, L	A	1	4.0	ns
AND	t_{PD} (max)	A, B, L	B	1	3.2	ns
MUX	t_{PD} (max)	A, B	A	1	4.0	ns
		L	A	1	4.9	ns
D-Flip-flop(5)	t_{setup} (min)	A, B, L	CLK	-	3.0	ns
D-Flip-flop(5)	t_{hold} (min)	CLK	A, B, L	-	0	ns
D-Flip-flop	t_{PD} (max)	CLK	A	1	3.0	ns
Bus Driver	t_{PD} (max)	A	L	2	4.0	ns
Repeater	t_{PD} (max)	L, E	E	3	2.3	ns
		L, E	L	2	3.0	ns
Column Clock	t_{PD} (max)	GCLK, A, ES	CLK	3	3.0	ns
Column Reset	t_{PD} (max)	GRES, A, EN	RES	3	3.0	ns
Clock Buffer(5)	t_{PD} (max)	CLOCK PIN	GCLK	4	2.9	ns
Reset Buffer(5)	t_{PD} (max)	RESET PIN	GRES	5	2.8	ns
TTL Input(1)	t_{PD} (max)	I/O	A	3	1.5	ns
CMOS Input(2)	t_{PD} (max)	I/O	A	3	2.3	ns
Fast Output(3)	t_{PD} (max)	A	I/O PIN	6	6.0	ns
Slow Output(3)	t_{PD} (max)	A	I/O PIN	6	12.0	ns
Output Disable(5)	t_{PXZ} (max)	L	I/O PIN	6	5.5	ns
Fast Enable(3)(5)	t_{PXZ} (max)	L	I/O PIN	6	6.5	ns
Slow Enable(3)(5)	t_{PXZ} (max)	L	I/O PIN	6	12.5	ns

Device	Cell Types	Outputs	I_{CC} (max)
Cell(6)	Wire, XWire, Half-adder, Flip-flop	A, B	2.3 µA/MHz
Bus(6)	Wire, XWire, Half-adder, Flip-flop, Repeater	L	1.3 µA/MHz
Column Clock(6)	Column Clock Driver	CLK	20 µA/MHz

Notes:
1. TTL buffer delays are measured from a V_{IH} of 1.5V at the pad to the internal V_{IH} at A. The input buffer load is constant.
2. CMOS buffer delays are measured from a V_{IH} of 1/2 V_{CC} at the apd to the internal V_{IH} at A. The input buffer load is constant.
3. Buffer delay is to a pad voltage of 1.5V with one output switching.
4. Max specifications are the average of mas t_{PDLH} and t_{PDHL}.
5. Parameter based on characterization and simulation; not tested in production
6. Exact power calculation is available in an Atmel application note.
7. Load Definition: 1 = Load of one A or B input; 2 = Load of one L input; 3 = Constant Load; 4 = Load of 28 Clock Columns; 5 = Load of 28 Reset Columns; 6 = Tester Load of 50 pF.
8. Obsolete. Not recommended for new design.

Absolute Maximum Ratings*

Supply Voltage (V_{CC})	-0.5V to + 7.0V
DC Input Voltage (V_{IN})	-0.5V to V_{CC} + 0.5V
DC Output Voltage (V_{ON})	-0.5V to V_{CC} + 0.5V
Storage Temperature Range (TSTG)	-65 °C to +150°C
Power Dissipation (PD)	1500 mW
Lead Temperature (T_L) (Soldering, 10 sec.)	260°C
ESD (R_{ZAP} = 1.5K, C_{ZAP} = 100 pF)	2000V

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress rating only and functional operation of the device at these or any other conditions beyond those listed under operating conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

DC and AC Operating Rage – 5V Operation

		AT6002-2/4(1) AT6003-2/4(1) AT6005-2/4(1) AT6010-2/4(1) Commercial(1)	**AT6002-2/4(1) AT6003-2/4(1) AT6005-2/4 AT6010-2/4 Industrial**	**AT6002-2/4(1) AT6003-2/4(1) AT6005-2/4(1) AT6010-2/4(1) Military(1)**
Operating Temperature (Case)		0°C - 70°C	-40°C - 85°C	-55°C - 125°C
V_{CC} Power Supply		5V ± 5%	5V ± 10%	5V ± 10%
Input Voltage Level (TTL)	High (V_{IHT})	2.0V - V_{CC}	2.0V - V_{CC}	2.0V - V_{CC}
	Low (V_{ILT})	0V - 0.8V	0V - 0.8V	0V - 0.8V
Input Voltage Level (CMOS)	High (V_{IHC})	70% - 100% V_{CC}	70% - 100% V_{CC}	70% - 100% V_{CC}
	Low (V_{ILC})	0 - 30% V_{CC}	0 - 30% V_{CC}	0 - 30% V_{CC}
Input Signal Transition Time (T_{IN})		50 ns (max)	50 ns (max)	50 ns (max)

DC and AC Operating Rage – 3.3V Operation(1)

		AT6002-2/4(1), AT6003-2/4(1) AT6005-2/4(1), AT6010-2/4(1) Commercial
Operating Temperature (Case)		0°C - 70°C
V_{CC} Power Supply		3.3V ± 5%
Input Voltage Level (TTL)	High (V_{IHT})	2.0V - V_{CC}
	Low (V_{ILT})	0V - 0.8V
Input Voltage Level (CMOS)	High (V_{IHC})	70% - 100% V_{CC}
	Low (V_{ILC})	0 - 30% V_{CC}
Input Signal Transition Time (T_{IN})		50 ns (max)

Note: 1. Obsolete. Not recommended for new design.

DC Characteristics – 5V Operation

Symbol	Parameter	Conditions		Min	Max	Units
V_{IH}	High-level Input Voltage	Commercial	CMOS	70% V_{CC}	V_{CC}	V
			TTL	2.0	V_{CC}	V
V_{IL}	Low-level Input Voltage	Commercial	CMOS	0	30% V_{CC}	V
			TTL	0	0.8	V
V_{OH}	High-level Output Voltage	Commercial	I_{OH} = -4 mA, V_{CC} min	3.9		V
			I_{OH} = -16 mA, V_{CC} min	3.0		V
V_{OL}	Low-level Output Voltage	Commercial	I_{OL} = 4 mA, V_{CC} min		0.4	V
			I_{OL} = 16 mA, V_{CC} min		0.5	V
I_{OZH}	High-level Tristate Output Leakage Current	$V_O = V_{CC}$ (max)			10	µA
I_{OZL}	High-level Tristate	Without Pull-up, $V_O = V_{SS}$		-10		µA
	Output Leakage Current	With Pull-up, $V_O = V_{SS}$		-500		µA
I_{IH}	High-level Input Current	$V_{IN} = V_{CC}$ (max)			10	µA
I_{IL}	Low-level Input Current	Without Pull-up, $V_{IN} = V_{SS}$		-10		µA
		With Pull-up, $V_{IN} = V_{SS}$		-500		µA
I_{CC}	Power Consumption	Without Internal Oscillator (Standby)			500	µA
C_{IN}	Input Capacitance	All Pins			10	pF

Note: 1. Obsolete. Not recommended for new design.

Ordering Information – AT6002[1]

Usable Gates	Speed Grade (ns)	Ordering Code	Package	Operation Range
6,000	2	AT6002-2AC AT6002A-2AC AT6002-2JC AT6002-2QC	100A 144A 84J 132Q	5V Commercial (0°C to 70°C)
		AT6002-2AI AT6002A-2AI AT6002-2JI AT6002-2QI	100A 144A 84J 132Q	5V Industrial (-40°C to 85°C)
6,000	4	AT6002-4AC AT6002A-4AC AT6002-4JC AT6002-4QC	100A 144A 84J 132Q	5V Commercial (0°C to 70°C)
		AT6002LV-4AC AT6002ALV-4AC AT6002LV-4JC AT6002LV-4QC	100A 144A 84J 132Q	3.3V Commercial (0°C to 70°C)
		AT6002-4AI AT6002A-4AI AT6002-4JI AT6002-4QI	100A 144A 84J 132Q	5V Industrial (-40°C to 85°C)

Note: 1. Obsolete. Not recommended for new design.

Package Type	
84J	84-lead, Plastic J-leaded Chip Carrier (PLCC)
100A	100-lead, Very Thin (1.0 mm) Plastic Gull-Wing Quad Flat Package (VQFP)
132Q	132-lead, Bumpered Plastic Gull-Wing Quad Flat Package (BQFP)
144A	144-lead, Thin (1.4 mm) Plastic Gull-Wing Quad Flat Package (TQFP)
208Q	208-lead, Plastic Gull-Wing Quad Flat Package (PQFP)
240Q	240-lead, Plastic Gull-Wing Quad Flat Package (PQFP)

Ordering Information – AT6003[1]

Usable Gates	Speed Grade (ns)	Ordering Code	Package	Operation Range
9,000	2	AT6003-2AC AT6003A-2AC AT6003-2JC AT6003-2QC	100A 144A 84J 132Q	5V Commercial (0°C to 70°C)
		AT6003-2AI AT6003A-2AI AT6003-2JI AT6003-2QI	100A 144A 84J 132Q	Industrial (-40°C to 85°C)
9,000	4	AT6003-4AC AT6003A-4AC AT6003-4JC AT6003-4QC	100A 144A 84J 132Q	5V Commercial (0°C to 70°C)
		AT6003LV-4AC AT6003ALV-4AC AT6003LV-4JC AT6003LV-4QC	100A 144A 84J 132Q	3.3V Commercial (0°C to 70°C)
		AT6003-4AI AT6003A-4AI AT6003-4JI AT6003-4QI	100A 144A 84J 132Q	5V Industrial (-40°C to 85°C)

Note: 1. Obsolete. Not recommended for new design.

Package Type	
84J	84-lead, Plastic J-leaded Chip Carrier (PLCC)
100A	100-lead, Very Thin (1.0 mm) Plastic Gull-Wing Quad Flat Package (VQFP)
132Q	132-lead, Bumpered Plastic Gull-Wing Quad Flat Package (BQFP)
144A	144-lead, Thin (1.4 mm) Plastic Gull-Wing Quad Flat Package (TQFP)
208Q	208-lead, Plastic Gull-Wing Quad Flat Package (PQFP)
240Q	240-lead, Plastic Gull-Wing Quad Flat Package (PQFP)

Revision History

Doc. No.	Date	Description
0264G	04/2015	Obsoleted AT6002, AT6003, and all AT6K low voltage (LV) devices and the AT6005 and AT6010A lead based packages. Added lead free packages options for AT6005 and AT6010A devices.
0264F	10/2009	

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