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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

| | |
|--------------------------------|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | 6400 |
| Total RAM Bits | - |
| Number of I/O | 108 |
| Number of Gates | 30000 |
| Voltage - Supply | 3.135V ~ 3.465V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 70°C |
| Package / Case | 132-BQFP Bumpered |
| Supplier Device Package | 132-BQFP (27.44x27.44) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/at6010lv-4qc |

Figure 2. Busing Network (one sector)

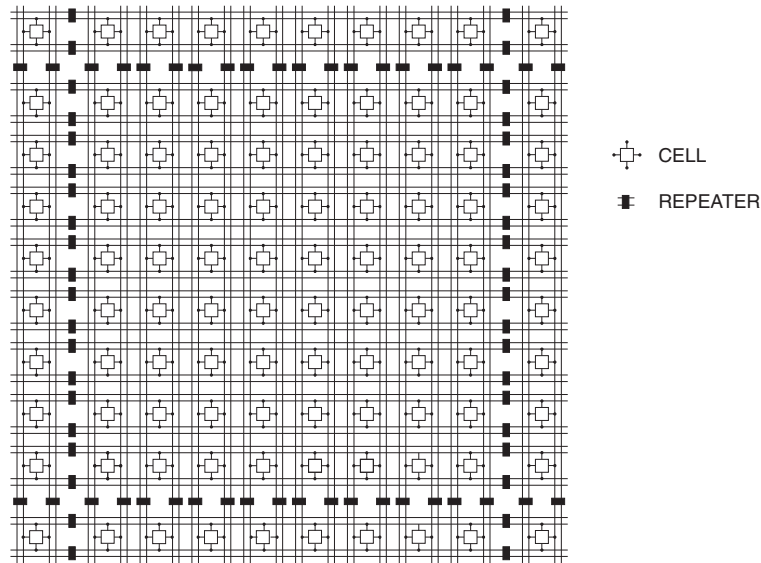
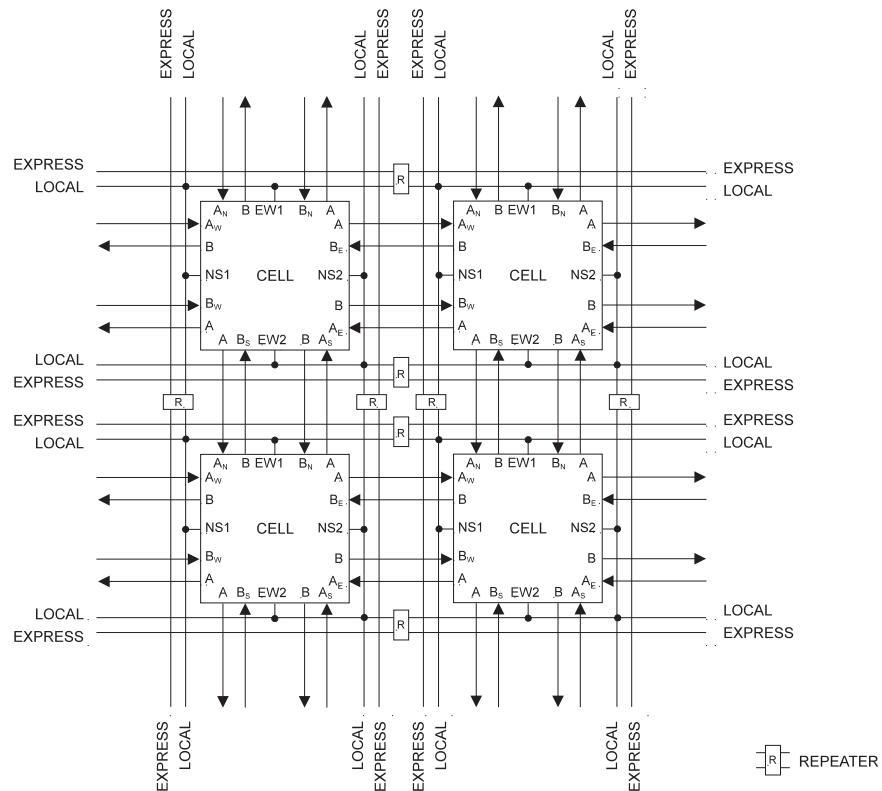


Figure 3. Cell-to-cell and Bus-to-bus Connections



Each cell, in addition, provides the ability to route a signal on a 90° turn between the NS1 bus and EW1 bus and between the NS2 bus and EW2 bus.

Express buses are not connected directly to cells, and thus provide higher speeds. They are the fastest way to cover long, straight-line distances within the array.

Each express bus is paired with a local bus, so there are two express buses for every column and two express buses for every row of cells.

Connective units, called repeaters, spaced every eight cells, divide each bus, both local and express, into segments spanning eight cells. Repeaters are aligned in rows and columns thereby partitioning the array into 8 x 8 sectors of cells. Each repeater is associated with a local/express pair, and on each side of the repeater are connections to a local-bus segment and an express-bus segment. The repeater can be programmed to provide any one of twenty-one connecting functions. These functions are symmetric with respect to both the two repeater sides and the two types of buses.

Among the functions provided are the ability to:

- Isolate bus segments from one another
- Connect two local-bus segments
- Connect two express-bus segments
- Implement a local/express transfer

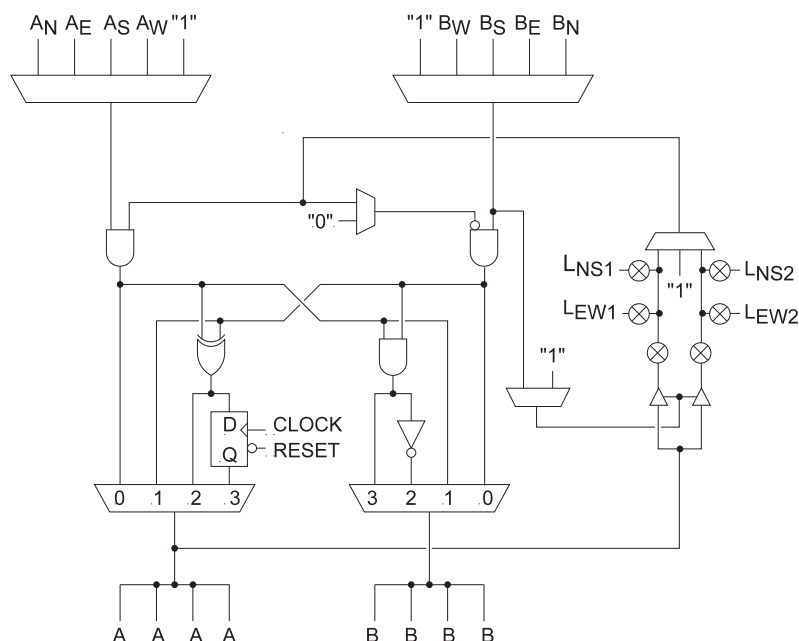
In all of these cases, each connection provides signal regeneration and is thus unidirectional. For bidirectional connections, the basic repeater function for the NS2 and EW2 repeaters is augmented with a special programmable connection allowing bidirectional communication between local-bus segments. This option is primarily used to implement long, tristate buses.

The Cell Structure

The Atmel cell (Figure 4) is simple and small and yet can be programmed to perform all the logic and wiring functions needed to implement any digital circuit. Its four sides are functionally identical, so each cell is completely symmetrical.

Read/write access to the four local buses – NS1, EW1, NS2 and EW2 – is controlled, in part, by four bidirectional pass gates connected directly to the buses. To read a local bus, the pass gate for that bus is turned on and the three-input multiplexer is set accordingly. To write to a local bus, the pass gate for that bus and the pass gate for the associated tristate driver are both turned on. The two-input multiplexer supplying the control signal to the drivers permits either: (1) active drive, or (2) dynamic tristating controlled by the B input. Turning between L_{NS1} and L_{EW1} or between L_{NS2} and L_{EW2} is accomplished by turning on the two associated pass gates. The operations of reading, writing and turning are subject to the restriction that each bus can be involved in no more than a **single** operation.

Figure 4. Cell Structure



In addition to the four local-bus connections, a cell receives two inputs and provides two outputs to each of its North (N), South (S), East (E) and West (W) neighbors. These inputs and outputs are divided into two classes: “A” and “B”. There is an A input and a B input from each neighboring cell and an A output and a B output driving all four neighbors. Between cells, an A output is always connected to an A input and a B output to a B input.

Within the cell, the four A inputs and the four B inputs enter two separate, independently configurable multiplexers. Cell flexibility is enhanced by allowing each multiplexer to select also the logical constant “1”. The two multiplexer outputs enter the two upstream AND gates.

Downstream from these two AND gates are an Exclusive-OR (XOR) gate, a register, an AND gate, an inverter and two four-input multiplexers producing the A and B outputs. These multiplexers are controlled in tandem (unlike the A and B input multiplexers) and determine the function of the cell.

- In State 0 – corresponding to the “0” inputs of the multiplexers – the output of the left-hand upstream AND gate is connected to the cell’s A output, and the output of the right-hand upstream AND gate is connected to the cell’s B output.
- In State 1 – corresponding to the “1” inputs of the multiplexers – the output of the left-hand upstream AND gate is connected to the cell’s B output, the output of the right-hand upstream AND gate is connected to the cell’s A output.
- In State 2 – corresponding to the “2” inputs of the multiplexers – the XOR of the outputs from the two upstream AND gates is provided to the cell’s A output, while the NAND of these two outputs is provided to the cell’s B output.

- In State 3 – corresponding to the “3” inputs of the multiplexers – the XOR function of State 2 is provided to the D input of a D-type flip-flop, the Q output of which is connected to the cell’s A output. Clock and asynchronous reset signals are supplied externally as described later. The AND of the outputs from the two upstream AND gates is provided to the cell’s B output.

Logic States

The Atmel cell implements a rich and powerful set of logic functions, stemming from 44 logical cell states which permute into 72 physical states. Some states use both A and B inputs. Other states are created by selecting the “1” input on either or both of the input multiplexers.

There are 28 combinatorial primitives created from the cell’s tristate capabilities and the 20 physical states represented in Figure 5. Five logical primitives are derived from the physical constants shown in Figure 7. More complex functions are created by using cells in combination.

A two-input AND feeding an XOR (Figure 8) is produced using a single cell (Figure 9). A two-to-one multiplexer selects the logical constant “0” and feeds it to the right-hand AND gate. The AND gate acts as a feed-through, letting the B input pass through to the XOR. The three-to-one multiplexer on the right side selects the local-bus input, LNS1, and passes it to the left-hand AND gate. The A and LNS1 signals are the inputs to the AND gate. The output of the AND gate feeds into the XOR, producing the logic state (A•L) XOR B.

Figure 5. Combinatorial Physical States

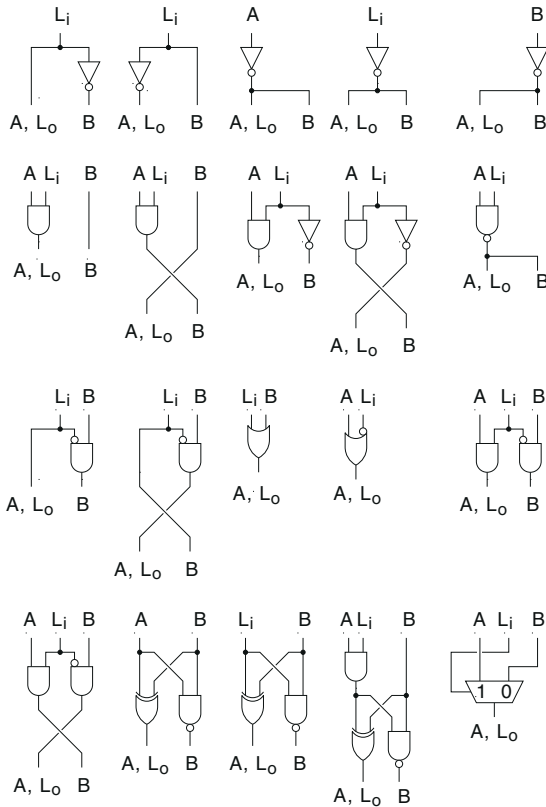


Figure 6. Register States

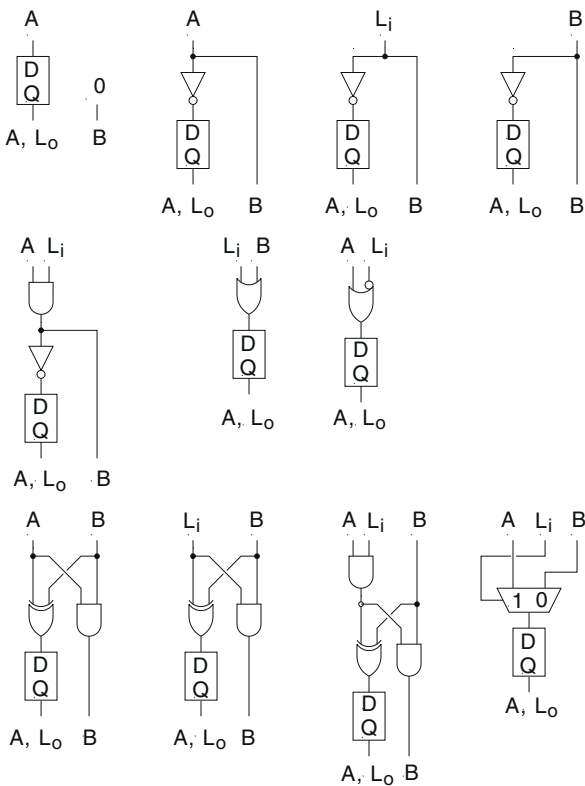


Figure 7. Physical Constants

| | | | | | | | |
|-------------------|---|-------------------|---|-------------------|---|-------------------|---|
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| A, L ₀ | B | A, L ₀ | B | A, L ₀ | B | A, L ₀ | B |

Figure 8. Two-input AND Feeding XOR

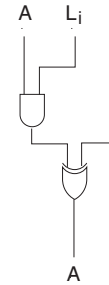
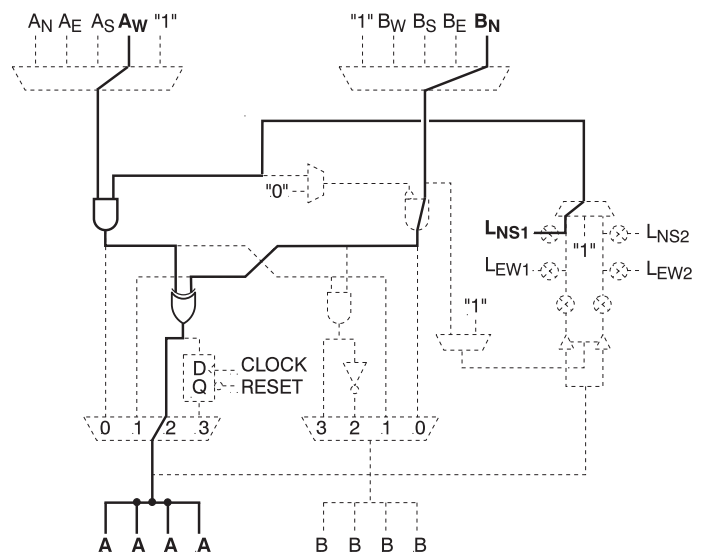


Figure 9. Cell Configuration (A•L) XOR B



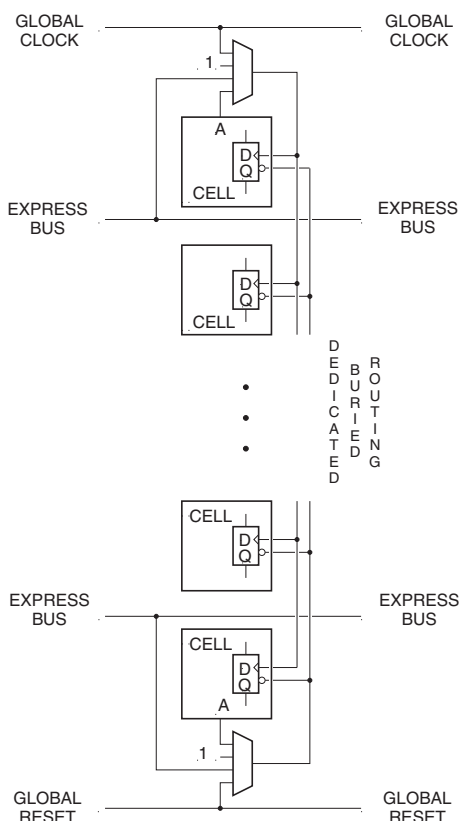
Clock Distribution

Along the top edge of the array is logic for distributing clock signals to the D flip-flop in each logic cell (Figure 10). The distribution network is organized by column and permits columns of cells to be independently clocked. At the head of each column is a user-configurable multiplexer providing the clock signal for that column. It has four inputs:

- Global clock supplied through the CLOCK pin
- Express bus adjacent to the distribution logic
- “A” output of the cell at the head of the column
- Logical constant “1” to conserve power (no clock)

Through the global clock, the network provides low-skew distribution of an externally supplied clock to any or all of the columns of the array. The global clock pin is also connected directly to the array via the A input of the upper left and right corner cells (AW on the left, and AN on the right). The express bus is useful in distributing a secondary clock to multiple columns when the global clock line is used as a primary clock. The A output of a cell is useful in providing a clock signal to a single column. The constant “1” is used to reduce power dissipation in columns using no registers.

Figure 10. Column Clock and Column Reset



Asynchronous Reset

Along the bottom edge of the array is logic for asynchronously resetting the D flip-flops in the logic cells (Figure 10). Like the clock network, the asynchronous reset network is organized by column and permits columns to be independently reset. At the bottom of each column is a user-configurable multiplexer providing the reset signal for that column. It has four inputs:

- Global asynchronous reset supplied through the $\overline{\text{RESET}}$ pin
- Express bus adjacent to the distribution logic
- “A” output of the cell at the foot of the column
- Logical constant “1” to conserve power

The asynchronous reset logic uses these four inputs in the same way that the clock distribution logic does. Through the global asynchronous reset, any or all columns can be reset by an externally supplied signal. The global asynchronous reset pin is also connected directly to the array via the A input of the lower left and right corner cells (AS on the left, and AE on the right). The express bus can be used to distribute a secondary reset to multiple columns when the global reset line is used as a primary reset, the A output of a cell can also provide an asynchronous reset signal to a single column, and the constant “1” is used by columns with registers requiring no reset. All registers are reset during power-up.

Input/Output

The Atmel architecture provides a flexible interface between the logic array, the configuration control logic and the I/O pins.

Two adjacent cells – an “exit” and an “entrance” cell – on the perimeter of the logic array are associated with each I/O pin.

There are two types of I/Os: A-type (Figure 11) and B-type (Figure 12). For A-type I/Os, the edge-facing A output of an exit cell is connected to an output driver, and the edge-facing A input of the adjacent entrance cell is connected to an input buffer. The output of the output driver and the input of the input buffer are connected to a common pin.

B-type I/Os are the same as A-type I/Os, but use the B inputs and outputs of their respective entrance and exit cells. A- and B-type I/Os alternate around the array. Control of the I/O logic is provided by user-configurable memory bits.

Figure 11. A-type I/O Logic

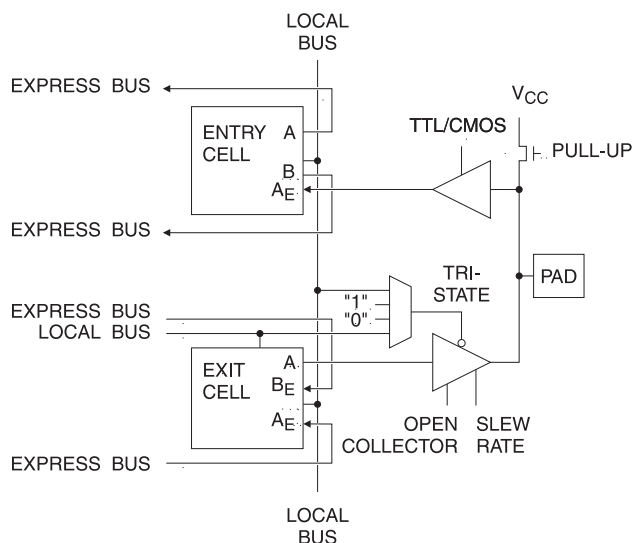
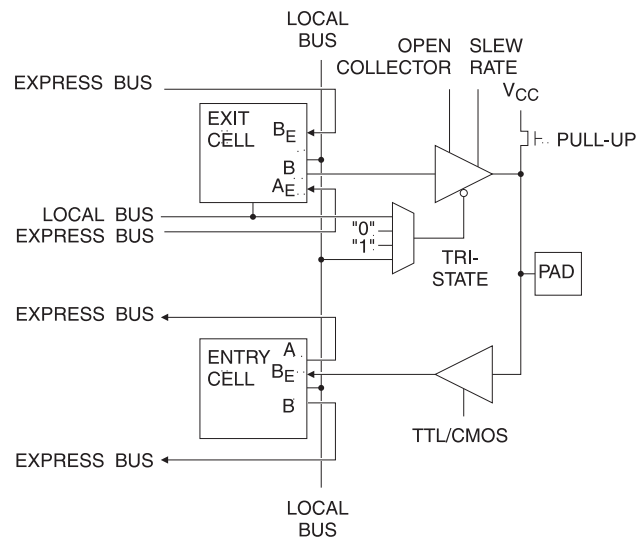


Figure 12. B-type I/O Logic



TTL/CMOS Inputs

A user-configurable bit determines the threshold level – TTL or CMOS – of the input buffer.

Open Collector/Tristate Outputs

A user-configurable bit which enables or disables the active pull-up of the output device.

Slew Rate Control

A user-configurable bit controls the slew rate – fast or slow – of the output buffer. A slow slew rate, which reduces noise and ground bounce, is recommended for outputs that are not speed-critical. Fast and slow slew rates have the same DC-current sinking capabilities, but the rate at which each allows the output devices to reach full drive differs.

Pull-up

A user-configurable bit controls the pull-up transistor in the I/O pin. It's primary function is to provide a logical "1" to unused input pins. When on, it is approximately equivalent to a 25K resistor to V_{CC} .

Enable Select

User-configurable bits determine the output-enable for the output driver. The output driver can be static – always on or always off – or dynamically controlled by a signal generated in the array. Four options are available from the array: (1) the control is low and always driving; (2) the control is high and never driving; (3) the control is connected to a vertical local bus associated with the output cell; or (4) the control is connected to a horizontal local bus associated with the output cell. On power-up, the user I/Os are configured as inputs with pull-up resistors.

In addition to the functionality provided by the I/O logic, the entrance and exit cells provide the ability to register both inputs and outputs. Also, these perimeter cells (unlike interior cells) are connected directly to express buses: the edge-facing A and B outputs of the entrance cell are connected to express buses, as are the edge-facing A and B inputs of the exit cell. These buses are perpendicular to the edge, and provide a rapid means of bringing I/O signals to and from the array interior and the opposite edge of the chip.

Chip Configuration


The Integrated Development System generates the SRAM bit pattern required to configure a AT6000 Series device. A PC parallel port, microprocessor, EPROM or serial configuration memory can be used to download configuration patterns.

Users select from several configuration modes. Many factors, including board area, configuration speed and the number of designs implemented in parallel can influence the user's final choice.

Configuration is controlled by dedicated configuration pins and dual-function pins that double as I/O pins when the device is in operation. The number of dual-function pins required for each mode varies.

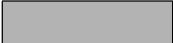
Pinout Assignment

| Left Side (Top to Bottom) | | | | | | | | | | |
|---------------------------|-----------------------|----------------|----------------|---------------------------|-------------|----------------------------|-------------|----------------------------|----------------------------|----------------------------|
| AT6002 ⁽³⁾ | AT6003 ⁽³⁾ | AT6005 | AT6010 | 84 ⁽³⁾ PLCC | 100 VQFP | 132 ⁽³⁾ PQFP | 144 TQFP | 180 ⁽³⁾ CPGA | 208 ⁽³⁾ PQFP | 240 ⁽³⁾ PQFP |
| - | - | - | I/O51(A) | - | - | - | - | B1 | 1 | 1 |
| I/O24(A) or A7 | I/O30(A) or A7 | I/O27(A) or A7 | I/O50(A) or A7 | 12 | 1 | 18 | 1 | C1 | 2 | 2 |
| - | I/O29(B) | - | I/O49(A) | - | - | - | 2 | D1 | 3 | 3 |
| - | - | - | I/O48(B) | - | - | - | - | - | - | 4 |
| - | - | - | VCC | - | - | - | - | PWR ⁽¹⁾ | 4 | 5 |
| - | - | - | I/O47(A) | - | - | - | - | E1 | 5 | 6 |
| - | - | - | GND | - | - | - | - | GND ⁽²⁾ | 6 | 7 |
| - | I/O28(A) | I/O26(A) | I/O46(A) | - | - | 19 | 3 | G1 | 7 | 8 |
| I/O23(A) or A6 | I/O27(A) or A6 | I/O25(A) or A6 | I/O45(A) or A6 | 13 | 2 | 20 | 4 | H1 | 8 | 9 |
| - | - | - | I/O44(B) | - | - | - | - | - | - | 10 |
| - | - | - | I/O43(A) | - | - | - | - | C2 | 9 | 11 |
| I/O22(B) | I/O26(A) | I/O24(A) | I/O42(A) | - | - | 21 | 5 | D2 | 10 | 12 |
| I/O21(A) or A5 | I/O25(A) or A5 | I/O23(A) or A5 | I/O41(A) or A5 | 14 | 3 | 22 | 6 | E2 | 11 | 13 |
| - | - | - | I/O40(B) | - | - | - | - | - | - | 14 |
| - | - | - | I/O39(A) | - | - | - | - | F2 | 12 | 15 |
| I/O20(B) | I/O24(B) | I/O22(A) | I/O38(A) | - | 4 | 23 | 7 | G2 | 13 | 16 |
| I/O19(A) or A4 | I/O23(A) or A4 | I/O21(A) or A4 | I/O37(A) or A4 | 15 | 5 | 24 | 8 | H2 | 14 | 17 |
| - | - | - | I/O36(B) | - | - | - | - | - | - | 18 |
| I/O18(B) | I/O22(B) | I/O20(A) | I/O35(A) | - | - | 25 | 9 | D3 | 15 | 19 |
| I/O17(A) or A3 | I/O21(A) or A3 | I/O19(A) or A3 | I/O34(A) or A3 | 16 | 6 | 26 | 10 | E3 | 16 | 20 |
| I/O16(B) | I/O20(B) | I/O18(A) | I/O33(A) | - | 7 | 27 | 11 | F3 | 17 | 21 |
| - | - | - | I/O32(B) | - | - | - | - | - | 18 | 22 |
| I/O15(A) or A2 | I/O19(A) or A2 | I/O17(A) or A2 | I/O31(A) or A2 | 17 | 8 | 28 | 12 | G3 | 19 | 23 |
| - | I/O18(B) | I/O16(A) | I/O30(A) | - | - | 29 | 13 | H3 | 20 | 24 |
| GND | GND | GND | GND | 18 | 9 | 30 | 14 | GND ⁽²⁾ | 21 | 25 |
| VSS | VSS | VSS | VSS | 19 | 10 | 31 | 15 | GND ⁽²⁾ | 22 | 26 |
| I/O14(A) or A1 | I/O17(A) or A1 | I/O15(A) or A1 | I/O29(A) or A1 | 20 | 11 | 32 | 16 | F4 | 23 | 27 |
| - | - | - | I/O28(B) | - | - | - | - | - | 24 | 28 |
| - | I/O16(B) | - | I/O27(A) | - | - | - | 17 | G4 | 25 | 29 |
| I/O13(A) or A0 | I/O15(A) or A0 | I/O14(A) or A0 | I/O26(A) or A0 | 21 | 12 | 33 | 18 | H4 | 26 | 30 |
| I/O12(B) or D7 | I/O14(A) or D7 | I/O13(A) or D7 | I/O25(B) or D7 | 22 | 13 | 34 | 19 | H5 | 27 | 31 |
| - | - | - | I/O24(B) | - | - | - | - | - | 28 | 32 |
| I/O11(A) or D6 | I/O13(A) or D6 | I/O12(A) or D6 | I/O23(A) or D6 | 23 | 14 | 35 | 20 | J4 | 29 | 33 |

- Notes:
1. PWR = Pins connected to power plane = F1, E4/E5, L2, R4, K15, L12, E14, A12.
 2. GND = Pins connected to ground plane = L4, M4, N9, N10, E12, D12, C7, C6.
 3.  Obsolete. Not recommended for new design.

Pinout Assignment (Continued)

| Left Side (Top to Bottom) | | | | | | | | | | |
|---------------------------|-----------------------|----------------|----------------|---------------------------|-------------|----------------------------|-------------|----------------------------|----------------------------|----------------------------|
| AT6002 ⁽³⁾ | AT6003 ⁽³⁾ | AT6005 | AT6010 | 84 ⁽³⁾ PLCC | 100 VQFP | 132 ⁽³⁾ PQFP | 144 TQFP | 180 ⁽³⁾ CPGA | 208 ⁽³⁾ PQFP | 240 ⁽³⁾ PQFP |
| I/O10(A) or D5 | I/O12(A) or D5 | I/O11(A) or D5 | I/O22(A) or D5 | 24 | 15 | 36 | 21 | K4 | 30 | 34 |
| VDD | VDD | VDD | VDD | 25 | 16 | 37 | 22 | PWR ⁽¹⁾ | 31 | 35 |
| VCC | VCC | VCC | VCC | 26 | 17 | 38 | 23 | PWR ⁽¹⁾ | 32 | 36 |
| I/O9(B) | I/O11(B) | I/O10(A) | I/O21(A) | - | - | 39 | 24 | J3 | 33 | 37 |
| - | - | - | I/O20(B) | - | - | - | - | - | 34 | 38 |
| I/O8(A) or D4 | I/O10(A) or D4 | I/O9(A) or D4 | I/O19(A) or D4 | 27 | 18 | 40 | 25 | K3 | 35 | 39 |
| I/O7(B) | I/O9(B) | I/O8(A) | I/O18(A) | - | 19 | 41 | 26 | L3 | 36 | 40 |
| - | - | - | I/O17(A) | - | - | - | - | M3 | 37 | 41 |
| - | - | - | I/O16(B) | - | - | - | - | - | - | 42 |
| I/O6(A) or D3 | I/O8(A) or D3 | I/O7(A) or D3 | I/O15(A) or D3 | 28 | 20 | 42 | 27 | N3 | 38 | 43 |
| - | I/O7(B) | I/O6(A) | I/O14(A) | - | - | 43 | 28 | J2 | 39 | 44 |
| - | - | - | I/O13(A) | - | - | - | - | K2 | 40 | 45 |
| GND | GND | GND | GND | - | - | 44 | 29 | GND ⁽²⁾ | 41 | 46 |
| - | - | - | VSS | - | - | - | - | GND ⁽²⁾ | 42 | 47 |
| - | - | - | I/O12(B) | - | - | - | - | - | - | 48 |
| I/O5(A) or D2 | I/O6(A) or D2 | I/O5(A) or D2 | I/O11(A) or D2 | 29 | 21 | 45 | 30 | M2 | 43 | 49 |
| I/O4(B) | I/O5(B) | I/O4(A) | I/O10(A) | - | 22 | 46 | 31 | N2 | 44 | 50 |
| - | - | - | I/O9(A) | - | - | - | - | P2 | 45 | 51 |
| - | - | - | I/O8(B) | - | - | - | - | - | - | 52 |
| I/O3(A) or D1 | I/O4(A) or D1 | I/O3(A) or D1 | I/O7(A) or D1 | 30 | 23 | 47 | 32 | J1 | 46 | 53 |
| I/O2(B) | I/O3(A) | I/O2(A) | I/O6(A) | - | - | 48 | 33 | K1 | 47 | 54 |
| - | - | - | I/O5(A) | - | - | - | - | L1 | 48 | 55 |
| - | - | - | I/O4(B) | - | - | - | - | - | - | 56 |
| - | I/O2(B) | - | I/O3(A) | - | - | - | 34 | M1 | 49 | 57 |
| I/O1(A) or D0 | I/O1(A) or D0 | I/O1(A) or D0 | I/O2(A) or D0 | 31 | 24 | 49 | 35 | N1 | 50 | 58 |
| - | - | - | I/O1(A) | - | - | - | - | P1 | 51 | 59 |
| CCLK | CCLK | CCLK | CCLK | 32 | 25 | 50 | 36 | R1 | 52 | 60 |


- Notes:
1. PWR = Pins connected to power plane = F1, E4/E5, L2, R4, K15, L12, E14, A12.
 2. GND = Pins connected to ground plane = L4, M4, N9, N10, E12, D12, C7, C6.
 3.  Obsolete. Not recommended for new design.

Pinout Assignment

| Bottom Side (Left to Right) | | | | | | | | | | |
|-----------------------------|-----------------------|-----------------------|-----------------------|---------------------------|-------------|----------------------------|-------------|----------------------------|----------------------------|----------------------------|
| AT6002 ⁽³⁾ | AT6003 ⁽³⁾ | AT6005 | AT6010 | 84 ⁽³⁾ PLCC | 100 VQFP | 132 ⁽³⁾ PQFP | 144 TQFP | 180 ⁽³⁾ CPGA | 208 ⁽³⁾ PQFP | 240 ⁽³⁾ PQFP |
| CON | CON | CON | CON | 33 | 26 | 51 | 37 | M5 | 53 | 61 |
| - | - | - | I/O204(A) | - | - | - | - | M6 | 54 | 62 |
| I/O96(A) | I/O120(A) | I/O108(A) | I/O203(A) | 34 | 27 | 52 | 38 | M7 | 55 | 63 |
| - | I/O119(B) | - | I/O202(A) | - | - | - | 39 | R2 | 56 | 64 |
| - | - | - | I/O201(B) | - | - | - | - | - | - | 65 |
| - | - | - | VCC | - | - | - | - | PWR ⁽¹⁾ | 57 | 66 |
| - | - | - | I/O200(A) | - | - | - | - | R3 | 58 | 67 |
| - | - | - | GND | - | - | - | - | GND ⁽²⁾ | 59 | 68 |
| - | I/O118(A) | I/O107(A) | I/O199(A) | - | - | 53 | 40 | R5 | 60 | 69 |
| I/O95(A) or CSOUT | I/O117(A) or CSOUT | I/O106(A) or CSOUT | I/O198(A) or CSOUT | 35 | 28 | 54 | 41 | R6 | 61 | 70 |
| - | - | - | I/O197(B) | - | - | - | - | - | - | 71 |
| - | - | - | I/O196(A) | - | - | - | - | R7 | 62 | 72 |
| I/O94(B) | I/O116(A) | I/O105(A) | I/O195(A) | - | - | 55 | 42 | P3 | 63 | 73 |
| I/O93(A) | I/O115(A) | I/O104(A) | I/O194(A) | 36 | 29 | 56 | 43 | P4 | 64 | 74 |
| - | - | - | I/O193(B) | - | - | - | - | - | - | 75 |
| - | - | - | I/O192(A) | - | - | - | - | P5 | 65 | 76 |
| I/O92(B) | I/O114(B) | I/O103(A) | I/O191(A) | - | 30 | 57 | 44 | P6 | 66 | 77 |
| I/O91(A) or CHECK | I/O113(A) or CHECK | I/O102(A) or CHECK | I/O190(A) or CHECK | 37 | 31 | 58 | 45 | P7 | 67 | 78 |
| - | - | - | I/O189(B) | - | - | - | - | - | - | 79 |
| I/O90(B) | I/O112(B) | I/O101(A) | I/O188(A) | - | - | 59 | 46 | N4 | 68 | 80 |
| I/O89(A) or ERR | I/O111(A) or ERR | I/O100(A) or ERR | I/O187(A) or ERR | 38 | 32 | 60 | 47 | N5 | 69 | 81 |
| I/O88(B) | I/O110(B) | I/O99(A) | I/O186(A) | - | 33 | 61 | 48 | N6 | 70 | 82 |
| - | - | - | I/O185(B) | - | - | - | - | - | 71 | 83 |
| I/O87(A) | I/O109(A) | I/O98(A) | I/O184(A) | 39 | 34 | 62 | 49 | N7 | 72 | 84 |
| - | I/O108(B) | I/O97(A) | I/O183(A) | - | - | 63 | 50 | M8 | 73 | 85 |
| GND | GND | GND | GND | 40 | 35 | 64 | 51 | GND ⁽²⁾ | 74 | 86 |
| I/O86(A) | I/O107(A) | I/O96(A) | I/O182(A) | 41 | 36 | 65 | 52 | M9 | 75 | 87 |
| - | - | - | I/O181(B) | - | - | - | - | - | 76 | 88 |
| - | I/O106(B) | - | I/O180(A) | - | - | - | 53 | M10 | 77 | 89 |
| I/O85(A) | I/O105(A) | I/O95(A) | I/O179(A) | 42 | 37 | 66 | 54 | M11 | 78 | 90 |
| CS | CS | CS | CS | 43 | 38 | 67 | 55 | L8 | 79 | 91 |
| I/O84(B) | I/O104(A) | I/O94(A) | I/O178(A) | 44 | 39 | 68 | 56 | M12 | 80 | 92 |

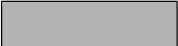
Notes: 1. PWR = Pins connected to power plane = F1, E4/E5, L2, R4, K15, L12, E14, A12.

2. GND = Pins connected to ground plane = L4, M4, N9, N10, E12, D12, C7, C6.

3.  Obsolete. Not recommended for new design.

Pinout Assignment (Continued)

| Right Side (Bottom to Top) | | | | | | | | | | |
|----------------------------|-----------------------|----------|-----------|---------------------------|-------------|----------------------------|-------------|----------------------------|----------------------------|----------------------------|
| AT6002 ⁽⁵⁾ | AT6003 ⁽⁵⁾ | AT6005 | AT6010 | 84 ⁽⁵⁾ PLCC | 100 VQFP | 132 ⁽⁵⁾ PQFP | 144 TQFP | 180 ⁽⁵⁾ CPGA | 208 ⁽⁵⁾ PQFP | 240 ⁽⁵⁾ PQFP |
| I/O59(A) | I/O73(A) | I/O66(A) | I/O125(A) | 65 | 64 | 101 | 92 | G12 | 133 | 153 |
| I/O58(A) | I/O72(A) | I/O65(A) | I/O124(A) | 66 | 65 | 102 | 93 | F12 | 134 | 154 |
| VDD | VDD | VDD | VDD | 67 | 66 | 103 | 94 | PWR ⁽¹⁾ | 135 | 155 |
| VCC | VCC | VCC | VCC | 68 | 67 | 104 | 95 | PWR ⁽¹⁾ | 136 | 156 |
| I/O57(B) | I/O71(B) | I/O64(A) | I/O123(A) | - | - | 105 | 96 | G13 | 137 | 157 |
| - | - | - | I/O122(B) | - | - | - | - | - | 138 | 158 |
| I/O56(A) | I/O70(A) | I/O63(A) | I/O121(A) | 69 | 68 | 106 | 97 | F13 | 139 | 159 |
| I/O55(B) | I/O69(B) | I/O62(A) | I/O120(A) | - | 69 | 107 | 98 | E13 | 140 | 160 |
| - | - | - | I/O119(A) | - | - | - | - | D13 | 141 | 161 |
| - | - | - | I/O118(B) | - | - | - | - | - | - | 162 |
| I/O54(A) | I/O68(A) | I/O61(A) | I/O117(A) | 70 | 70 | 108 | 99 | C13 | 142 | 163 |
| - | I/O67(B) | I/O60(A) | I/O116(A) | - | - | 109 | 100 | G14 | 143 | 164 |
| - | - | - | I/O115(A) | - | - | - | - | F14 | 144 | 165 |
| GND | GND | GND | GND | - | - | 110 | 101 | GND ⁽²⁾ | 145 | 166 |
| - | - | - | VSS | - | - | - | - | GND ⁽²⁾ | 146 | 167 |
| - | - | - | I/O114(B) | - | - | - | - | - | - | 168 |
| I/O53(A) | I/O66(A) | I/O59(A) | I/O113(A) | 71 | 71 | 111 | 102 | D14 | 147 | 169 |
| I/O52(B) | I/O65(B) | I/O58(A) | I/O112(A) | - | 72 | 112 | 103 | C14 | 148 | 170 |
| - | - | - | I/O111(A) | - | - | - | - | B14 | 149 | 171 |
| - | - | - | I/O110(B) | - | - | - | - | - | - | 172 |
| I/O51(A) | I/O64(A) | I/O57(A) | I/O109(A) | 72 | 73 | 113 | 104 | G15 | 150 | 173 |
| I/O50(B) | I/O63(A) | I/O56(A) | I/O108(A) | - | - | 114 | 105 | F15 | 151 | 174 |
| - | - | - | I/O107(A) | - | - | - | - | E15 | 152 | 175 |
| - | - | - | I/O106(B) | - | - | - | - | - | - | 176 |
| - | I/O62(B) | - | I/O105(A) | - | - | - | 106 | D15 | 153 | 177 |
| I/O49(A) | I/O61(A) | I/O55(A) | I/O104(A) | 73 | 74 | 115 | 107 | C15 | 154 | 178' |
| - | - | - | I/O103(A) | - | - | - | - | B15 | 155 | 179 |
| M2 | M2 | M2 | M2 | 74 | 75 | 116 | 108 | A15 | 156 | 180 |

- Notes:
1. PWR = Pins connected to power plane = F1, E4/E5, L2, R4, K15, L12, E14, A12.
 2. GND = Pins connected to ground plane = L4, M4, N9, N10, E12, D12, C7, C6.
 3. 85 = Pin 85 on AT6005.
 4. 85 = Pin 85 on AT6003 and AT6010.
 5.  Obsolete. Not recommended for new design.

Pinout Assignment

| Top Side (Right to Left) | | | | | | | | | | |
|--------------------------|-----------------------|-----------------|-----------------|---------------------------|-------------|----------------------------|-------------|----------------------------|----------------------------|----------------------------|
| AT6002 ⁽³⁾ | AT6003 ⁽³⁾ | AT6005 | AT6010 | 84 ⁽³⁾ PLCC | 100 VQFP | 132 ⁽³⁾ PQFP | 144 TQFP | 180 ⁽³⁾ CPGA | 208 ⁽³⁾ PQFP | 240 ⁽³⁾ PQFP |
| M1 | M1 | M1 | M1 | 75 | 76 | 117 | 109 | D11 | 157 | 181 |
| - | - | - | I/O102(A) | - | - | - | - | D10 | 158 | 182 |
| I/O48(A) | I/O60(A) | I/O54(A) | I/O101(A) | 76 | 77 | 118 | 110 | D9 | 159 | 183 |
| - | I/O59(B) | - | I/O100(A) | - | - | - | 111 | A14 | 160 | 184 |
| - | - | - | I/O99(B) | - | - | - | - | - | - | 185 |
| - | - | - | VCC | - | - | - | - | PWR ⁽¹⁾ | 161 | 186 |
| - | - | - | I/O98(A) | - | - | - | - | A13 | 162 | 187 |
| - | - | - | GND | - | - | - | - | GND ⁽²⁾ | 163 | 188 |
| - | I/O58(A) | I/O53(A) | I/O97(A) | - | - | 119 | 112 | A11 | 164 | 189 |
| I/O47(A) | I/O57(A) | I/O52(A) | I/O96(A) | 77 | 78 | 120 | 113 | A10 | 165 | 190 |
| - | - | - | I/O95(B) | - | - | - | - | - | - | 191 |
| - | - | - | I/O94(A) | - | - | - | - | A9 | 166 | 192 |
| I/O46(B) | I/O56(A) | I/O51(A) | I/O93(A) | - | - | 121 | 114 | B13 | 167 | 193 |
| I/O45(A) | I/O55(A) | I/O50(A) | I/O92(A) | 78 | 79 | 122 | 115 | B12 | 168 | 194 |
| - | - | - | I/O91(B) | - | - | - | - | - | - | 195 |
| - | - | - | I/O90(A) | - | - | - | - | B11 | 169 | 196 |
| I/O44(B) | I/O54(B) | I/O49(A) | I/O89(A) | - | 80 | 123 | 116 | B10 | 170 | 197 |
| I/O43(A) | I/O53(A) | I/O48(A) | I/O88(A) | 79 | 81 | 124 | 117 | B9 | 171 | 198 |
| - | - | - | I/O87(B) | - | - | - | - | - | - | 199 |
| I/O42(B) | I/O52(B) | I/O47(A) | I/O86(A) | - | - | 125 | 118 | C12 | 172 | 200 |
| I/O41(A) | I/O51(A) | I/O46(A) | I/O85(A) | 80 | 82 | 126 | 119 | C11 | 173 | 201 |
| I/O40(B) | I/O50(B) | I/O45(A) | I/O84(A) | - | 83 | 127 | 120 | C10 | 174 | 202 |
| - | - | - | I/O83(B) | - | - | - | - | - | 175 | 203 |
| I/O39(A) | I/O49(A) | I/O44(A) | I/O82(A) | 81 | 84 | 128 | 121 | C9 | 176 | 204 |
| - | I/O48(B) | I/O43(A) | I/O81(A) | - | - | 129 | 122 | D8 | 177 | 205 |
| GND | GND | GND | GND | 82 | 85 | 130 | 123 | GND ⁽²⁾ | 178 | 206 |
| I/O38(A) | I/O47(A) | I/O42(A) | I/O80(A) | 83 | 86 | 131 | 124 | D7 | 179 | 207 |
| - | - | - | I/O79(B) | - | - | - | - | - | 180 | 208 |
| - | I/O46(B) | - | I/O78(A) | - | - | - | 125 | D6 | 181 | 209 |
| I/O37(A) or A16 | I/O45(A) or A16 | I/O41(A) or A16 | I/O77(A) or A16 | 84 | 87 | 132 | 126 | D5 | 182 | 210 |
| CLOCK | CLOCK | CLOCK | CLOCK | 1 | 88 | 1 | 127 | E8 | 183 | 211 |
| I/O36(B) or A15 | I/O44(B) or A15 | I/O40(A) or A15 | I/O76(A) or A15 | 2 | 89 | 2 | 128 | D4 | 184 | 212 |

Notes: 1. PWR = Pins connected to power plane = F1, E4/E5, L2, R4, K15, L12, E14, A12.

2. GND = Pins connected to ground plane = L4, M4, N9, N10, E12, D12, C7, C6.

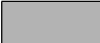
3.  Obsolete. Not recommended for new design.

AC Timing Characteristics – 3.3V Operation ⁽⁸⁾

Delays are based on fixed load. Loads for each type of device are described in the notes. Delays are in nanoseconds. Worst case: $V_{CC} = 3.0V$ to $3.6V$. Temperature = $0^{\circ}C$ to $70^{\circ}C$.

| Cell Function | Parameter | From | To | Load Definition ⁽⁷⁾ | -4 | Units |
|-------------------------------|----------------------|-------------|---------|--------------------------------|------|-------|
| Wire ⁽⁴⁾ | $t_{PD} (max)^{(4)}$ | A, B, L | A, B | 1 | 1.8 | ns |
| NAND | $t_{PD} (max)$ | A, B, L | B | 1 | 3.2 | ns |
| XOR | $t_{PD} (max)$ | A, B, L | A | 1 | 4.0 | ns |
| AND | $t_{PD} (max)$ | A, B, L | B | 1 | 3.2 | ns |
| MUX | $t_{PD} (max)$ | A, B | A | 1 | 4.0 | ns |
| | | L | A | 1 | 4.9 | ns |
| D-Flip-flop ⁽⁵⁾ | $t_{setup} (min)$ | A, B, L | CLK | - | 3.0 | ns |
| D-Flip-flop ⁽⁵⁾ | $t_{hold} (min)$ | CLK | A, B, L | - | 0 | ns |
| D-Flip-flop | $t_{PD} (max)$ | CLK | A | 1 | 3.0 | ns |
| Bus Driver | $t_{PD} (max)$ | A | L | 2 | 4.0 | ns |
| Repeater | $t_{PD} (max)$ | L, E | E | 3 | 2.3 | ns |
| | | L, E | L | 2 | 3.0 | ns |
| Column Clock | $t_{PD} (max)$ | GCLK, A, ES | CLK | 3 | 3.0 | ns |
| Column Reset | $t_{PD} (max)$ | GRES, A, EN | RES | 3 | 3.0 | ns |
| Clock Buffer ⁽⁵⁾ | $t_{PD} (max)$ | CLOCK PIN | GCLK | 4 | 2.9 | ns |
| Reset Buffer ⁽⁵⁾ | $t_{PD} (max)$ | RESET PIN | GRES | 5 | 2.8 | ns |
| TTL Input ⁽¹⁾ | $t_{PD} (max)$ | I/O | A | 3 | 1.5 | ns |
| CMOS Input ⁽²⁾ | $t_{PD} (max)$ | I/O | A | 3 | 2.3 | ns |
| Fast Output ⁽³⁾ | $t_{PD} (max)$ | A | I/O PIN | 6 | 6.0 | ns |
| Slow Output ⁽³⁾ | $t_{PD} (max)$ | A | I/O PIN | 6 | 12.0 | ns |
| Output Disable ⁽⁵⁾ | $t_{PXZ} (max)$ | L | I/O PIN | 6 | 5.5 | ns |
| Fast Enable ⁽³⁾⁽⁵⁾ | $t_{PXZ} (max)$ | L | I/O PIN | 6 | 6.5 | ns |
| Slow Enable ⁽³⁾⁽⁵⁾ | $t_{PXZ} (max)$ | L | I/O PIN | 6 | 12.5 | ns |

| Device | Cell Types | Outputs | $I_{CC} (max)$ |
|-----------------------------|--|---------|-----------------|
| Cell ⁽⁶⁾ | Wire, XWire, Half-adder, Flip-flop | A, B | 2.3 $\mu A/MHz$ |
| Bus ⁽⁶⁾ | Wire, XWire, Half-adder, Flip-flop, Repeater | L | 1.3 $\mu A/MHz$ |
| Column Clock ⁽⁶⁾ | Column Clock Driver | CLK | 20 $\mu A/MHz$ |

- Notes:
1. TTL buffer delays are measured from a V_{IH} of 1.5V at the pad to the internal V_{IH} at A. The input buffer load is constant.
 2. CMOS buffer delays are measured from a V_{IH} of 1/2 V_{CC} at the pad to the internal V_{IH} at A. The input buffer load is constant.
 3. Buffer delay is to a pad voltage of 1.5V with one output switching.
 4. Max specifications are the average of t_{PDLH} and t_{PDHL} .
 5. Parameter based on characterization and simulation; not tested in production
 6. Exact power calculation is available in an Atmel application note.
 7. Load Definition: 1 = Load of one A or B input; 2 = Load of one L input; 3 = Constant Load; 4 = Load of 28 Clock Columns; 5 = Load of 28 Reset Columns; 6 = Tester Load of 50 pF.
 8.  Obsolete. Not recommended for new design.

Absolute Maximum Ratings*

| | |
|--|--------------------------|
| Supply Voltage (V_{CC}) | -0.5V to + 7.0V |
| DC Input Voltage (V_{IN}) | -0.5V to $V_{CC} + 0.5V$ |
| DC Output Voltage (V_{ON}) | -0.5V to $V_{CC} + 0.5V$ |
| Storage Temperature Range (TSTG) | -65°C to +150°C |
| Power Dissipation (PD) | 1500 mW |
| Lead Temperature (T_L) (Soldering, 10 sec.) | 260°C |
| ESD ($R_{ZAP} = 1.5K$, $C_{ZAP} = 100$ pF) | 2000V |

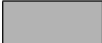
***NOTICE:** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress rating only and functional operation of the device at these or any other conditions beyond those listed under operating conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

DC and AC Operating Range – 5V Operation

| | | AT6002-2/4 ⁽¹⁾ AT6003-2/4 ⁽¹⁾ AT6005-2/4 ⁽¹⁾ AT6010-2/4 ⁽¹⁾ Commercial ⁽¹⁾ | AT6002-2/4 ⁽¹⁾ AT6003-2/4 ⁽¹⁾ AT6005-2/4 ⁽¹⁾ AT6010-2/4 ⁽¹⁾ Industrial | AT6002-2/4 ⁽¹⁾ AT6003-2/4 ⁽¹⁾ AT6005-2/4 ⁽¹⁾ AT6010-2/4 ⁽¹⁾ Military ⁽¹⁾ |
|---|--------------------|---|--|---|
| Operating Temperature (Case) | | 0°C - 70°C | -40°C - 85°C | -55°C - 125°C |
| V_{CC} Power Supply | | 5V ± 5% | 5V ± 10% | 5V ± 10% |
| Input Voltage Level (TTL) | High (V_{IHT}) | 2.0V - V_{CC} | 2.0V - V_{CC} | 2.0V - V_{CC} |
| | Low (V_{ILT}) | 0V - 0.8V | 0V - 0.8V | 0V - 0.8V |
| Input Voltage Level (CMOS) | High (V_{IHC}) | 70% - 100% V_{CC} | 70% - 100% V_{CC} | 70% - 100% V_{CC} |
| | Low (V_{ILC}) | 0 - 30% V_{CC} | 0 - 30% V_{CC} | 0 - 30% V_{CC} |
| Input Signal Transition Time (T_{IN}) | | 50 ns (max) | 50 ns (max) | 50 ns (max) |


DC and AC Operating Range – 3.3V Operation⁽¹⁾

| | | AT6002-2/4 ⁽¹⁾ , AT6003-2/4 ⁽¹⁾ AT6005-2/4 ⁽¹⁾ , AT6010-2/4 ⁽¹⁾ Commercial |
|---|--------------------|--|
| Operating Temperature (Case) | | 0°C - 70°C |
| V_{CC} Power Supply | | 3.3V ± 5% |
| Input Voltage Level (TTL) | High (V_{IHT}) | 2.0V - V_{CC} |
| | Low (V_{ILT}) | 0V - 0.8V |
| Input Voltage Level (CMOS) | High (V_{IHC}) | 70% - 100% V_{CC} |
| | Low (V_{ILC}) | 0 - 30% V_{CC} |
| Input Signal Transition Time (T_{IN}) | | 50 ns (max) |

Note: 1.  Obsolete. Not recommended for new design.

DC Characteristics – 5V Operation

| Symbol | Parameter | Conditions | | Min | Max | Units |
|------------------|---------------------------|--|---|---------------------|---------------------|-------|
| V _{IH} | High-level Input Voltage | Commercial | CMOS | 70% V _{CC} | V _{CC} | V |
| | | | TTL | 2.0 | V _{CC} | V |
| V _{IL} | Low-level Input Voltage | Commercial | CMOS | 0 | 30% V _{CC} | V |
| | | | TTL | 0 | 0.8 | V |
| V _{OH} | High-level Output Voltage | Commercial | I _{OH} = -4 mA, V _{CC} min | 3.9 | | V |
| | | | I _{OH} = -16 mA, V _{CC} min | 3.0 | | V |
| V _{OL} | Low-level Output Voltage | Commercial | I _{OL} = 4 mA, V _{CC} min | | 0.4 | V |
| | | | I _{OL} = 16 mA, V _{CC} min | | 0.5 | V |
| I _{OZH} | High-level Tristate | V _O = V _{CC} (max) | | | 10 | μA |
| | Output Leakage Current | | | | | |
| I _{OZL} | High-level Tristate | Without Pull-up, V _O = V _{SS} | | -10 | | μA |
| | Output Leakage Current | With Pull-up, V _O = V _{SS} | | -500 | | μA |
| I _{IH} | High-level Input Current | V _{IN} = V _{CC} (max) | | | 10 | μA |
| I _{IL} | Low-level Input Current | Without Pull-up, V _{IN} = V _{SS} | | -10 | | μA |
| | | With Pull-up, V _{IN} = V _{SS} | | -500 | | μA |
| I _{CC} | Power Consumption | Without Internal Oscillator (Standby) | | | 500 | μA |
| C _{IN} | Input Capacitance | All Pins | | | 10 | pF |

Note: 1.  Obsolete. Not recommended for new design.

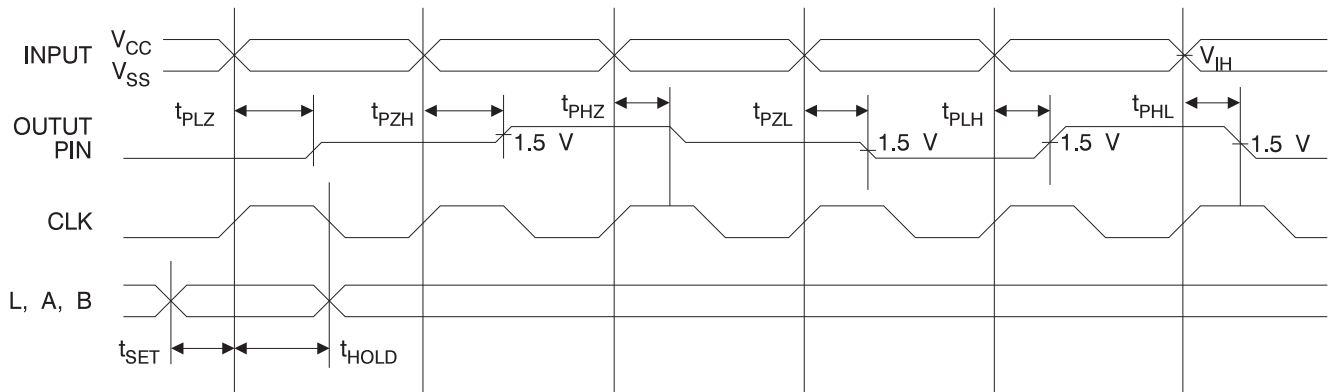
DC Characteristics – 3.3V Operation⁽²⁾

| Symbol | Parameter | Conditions | Min | Max | Units |
|----------------|---------------------------|---------------------------------------|--|--------------|---------------|
| V_{IH} | High-level Input Voltage | Commercial | CMOS | 70% V_{CC} | V |
| | | | TTL | 2.0 | V |
| V_{IL} | Low-level Input Voltage | Commercial | CMOS | 0 | 30% V_{CC} |
| | | | TTL | 0 | 0.8 |
| V_{OH} | High-level Output Voltage | Commercial | $I_{OH} = -2 \text{ mA}, V_{CC} \text{ min}$ | 2.4 | V |
| | | | $I_{OH} = -6 \text{ mA}, V_{CC} \text{ min}$ | 2.0 | V |
| V_{OL} | Low-level Output Voltage | Commercial | $I_{OL} = +2 \text{ mA}, V_{CC} \text{ min}$ | 0.4 | V |
| | | | $I_{OL} = +6 \text{ mA}, V_{CC} \text{ min}$ | 0.5 | V |
| I_{OZH} | High-level Tristate | $V_O = V_{CC} \text{ (max)}$ | | 10 | μA |
| | Output Leakage Current | | | | |
| I_{OZL} | High-level Tristate | Without Pull-up, $V_O = V_{SS}$ | -10 | | μA |
| | Output Leakage Current | With Pull-up, $V_O = V_{SS}$ | -500 | | μA |
| I_{IH} | High-level Input Current | $V_{IN} = V_{CC} \text{ (max)}$ | | 10 | μA |
| I_{IL} | Low-level Input Current | Without Pull-up, $V_{IN} = V_{SS}$ | -10 | | μA |
| | | With Pull-up, $V_{IN} = V_{SS}$ | -500 | | μA |
| I_{CC} | Power Consumption | Without Internal Oscillator (Standby) | | 200 | μA |
| $C_{IN}^{(1)}$ | Input Capacitance | All Pins | | 10 | pF |

Notes: 1. Parameter based on characterization and simulation; it is not tested in production.


2. Obsolete. Not recommended for new design.

Device Timing: During Operation



Ordering Information – AT6002⁽¹⁾

| Usable Gates | Speed Grade (ns) | Ordering Code | Package | Operation Range |
|--------------|------------------|---------------|---------|----------------------------------|
| 6,000 | 2 | AT6002-2AC | 100A | 5V Commercial (0°C to 70°C) |
| | | AT6002A-2AC | 144A | |
| | | AT6002-2JC | 84J | |
| | | AT6002-2QC | 132Q | |
| | | AT6002-2AI | 100A | 5V Industrial (-40°C to 85°C) |
| | | AT6002A-2AI | 144A | |
| | | AT6002-2JI | 84J | |
| | | AT6002-2QI | 132Q | |
| 6,000 | 4 | AT6002-4AC | 100A | 5V Commercial (0°C to 70°C) |
| | | AT6002A-4AC | 144A | |
| | | AT6002-4JC | 84J | |
| | | AT6002-4QC | 132Q | |
| | | AT6002LV-4AC | 100A | 3.3V Commercial (0°C to 70°C) |
| | | AT6002ALV-4AC | 144A | |
| | | AT6002LV-4JC | 84J | |
| | | AT6002LV-4QC | 132Q | |
| | | AT6002-4AI | 100A | 5V Industrial (-40°C to 85°C) |
| | | AT6002A-4AI | 144A | |
| | | AT6002-4JI | 84J | |
| | | AT6002-4QI | 132Q | |

Note: 1.  Obsolete. Not recommended for new design.

| Package Type | |
|--------------|---|
| 84J | 84-lead, Plastic J-leaded Chip Carrier (PLCC) |
| 100A | 100-lead, Very Thin (1.0 mm) Plastic Gull-Wing Quad Flat Package (VQFP) |
| 132Q | 132-lead, Bumped Plastic Gull-Wing Quad Flat Package (BQFP) |
| 144A | 144-lead, Thin (1.4 mm) Plastic Gull-Wing Quad Flat Package (TQFP) |
| 208Q | 208-lead, Plastic Gull-Wing Quad Flat Package (PQFP) |
| 240Q | 240-lead, Plastic Gull-Wing Quad Flat Package (PQFP) |

Ordering Information – AT6003⁽¹⁾


| Usable Gates | Speed Grade (ns) | Ordering Code | Package | Operation Range |
|--------------|------------------|---------------|---------|----------------------------------|
| 9,000 | 2 | AT6003-2AC | 100A | 5V Commercial (0°C to 70°C) |
| | | AT6003A-2AC | 144A | |
| | | AT6003-2JC | 84J | |
| | | AT6003-2QC | 132Q | |
| | | AT6003-2AI | 100A | Industrial (-40°C to 85°C) |
| | | AT6003A-2AI | 144A | |
| | | AT6003-2JI | 84J | |
| | | AT6003-2QI | 132Q | |
| 9,000 | 4 | AT6003-4AC | 100A | 5V Commercial (0°C to 70°C) |
| | | AT6003A-4AC | 144A | |
| | | AT6003-4JC | 84J | |
| | | AT6003-4QC | 132Q | |
| | | AT6003LV-4AC | 100A | 3.3V Commercial (0°C to 70°C) |
| | | AT6003ALV-4AC | 144A | |
| | | AT6003LV-4JC | 84J | |
| | | AT6003LV-4QC | 132Q | |
| | | AT6003-4AI | 100A | 5V Industrial (-40°C to 85°C) |
| | | AT6003A-4AI | 144A | |
| | | AT6003-4JI | 84J | |
| | | AT6003-4QI | 132Q | |

Note: 1.  Obsolete. Not recommended for new design.

| Package Type | |
|--------------|---|
| 84J | 84-lead, Plastic J-leaded Chip Carrier (PLCC) |
| 100A | 100-lead, Very Thin (1.0 mm) Plastic Gull-Wing Quad Flat Package (VQFP) |
| 132Q | 132-lead, Bumped Plastic Gull-Wing Quad Flat Package (BQFP) |
| 144A | 144-lead, Thin (1.4 mm) Plastic Gull-Wing Quad Flat Package (TQFP) |
| 208Q | 208-lead, Plastic Gull-Wing Quad Flat Package (PQFP) |
| 240Q | 240-lead, Plastic Gull-Wing Quad Flat Package (PQFP) |

Ordering Information – AT6005

| Usable Gates | Speed Grade (ns) | Ordering Code | Package | Operation Range |
|--------------|------------------|---------------|---------|--|
| 15,000 | 2 | AT6005-2AU | 100A | 5V Industrial Temperature (-40°C to 85°C) |
| 15,000 | 2 | AT6005-2AC | 100A | 5V Commercial (0°C to 70°C) |
| | | AT6005A-2AC | 144A | |
| | | AT6005-2JC | 84J | |
| | | AT6005-2QC | 132Q | |
| | | AT6005A-2QC | 208Q | |
| | | AT6005-2AI | 100A | Industrial (-40°C to 85°C) |
| | | AT6005A-2AI | 144A | |
| | | AT6005-2JI | 84J | |
| | | AT6005-2QI | 132Q | |
| | | AT6005A-2QI | 208Q | |
| 15,000 | 4 | AT6005-4AC | 100A | 5V Commercial (0°C to 70°C) |
| | | AT6005A-4AC | 144A | |
| | | AT6005-4JC | 84J | |
| | | AT6005-4QC | 132Q | |
| | | AT6005A-4QC | 208Q | |
| | | AT6005LV-4AC | 100A | 3.3V Commercial (0°C to 70°C) |
| | | AT6005ALV-4AC | 144A | |
| | | AT6005LV-4JC | 84J | |
| | | AT6005LV-4QC | 132Q | |
| | | AT6005ALV-4QC | 208Q | |
| | | AT6005-4AI | 100A | 5V Commercial (-40°C to 85°C) |
| | | AT6005A-4AI | 144A | |
| | | AT6005-4JI | 84J | |
| | | AT6005-4QI | 132Q | |
| | | AT6005A-4QI | 208Q | |

Note: 1  Obsolete. Package options are not recommended for new design.

| Package Type | |
|--------------|---|
| 84J | 84-lead, Plastic J-leaded Chip Carrier (PLCC) |
| 100A | 100-lead, Very Thin (1.0 mm) Plastic Gull-Wing Quad Flat Package (VQFP) |
| 132Q | 132-lead, Bumped Plastic Gull-Wing Quad Flat Package (BQFP) |
| 144A | 144-lead, Thin (1.4 mm) Plastic Gull-Wing Quad Flat Package (TQFP) |
| 208Q | 208-lead, Plastic Gull-Wing Quad Flat Package (PQFP) |
| 240Q | 240-lead, Plastic Gull-Wing Quad Flat Package (PQFP) |

Revision History

| Doc. No. | Date | Description |
|----------|---------|---|
| 0264G | 04/2015 | Obsoleted AT6002, AT6003, and all AT6K low voltage (LV) devices and the AT6005 and AT6010A lead based packages. Added lead free packages options for AT6005 and AT6010A devices. |
| 0264F | 10/2009 | |



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