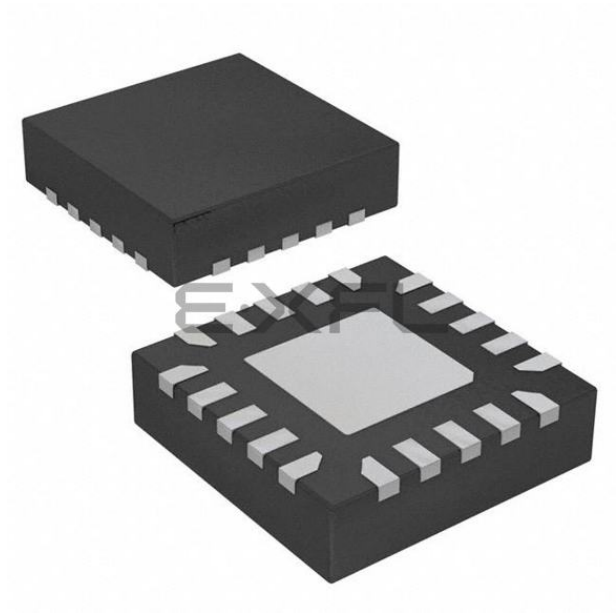

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	18
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-VFQFN Exposed Pad
Supplier Device Package	20-VQFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/attiny406-mfr

6.10.2.2 Serial Number Byte n

Name: SERNUMn
Offset: 0x03 + n*0x01 [n=0..9]
Reset: [device serial number]
Property: -

Each device has an individual serial number, representing a unique ID. This can be used to identify a specific device in the field. The serial number consists of ten bytes: SIGROW.SERNUM[9:0].

Bit	7	6	5	4	3	2	1	0
	SERNUM[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	x	x	x	x	x	x	x	x

Bits 7:0 – SERNUM[7:0] Serial Number Byte n

8.7.3 STATUS Register

Name: SREG
Offset: 0x0F
Reset: 0x00
Property: -

The STATUS register contains information about the result of the most recently executed arithmetic or logic instruction. For details about the bits in this register and how they are affected by the different instructions, see the Instruction Set Summary.

Bit	7	6	5	4	3	2	1	0
	I	T	H	S	V	N	Z	C
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 7 – I Global Interrupt Enable
Writing a '1' to this bit enables interrupts on the device.

Writing a '0' to this bit disables interrupts on the device, independent of the individual interrupt enable settings of the peripherals.

This bit is not cleared by hardware after an interrupt has occurred.

This bit can be set and cleared by software with the `SEI` and `CLI` instructions.

Changing the I flag through the I/O register results in a one-cycle Wait state on the access.

Bit 6 – T Bit Copy Storage
The bit copy instructions bit load (`BLD`) and bit store (`BST`) use the T bit as source or destination for the operated bit.

A bit from a register in the register file can be copied into this bit by the `BST` instruction, and this bit can be copied into a bit in a register in the register file by the `BLD` instruction.

Bit 5 – H Half Carry Flag
This bit indicates a half carry in some arithmetic operations. Half carry is useful in BCD arithmetic.

Bit 4 – S Sign Bit, S = N ⊕ V
The sign bit (S) is always an exclusive or (*xor*) between the negative flag (N) and the two's complement overflow flag (V).

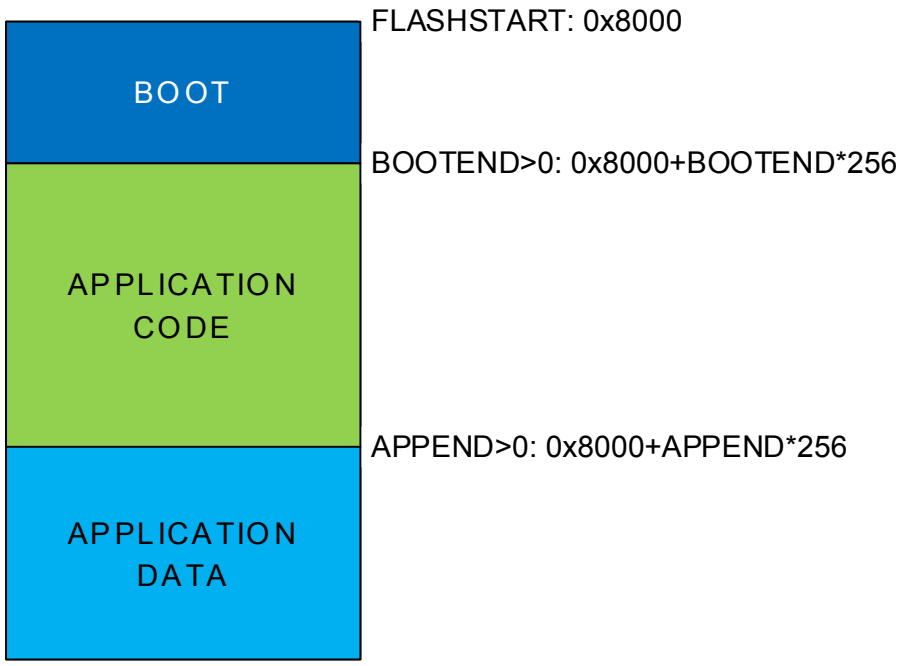
Bit 3 – V Two's Complement Overflow Flag
The two's complement overflow flag (V) supports two's complement arithmetic.

Bit 2 – N Negative Flag
The negative flag (N) indicates a negative result in an arithmetic or logic operation.

Bit 1 – Z Zero Flag
The zero flag (Z) indicates a zero result in an arithmetic or logic operation.

The Flash can be divided into three sections in blocks of 256 bytes for different security. The three different sections are BOOT, Application Code (APPCODE), and Application Data (APPDATA).

Figure 9-2. Flash Sections



Section Sizes

The sizes of these sections are set by the Boot Section End fuse (FUSE.BOOTEND) and Application Code Section End fuse (FUSE.APPEND).

The fuses select the section sizes in blocks of 256 bytes. As shown in Figure 9-2, the BOOT section stretches from the start of the Flash until BOOTEND. The APPCODE section runs from BOOTEND until APPEND. The remaining area is the APPDATA section. If APPEND is written to 0, the APPCODE section runs from BOOTEND to the end of Flash (removing the APPDATA section). If BOOTEND and APPEND are written to 0, the entire Flash is regarded as BOOT section. APPEND should either be set to 0 or a value greater or equal than BOOTEND.

Table 9-2. Setting Up Flash Sections

BOOTEND	APPEND	BOOT Section	APPCODE Section	APPDATA Section
0	0	0 to FLASHEND	-	-
> 0	0	0 to 256*BOOTEND	256*BOOTEND to FLASHEND	-
> 0	== BOOTEND	0 to 256*BOOTEND	-	256*BOOTEND to FLASHEND
> 0	> BOOTEND	0 to 256*BOOTEND	256*BOOTEND to 256*APPEND	256*APPEND to FLASHEND

Note:

- See also the BOOTEND and APPEND descriptions.

9.5.2 Control B

Name: CTRLB
Offset: 0x01
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
							BOOTLOCK	APCWP
Access							R/W	R/W
Reset							0	0

Bit 1 – BOOTLOCK Boot Section Lock
Writing a '1' to this bit locks the boot section from read and instruction fetch.

If this bit is '1', a read from the boot section will return '0'. A fetch from the boot section will also return 0 as instruction.

This bit can be written from the boot section only. It can only be cleared to '0' by a Reset.

This bit will take effect only when the boot section is left the first time after the bit is written.

Bit 0 – APCWP Application Code Section Write Protection
Writing a '1' to this bit protects the application code section from further writes.

This bit can only be written to '1'. It is cleared to '0' only by Reset.

11.5.1 Control A

Name: CTRLA
Offset: 0x00
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
						SMODE[1:0]		SEN
Access	R	R	R	R	R	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

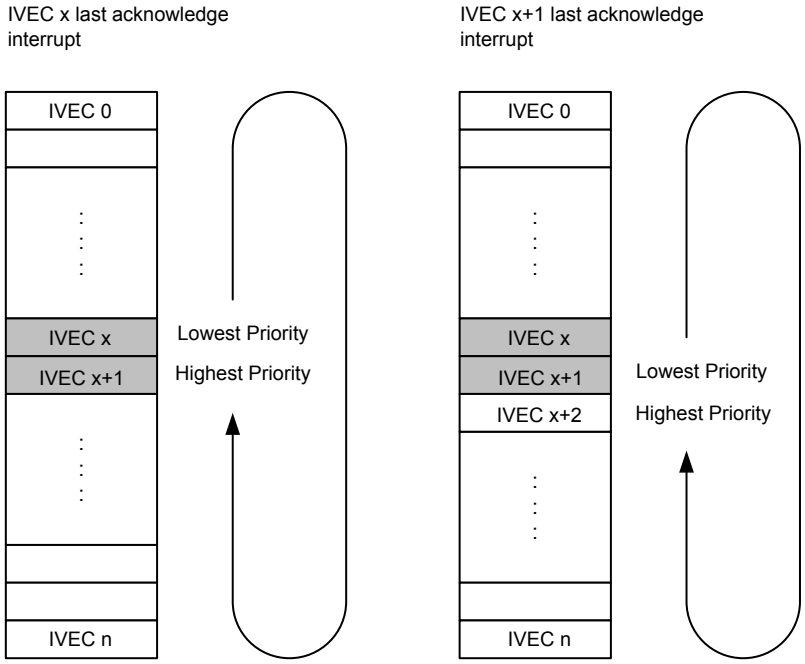
Bits 2:1 – SMODE[1:0] Sleep Mode
Writing these bits selects the sleep mode entered when the Sleep Enable bit (SEN) is written to '1' and the `SLEEP` instruction is executed.

Value	Name	Description
0x0	IDLE	Idle Sleep mode enabled
0x1	STANDBY	Standby Sleep mode enabled
0x2	PDOWN	Power-Down Sleep mode enabled
other	-	Reserved

Bit 0 – SEN Sleep Enable
This bit must be written to '1' before the `SLEEP` instruction is executed to make the MCU enter the selected sleep mode.

When round robin scheduling is enabled, the interrupt vector address for the last acknowledged LVL0 interrupt will have the lowest priority the next time one or more LVL0 interrupts are requested, as illustrated in the figure below.

Figure 13-4. Round Robin Scheduling



Compact Vector Table

The Compact Vector Table (CVT) is a feature to allow writing of compact code.

When CVT is enabled by writing a '1' to the CVT bit in the Control A register (CPUINT.CTRLA), the vector table contains these three interrupt vectors:

1. The non-maskable interrupts (NMI) at vector address 1.
2. The priority level 1 (LVL1) interrupt at vector address 2.
3. All priority level 0 (LVL0) interrupts share vector address 3.

This feature is most suitable for applications using a small number of interrupt generators.

13.3.3 Events

Not applicable.

13.3.4 Sleep Mode Operation

Not applicable.

13.3.5 Configuration Change Protection

This peripheral has registers that are under Configuration Change Protection (CCP). In order to write to these, a certain key must be written to the CPU.CCP register first, followed by a write access to the protected bits within four CPU instructions.

It is possible to try writing to these registers any time, but the values are not altered.

The following registers are under CCP:

13.4 Register Summary - CPUINT

Offset	Name	Bit Pos.								
0x00	CTRLA	7:0		IVSEL	CVT					LVL0RR
0x01	STATUS	7:0	NMIEX						LVL1EX	LVL0EX
0x02	LVL0PRI	7:0	LVL0PRI[7:0]							
0x03	LVL1VEC	7:0	LVL1VEC[7:0]							

13.5 Register Description

14.5.1 Asynchronous Channel Strobe

Name: ASYNCSTROBE
Offset: 0x00
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
	ASYNCSTROBE[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – ASYNCSTROBE[7:0] Asynchronous Channel Strobe
If the Strobe register location is written, each event channel will be inverted for one system clock cycle (i.e., a single event is generated).

15.3.1 Control A

Name: CTRLA
Offset: 0x00
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
			LUT1	LUT0		EVOUT2	EVOUT1	EVOUT0
Access			R/W	R/W		R/W	R/W	R/W
Reset			0	0		0	0	0

Bit 5 – LUT1 CCL LUT 1 output
Write this bit to '1' to select alternative pin location for CCL LUT 1.

Bit 4 – LUT0 CCL LUT 0 output
Write this bit to '1' to select alternative pin location for CCL LUT 0.

Bit 2 – EVOUT2 Event Output 2
Write this bit to '1' to enable event output 2.

Bit 1 – EVOUT1 Event Output 1
Write this bit to '1' to enable event output 1.

Bit 0 – EVOUT0 Event Output 0
Write this bit to '1' to enable event output 0.

15.3.3 Control C

Name: CTRLC
Offset: 0x02
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
			TCA05	TCA04	TCA03	TCA02	TCA01	TCA00
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit 5 – TCA05 TCA0 Waveform output 5
Write this bit to '1' to select alternative output pin for TCA0 waveform output 5 in Split mode.

Not applicable when TCA in normal mode.

Bit 4 – TCA04 TCA0 Waveform output 4
Write this bit to '1' to select alternative output pin for TCA0 waveform output 4 in Split mode.

Not applicable when TCA in normal mode.

Bit 3 – TCA03 TCA0 Waveform output 3
Write this bit to '1' to select alternative output pin for TCA0 waveform output 3 in Split mode.

Not applicable when TCA in normal mode.

Bit 2 – TCA02 TCA0 Waveform output 2
Write this bit to '1' to select alternative output pin for TCA0 waveform output 2.

In Split Mode, this bit controls output from low byte compare channel 2.

Bit 1 – TCA01 TCA0 Waveform output 1
Write this bit to '1' to select alternative output pin for TCA0 waveform output 1.

In Split mode, this bit controls output from low byte compare channel 1.

Bit 0 – TCA00 TCA0 Waveform output 0
Write this bit to '1' to select alternative output pin for TCA0 waveform output 0.

In Split mode, this bit controls output from low byte compare channel 0.

When an interrupt condition occurs, the corresponding interrupt flag is set in the Interrupt Flags register of the peripheral (*peripheral*.INTFLAGS).

An interrupt source is enabled or disabled by writing to the corresponding enable bit in the peripheral's Interrupt Control register (*peripheral*.INTCTRL).

An interrupt request is generated when the corresponding interrupt source is enabled and the interrupt flag is set. The interrupt request remains active until the interrupt flag is cleared. See the peripheral's INTFLAGS register for details on how to clear interrupt flags.

Related Links

AVR CPU

SREG

17.3.3 Sleep Mode Operation

There are two separate fuses defining the BOD configuration in different sleep modes; One fuse defines the mode used in Active mode and Idle Sleep mode (ACTIVE in FUSE.BODCFG), and is written to the ACTIVE bits in the Control A register (BOD.CTRLA). The second fuse (SLEEP in FUSE.BODCFG) selects the mode used in Standby Sleep mode and Power-Down Sleep mode, and is loaded into the SLEEP bits in the Control A register (BOD.CTRLA).

The operating mode in Active mode and Idle Sleep mode (i.e., ACTIVE in BOD.CTRLA) cannot be altered by software. The operating mode in Standby Sleep mode and Power-Down Sleep mode can be altered by writing to the SLEEP bits in the Control A register (BOD.CTRLA).

When the device is going into Standby Sleep mode or Power-Down Sleep mode, the BOD will change operation mode as defined by SLEEP in BOD.CTRLA. When the device is waking up from Standby or Power-Down Sleep mode, the BOD will operate in the mode defined by the ACTIVE bit field in BOD.CTRLA.

17.3.4 Synchronization

Not applicable.

17.3.5 Configuration Change Protection

This peripheral has registers that are under Configuration Change Protection (CCP). In order to write to these, a certain key must be written to the CPU.CCP register first, followed by a write access to the protected bits within four CPU instructions.

It is possible to try writing to these registers any time, but the values are not altered.

The following registers are under CCP:

Table 17-3. Registers Under Configuration Change Protection

Register	Key
SLEEP in BOD.CTRLA	IOREG

Related Links

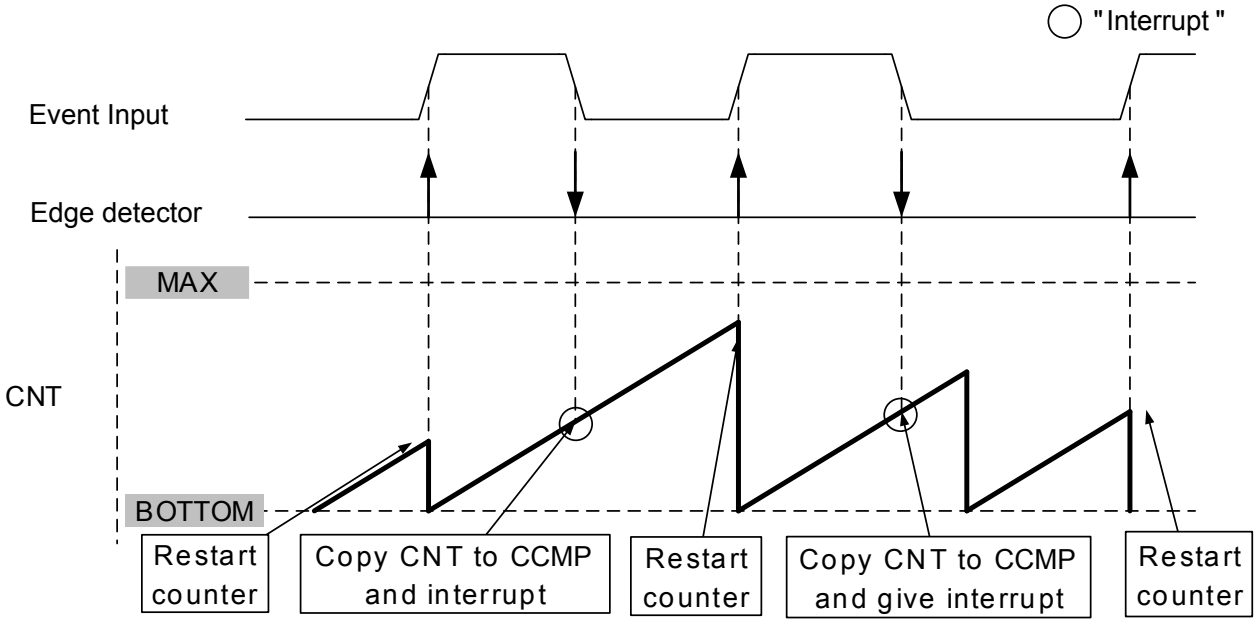
Sequence for Write Operation to Configuration Change Protected I/O Registers

respective Reference Select bit field (ADC0REFSEL, DAC0REFSEL) in the Control A register (VREF.CTRLA).

Input Capture Pulse-Width Measurement Mode

The input capture pulse-width measurement will restart the counter on a positive edge and capture on the next falling edge before an interrupt request is generated. The interrupt flag is automatically cleared when the high byte of the capture register is read. The timer will automatically switch between rising and falling edge detection, but a minimum edge separation of two clock cycles is required for correct behavior.

Figure 21-6. Input Capture Pulse-Width Measurement



Input Capture Frequency and Pulse-Width Measurement Mode

In this mode the timer will start counting when a positive edge is detected on the even input signal. On the following falling edge, the count value is captured. The counter stops when the second rising edge of the event input signal is detected and this will set the interrupt flag.

Reading the capture will clear the interrupt flag. When the capture register is read or the interrupt flag is cleared the TC is ready for a new capture sequence. The counter register should, therefore, be read before the capture register as this is reset to zero at the next positive edge.

21.5.8 Temporary Value

Name: TEMP
Offset: 0x09
Reset: 0x00
Property: -

The Temporary register is used by the CPU for single-cycle, 16-bit access to the 16-bit registers of this peripheral. It can be read and written by software. See Accessing 16-Bit Registers. There is one common Temporary register for all the 16-bit registers of this peripheral.

Bit	7	6	5	4	3	2	1	0
	TEMP[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – TEMP[7:0] Temporary Value

22.11.6 Debug Control

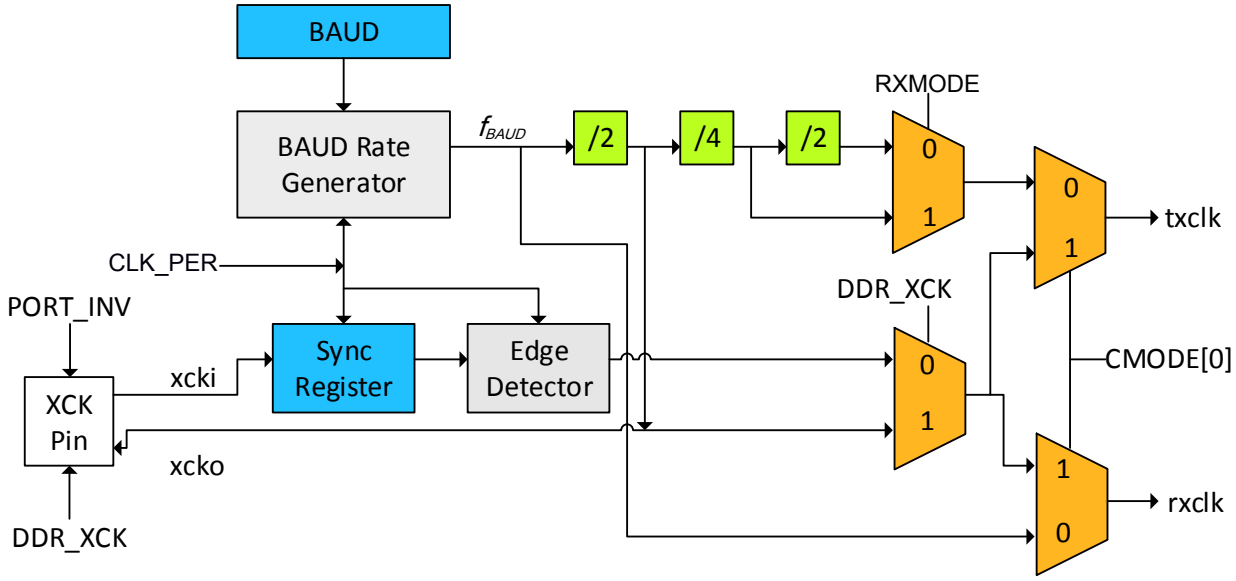
Name: DBGCTRL
Offset: 0x05
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
								DBGRUN
Access								R/W
Reset								0

Bit 0 – DBGRUN Debug Run

Value	Description
0	The peripheral is halted in Break Debug mode and ignores events.
1	The peripheral will continue to run in Break Debug mode when the CPU is halted.

Figure 23-2. Clock Generation Logic Block Diagram



Internal Clock Generation - The Fractional Baud Rate Generator

The Baud Rate Generator is used for internal clock generation for Asynchronous modes, Aynchronous Master mode, and Master SPI mode operation. The output frequency generated (f_{BAUD}) is determined by the baud register value (USARTn.BAUD) and the peripheral clock frequency (f_{CLK_PER}). The following table contains equations for calculating the baud rate (in bits per second) and for calculating the USARTn.BAUD value for each mode of operation. It also shows the maximum baud rate versus peripheral clock frequency. For asynchronous operation, the USARTn.BAUD register value is 16 bits. The 10 MSBs (BAUD[15:6]) hold the integer part, while the 6 LSBs (BAUD[5:0]) hold the fractional part. In Synchronous mode, only the integer part of the BAUD register determine the baud rate.

Table 23-2. Equations for Calculating Baud Rate Register Setting

Operating Mode	Conditions	Baud Rate (Bits Per Seconds)	USART.BAUD Register Value Calculation
Asynchronous	$f_{BAUD} \leq \frac{f_{CLK\_PER}}{S}$	$f_{BAUD} = \frac{64 \times f_{CLK\_PER}}{S \times BAUD}$	$BAUD = \frac{64 \times f_{CLK\_PER}}{S \times f_{BAUD}}$
Synchronous	$f_{BAUD} \leq \frac{f_{CLK\_PER}}{2}$	$f_{BAUD} = \frac{f_{CLK\_PER}}{2 \times BAUD[15:6]}$	$BAUD[15:6] = \frac{f_{CLK\_PER}}{2 \times f_{BAUD}}$

S is the number of samples per bit. In Asynchronous operating mode (CMODE[0]=0), it could be set as 16 (NORMAL mode) or 8 (CLK2X mode) by RXMODE in USARTn.CTRLB. For Synchronous operating mode (CMODE[0]=1), *S* equals 2.

External Clock

External clock (XCK) is used in Synchronous Slave mode operation. The XCK clock input is sampled on the peripheral clock frequency and the maximum XCK clock frequency (f_{XCK}) is limited by the following:

$$f_{XCK} < \frac{f_{CLK\_PER}}{4}$$

24.5.3 Interrupt Control

Name: INTCTRL
Offset: 0x02
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
	RXCIE	TXCIE	DREIE	SSIE				IE
Access	R/W	R/W	R/W	R/W				R/W
Reset	0	0	0	0				0

Bit 7 – RXCIE Receive Complete Interrupt Enable
In Buffer mode, this bit enables the receive complete interrupt. The enabled interrupt will be triggered when the RXCIF flag in the SPIn.INTFLAGS register is set. In Non-Buffer mode this bit is zero.

Bit 6 – TXCIE Transfer Complete Interrupt Enable
In Buffer mode, this bit enables the transfer complete interrupt. The enabled interrupt will be triggered when the TXCIF flag in the SPIn.INTFLAGS register is set. In Non-Buffer mode, this bit is zero.

Bit 5 – DREIE Data Register Empty Interrupt Enable
In Buffer mode this bit enables the data register empty interrupt. The enabled interrupt will be triggered when the DREIF flag in the SPIn.INTFLAGS register is set. In Non-Buffer mode, this bit is zero.

Bit 4 – SSIE Slave Select Trigger Interrupt Enable
In Buffer mode, this bit enables the Slave Select interrupt. The enabled interrupt will be triggered when the SSIF flag in the SPIn.INTFLAGS register is set. In Non-Buffer mode, this bit is zero.

Bit 0 – IE Interrupt Enable
This bit enables the SPI interrupt when the SPI is not in Buffer mode. The enabled interrupt will be triggered when RXCIF/IF is set in the SPIn.INTFLAGS register.

28.4 Register Summary - AC

Offset	Name	Bit Pos.								
0x00	CTRLA	7:0	RUNSTDBY	OUTEN	INTMODE[1:0]			HYSMODE[1:0]		ENABLE
0x01	Reserved									
0x02	MUXCTRLA	7:0	INVERT				MUXPOS		MUXNEG[1:0]	
0x03 ... 0x05	Reserved									
0x06	INTCTRL	7:0								CMP
0x07	STATUS	7:0				STATE				CMP

28.5 Register Description

31.9 Oscillators and Clocks

Operating conditions:

- V_{DD} = 3V, except where specified otherwise

Table 31-12. Internal Oscillator (OSC20M) Characteristics

Symbol	Description	Condition		Min.	Typ.	Max.	Unit
f_{OSC20M}	Accuracy with 16 MHz and 20 MHz frequency selection relative to the factory-stored frequency value	Factory calibrated V_{DD}=3V(1)	T=[0, 70]°C, V_{DD}=[1.8, 4.5]V(3)	-2.0	-	2.0	%
		Factory calibrated V_{DD}=5V(1)	T=[0, 70]°C, V_{DD}=[4.5, 5.5]V(3)	-2.0	-	2.0	
	Accuracy with 16 MHz and 20 MHz frequency selection	Factory calibrated	T=25°C, 3.0V	-3.0	-	3.0	%
			T=[0, 70]°C, V_{DD}=[1.8, 3.6]V(3)	-4.0	-	4.0	
			Full operation range(3)	-5.0	-	5.0	
f_{CAL}	User calibration range	OSC20M(2) = 16 MHz		14.5	-	17.5	MHz
		OSC20M(2) = 20 MHz		18.5	-	21.5	
%CAL	Calibration step size			-	1.5	-	%
DC	Duty cycle			-	50	-	%
T_{start}	Start-up time	Within 2% accuracy		-	8	-	µs

Note:

1. See the description of OSC20M on calibration.
2. Oscillator frequencies above speed specification must be divided so that CPU clock always is within specification.
3. These values are based on characterization and not covered by production test limits.

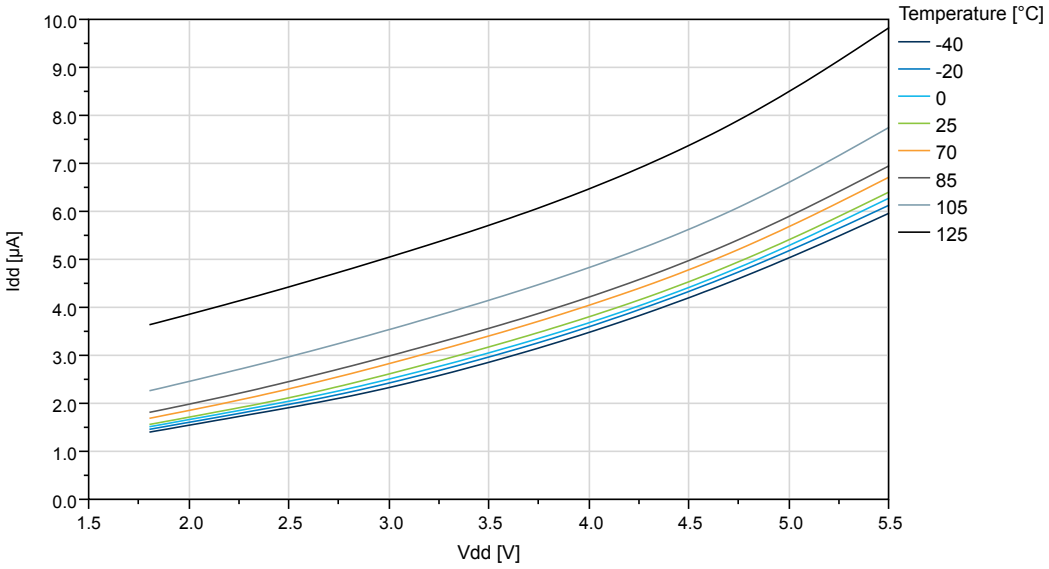
Table 31-13. 32.768 kHz Internal Oscillator (OSCULP32K) Characteristics

Symbol	Description	Condition	Condition	Min.	Typ.	Max.	Unit
$f_{OSCULP32K}$	Accuracy	Factory calibrated	T=25°C, 3.0V	-3	-	3	%
			T=[0, 70]°C, V_{DD}=[1.8, 3.6]V(1)	-10	-	10	
			Full operation range(1)	-30	-	30	
DC	Duty cycle			-	50	-	%
T_{start}	Start-up time			-	250	-	µs

Note:

1. These values are based on characterization and not covered by production test limits.

Figure 32-9. ATtiny406: Idle Supply Current vs. V_{DD} (f=32 KHz OSCULP32K)



32.1.3 Supply Currents in Power-Down Mode for ATtiny406

Figure 32-10. ATtiny406: Power-Down Mode Supply Current vs. Temperature (All Functions Disabled)