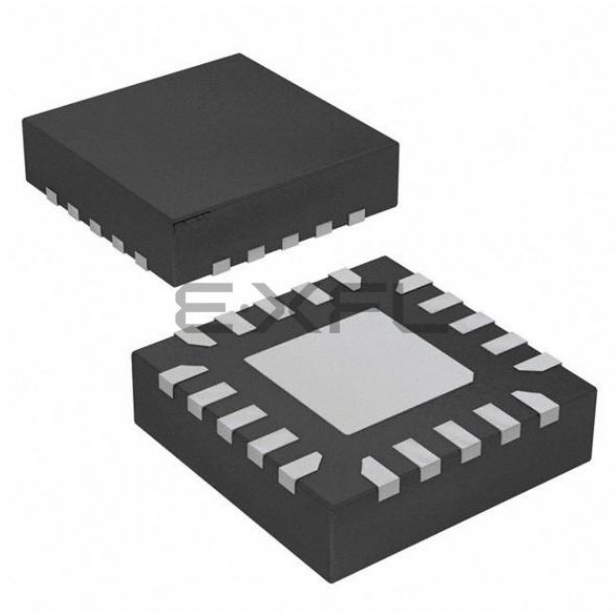

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	18
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-VFQFN Exposed Pad
Supplier Device Package	20-VQFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/attiny406-mnr

6.10.2.4 OSC16 Error at 3V

Name: OSC16ERR3V
Offset: 0x22
Reset: [Oscillator frequency error value]
Property: -

Bit	7	6	5	4	3	2	1	0
	OSC16ERR3V[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	x	x	x	x	x	x	x	x

Bits 7:0 – OSC16ERR3V[7:0] OSC16 Error at 3V
These registers contain the signed oscillator frequency error value when running at internal 16 MHz at 3V, as measured during production.

6.10.4.5 System Configuration 1

Name: SYSCFG1
Offset: 0x06
Reset: -
Property: -

Bit	7	6	5	4	3	2	1	0
						SUT[2:0]		
Access						R	R	R
Reset						1	1	1

Bits 2:0 – SUT[2:0] Start-Up Time Setting
These bits select the start-up time between power-on and code execution.

Value	Description
0x0	0 ms
0x1	1 ms
0x2	2 ms
0x3	4 ms
0x4	8 ms
0x5	16 ms
0x6	32 ms
0x7	64 ms

9.4 Register Summary - NVMCTRL

Offset	Name	Bit Pos.								
0x00	CTRLA	7:0						CMD[2:0]		
0x01	CTRLB	7:0							BOOTLOCK	APCWP
0x02	STATUS	7:0						WRERROR	EEBUSY	FBUSY
0x03	INTCTRL	7:0								EEREADY
0x04	INTFLAGS	7:0								EEREADY
0x05	Reserved									
0x06	DATA	7:0	DATA[7:0]							
		15:8	DATA[15:8]							
0x08	ADDR	7:0	ADDR[7:0]							
		15:8	ADDR[15:8]							

9.5 Register Description

15.3.2 Control B

Name: CTRLB
Offset: 0x01
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
						SPI0		USART0
Access						R/W		R/W
Reset						0		0

Bit 2 – SPI0 SPI 0 communication
Write this bit to '1' to select alternative communication pins for SPI 0.

Bit 0 – USART0 USART 0 communication
Write this bit to '1' to select alternative communication pins for USART 0.

Asynchronous Sensing Pin Properties

Table 16-4. Behavior Comparison of Fully/Partly Asynchronous Sense Pin

Property	Synchronous or Partly Asynchronous Sense Support	Full Asynchronous Sense Support
Minimum pulse-width to trigger interrupt	Minimum one system clock cycle	Less than a system clock cycle
Waking the device from sleep	From all interrupt sense configurations from sleep modes with main clock running. Only from BOTHEDGES or LEVEL interrupt sense configuration from sleep modes with main clock stopped.	From all interrupt sense configurations from all sleep modes
Interrupt "dead time"	No new interrupt for three cycles after the previous	No limitation
Minimum wake-up pulse length	Value on pad must be kept until the system clock has restarted	No limitation

Related Links

AVR CPU

SREG

16.3.4 Events

All PORT pins are asynchronous event system generators, PORT has as many event generators as there are PORT pins in the device. Each event system output from PORT is the value present on the corresponding pin if the digital input driver is enabled. If a pin input driver is disabled, the corresponding event system output is zero.

PORT has no event inputs.

16.3.5 Sleep Mode Operation

With the exception of interrupts and input synchronization, all pin configurations are independent of the Sleep mode. Peripherals connected to the ports can be affected by Sleep modes, described in the respective peripherals' documentation.

The port peripheral will always use the main clock. Input synchronization will halt when this clock stops.

16.3.6 Synchronization

Not applicable.

16.3.7 Configuration Change Protection

Not applicable.

16.7.2 Output Value

Name: OUT
Offset: 0x01
Reset: 0x00
Property: -

Writing to the Virtual PORT registers has the same effect as writing to the regular registers, but allows for memory-specific instructions, such as bit-manipulation instructions, which are not valid for the extended I/O memory space where the regular PORT registers reside.

Bit	7	6	5	4	3	2	1	0
	OUT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – OUT[7:0] Output Value
This bit field selects the data output value for the individual pins in the port.

20.5.7 Control Register F Clear

Name: CTRLFCLR
Offset: 0x06
Reset: 0x00
Property: -

The individual Status bit can be cleared by writing a '1' to its bit location. This allows each bit to be cleared without the use of a read-modify-write operation on a single register.

Bit	7	6	5	4	3	2	1	0
					CMP2BV	CMP1BV	CMP0BV	PERBV
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 3 – CMP2BV Compare 2 Buffer Valid
See CMP0BV.

Bit 2 – CMP1BV Compare 1 Buffer Valid
See CMP0BV.

Bit 1 – CMP0BV Compare 0 Buffer Valid
The CMPnBV bits are set when a new value is written to the corresponding TCAn.CMPnBUF register. These bits are automatically cleared on an UPDATE condition.

Bit 0 – PERBV Period Buffer Valid
This bit is set when a new value is written to the TCAn.PERBUF register. This bit is automatically cleared on an UPDATE condition.

20.7.1 Control A

Name: CTRLA
Offset: 0x00
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
					CLKSEL[2:0]			ENABLE
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bits 3:1 – CLKSEL[2:0] Clock Select
These bits select the clock frequency for the timer/counter.

Value	Name	Description
0x0	DIV1	$f_{TCA} = f_{CLK\_PER}/1$
0x1	DIV2	$f_{TCA} = f_{CLK\_PER}/2$
0x2	DIV4	$f_{TCA} = f_{CLK\_PER}/4$
0x3	DIV8	$f_{TCA} = f_{CLK\_PER}/8$
0x4	DIV16	$f_{TCA} = f_{CLK\_PER}/16$
0x5	DIV64	$f_{TCA} = f_{CLK\_PER}/64$
0x6	DIV256	$f_{TCA} = f_{CLK\_PER}/256$
0x7	DIV1024	$f_{TCA} = f_{CLK\_PER}/1024$

Bit 0 – ENABLE Enable

Value	Description
0	The peripheral is disabled
1	The peripheral is enabled

20.7.15 High Byte Compare Register n - Split Mode

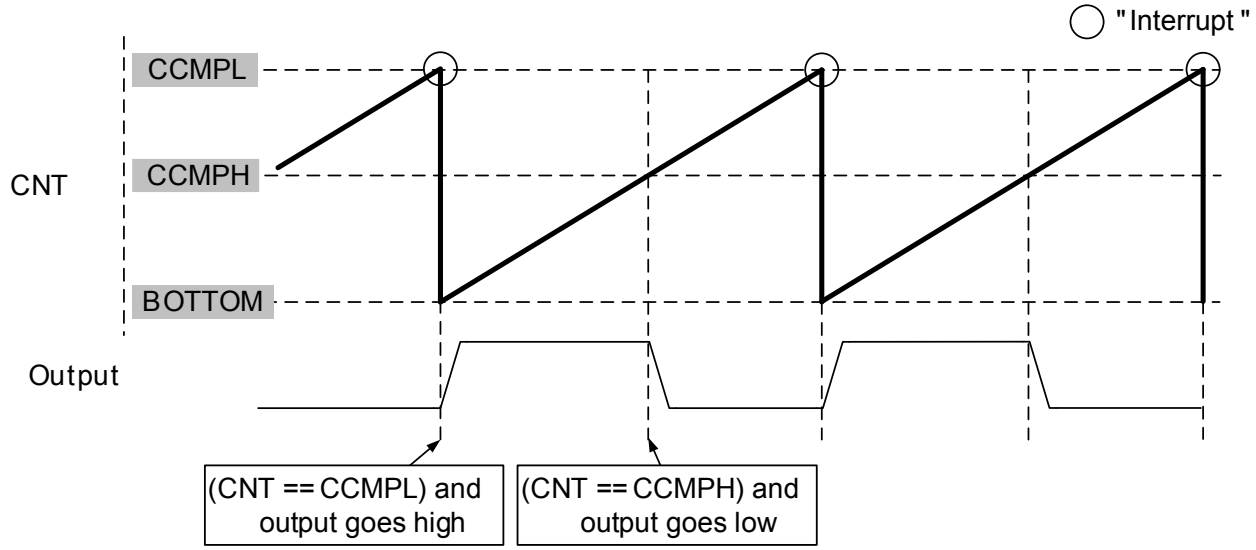
Name: HCMP
Offset: 0x29 + n*0x02 [n=0..2]
Reset: 0x00
Property: -

The TCAn.HCMPn register represents the compare value of compare channel n for high byte timer. This register is continuously compared to the counter value of the high byte timer, TCAn.HCNT. Normally, the outputs from the comparators are then used for generating waveforms.

Bit	7	6	5	4	3	2	1	0
	HCMP[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – HCMP[7:0] Compare Value of Channel n
These bits hold the compare value of channel n that is compared to TCAn.HCNT.

Figure 21-9. 8-Bit PWM Mode



21.3.3.2 Output

If ASYNC in TCBn.CTRLB is written to '0' ('1'), the output pin is driven synchronously (asynchronously) to the TCB clock. The bits CCMPINIT, CCMPEN, and CNTMODE in TCBn.CTRLB control how the synchronous output is driven. The different configurations and their impact on the output are listed in the table below.

Table 21-3. Synchronous Output

CNTMODE	Output, CTRLB='0', CCMPEN=1	Output, CTRLB='1', CCMPEN=1
Single-Shot mode	Output high when the counter starts and output low when counter stops	Output high when event arrives and output low when the counter stops
8-bit PWM mode	PWM mode output	PWM mode output
Modes except single shot and PWM	Bit CCMPINIT in TCBn.CTRLB	Bit CCMPINIT in TCBn.CTRLB

21.3.3.3 Noise Canceler

The noise canceler improves noise immunity by using a simple digital filter scheme. When the noise filter is enabled, the peripheral monitors the event channel and keeps a record of the last four observed samples. If four consecutive samples are equal, the input is considered to be stable and the signal is fed to the edge detector.

When enabled, the noise canceler introduces an additional delay of four system clock cycles between a change applied to the input and the update of the input compare register.

The noise canceler uses the system clock and is, therefore, not affected by the prescaler.

21.3.3.4 Synchronized with TCAn

TCB can be configured to use the clock (CLK_TCA) of the Timer/Counter type A (TCAn) by writing to the Clock Select bit field (CLKSEL) in the Control A register (TCBn.CTRLA). In this setting, the TCB will count on the exect same clocks sources as selected in TCA.

22.11.10 Compare

Name: CMP
Offset: 0x0C
Reset: 0x00
Property: -

The RTC.CMPL and RTC.CMPH register pair represents the 16-bit value, CMP. The low byte [7:0] (suffix L) is accessible at the original offset. The high byte [15:8] (suffix H) can be accessed at offset + 0x01. For more details on reading and writing 16-bit registers, refer to Accessing 16-Bit Registers.

Bit	15	14	13	12	11	10	9	8
	CMP[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CMP[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – CMP[15:8] Compare High Byte
These bits hold the MSB of the 16-bit Compare register.

Bits 7:0 – CMP[7:0] Compare Low Byte
These bits hold the LSB of the 16-bit Compare register.

Related Links

CTRLC

USART SPI vs. SPI

The USART in Master SPI mode is fully compatible with the stand-alone SPI module in that:

- Timing diagrams are the same
- UCPHA bit functionality is identical to that of the SPI CPHA bit
- UDORD bit functionality is identical to that of the SPI DORD bit

When the USART is set in Master SPI mode, configuration and use are in some cases different from those of the stand-alone SPI module. In addition, the following difference exists:

- The USART in Master SPI mode does not include the SPI (Write Collision) feature

The USART in Master SPI mode does not include the SPI Double-Speed mode feature, but this can be achieved by configuring the Baud Rate Generator accordingly:

- Interrupt timing is not compatible
- Pin control differs due to the master-only operation of the USART in SPI Master mode

A comparison of the USART in Master SPI mode and the SPI pins is shown in Table 23-6.

Table 23-6. Comparison of USART in Master SPI Mode and SPI Pins

USART	SPI	Comment
TxD	MOSI	Master out only
RxD	MISO	Master in only
XCK	SCK	Functionally identical
-	SS	Not supported by USART in Master SPI mode

Related Links

CTRLC

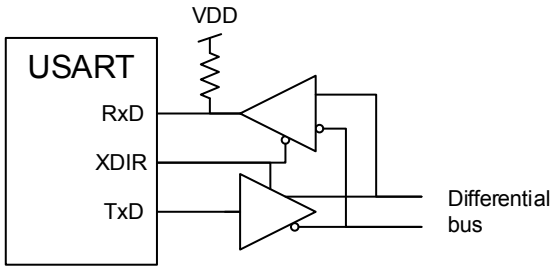
23.3.2.6 RS-485 Mode of Operation

The RS-485 feature enables the support of external components to comply with the RS-485 standard.

Either an external line driver is supported as shown in the figure below (RS-485=0x1 in USARTn.CTRLA), or control of the transmitter driving the TxD pin is provided (RS-485=0x2).

While operating in RS-485 mode, the Transmit Direction pin (XDIR) is driven high when the transmitter is active.

Figure 23-10. RS-485 Bus Connection



25.3.7 Sleep Mode Operation

The bus state logic and slave continue to operate in all Sleep modes, including Power-Down Sleep mode. If a slave device is in Sleep mode and a Start condition is detected, clock stretching is active during the wake-up period until the system clock is available. The master will stop operation in all Sleep modes.

25.3.8 Synchronization

Not applicable.

25.3.9 Configuration Change Protection

Not applicable.

27. Configurable Custom Logic (CCL)

27.1 Features

- Glue Logic for General Purpose PCB Design
- Up to two Programmable Look-Up Tables LUT[1:0]
- Combinatorial Logic Functions: Any Logic Expression That is a Function of up to Three Inputs.
- Sequential Logic Functions:
  Gated D Flip-Flop, JK Flip-Flop, gated D Latch, RS Latch
- Flexible Look-Up Table Inputs Selection:
  - I/Os
  - Events
  - Subsequent LUT output
  - Internal peripherals
    - Analog comparator
    - Timer/counters
    - USART
    - SPI
- Clocked by System Clock or Other Peripherals
- Output Can be Connected to I/O pins or Event System
- Optional Synchronizer, Filter, or Edge Detector Available on Each LUT Output

27.2 Overview

The Configurable Custom Logic (CCL) is a programmable logic peripheral which can be connected to the device pins, to events, or to other internal peripherals. The CCL can serve as "glue logic" between the device peripherals and external devices. The CCL can eliminate the need for external logic components, and can also help the designer to overcome real-time constraints by combining core independent peripherals to handle the most time-critical parts of the application independent of the CPU.

The CCL peripheral has one pair of Look-Up Tables (LUT). Each LUT consists of three inputs, a truth table, and a filter/edge detector. Each LUT can generate an output as a user programmable logic expression with three inputs. Inputs can be individually masked.

The output can be generated from the inputs combinatorially and can be filtered to remove spikes. An optional sequential module can be enabled. The inputs to the sequential module are individually controlled by two independent, adjacent LUT (LUT0/LUT1) outputs, enabling complex waveform generation.

27.2.3.1 Clocks

By default, the CCL is using the peripheral clock of the device (CLK_PER).

Alternatively, the CCL can be clocked by a peripheral input that is available on LUT n input line 2 (LUTn_IN[2]). This is configured by writing a '1' to the Clock Source Selection bit (CLKSRC) in the LUTn Control A register (CCL.LUTnCTRLA). The sequential block is clocked by the same clock as that of the even LUT in the LUT pair (SEQn.clk = LUT2n.clk). It is advised to disable the peripheral by writing a '0' to the Enable bit (ENABLE) in the Control A register (CCL.CTRLA) before configuring the CLKSRC bit in CCL.LUTnCTRLA.

Alternatively, the input line 2 (IN[2]) of an LUT can be used to clock the LUT and the corresponding Sequential block. This is enabled by writing a '1' to the Clock Source Selection bit (CLKSRC) in the LUTn Control A register (CCL.LUTnCTRLA).

The CCL must be disabled before changing the LUT clock source: write a '0' to the Enable bit (ENABLE) in Control A register (CCL.CTRLA).

Related Links

Clock Controller (CLKCTRL)

27.2.3.2 I/O Lines

The CCL can take inputs and generate output through I/O pins. For this to function properly, the I/O pins must be configured to be used by a Look Up Table (LUT).

Related Links

I/O Pin Configuration (PORT)

27.2.3.3 Interrupts

Not applicable.

27.2.3.4 Events

The CCL can use events from other peripherals and generate events that can be used by other peripherals. For this feature to function, the events have to be configured properly. Refer to the Related Links below for more information about the event users and event generators.

27.2.3.5 Debug Operation

When the CPU is halted in Debug mode the CCL continues normal operation. However, the CCL cannot be halted when the CPU is halted in Debug mode. If the CCL is configured in a way that requires it to be periodically serviced by the CPU, improper operation or data loss may result during debugging.

27.3 Functional Description

27.3.1 Initialization

The following bits are enable-protected, meaning that they can only be written when the corresponding even LUT is disabled (ENABLE=0 in CCL.LUT0CTRLA):

- Sequential Selection (SEQSEL) in Sequential Control 0 register (CCL.SEQCTRL0)

The following registers are enable-protected, meaning that they can only be written when the corresponding LUT is disabled (ENABLE=0 in CCL.LUT0CTRLA):

- LUT n Control x register, except ENABLE bit (CCL.LUTnCTRLx)

Enable-protected bits in the CCL.LUTnCTRLx registers can be written at the same time as ENABLE in CCL.LUTnCTRLx is written to '1', but not at the same time as ENABLE is written to '0'.

27.5.6 TRUTHn

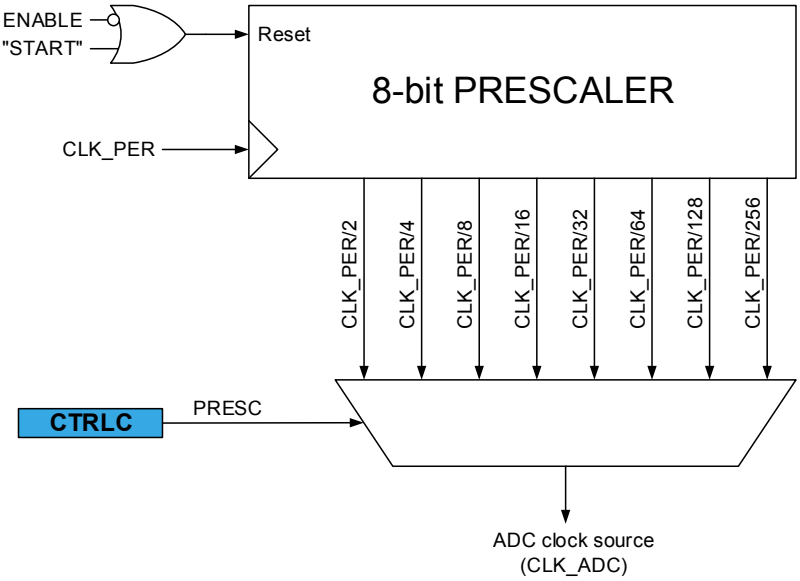
Name: TRUTH
Offset: 0x08 + n*0x04 [n=0..1]
Reset: 0x00
Property: Enable-Protected

Bit	7	6	5	4	3	2	1	0
	TRUTH[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – TRUTH[7:0] Truth Table
These bits define the value of truth logic as a function of inputs IN[2:0].

29.3.2.2 Clock Generation

Figure 29-6. ADC Prescaler



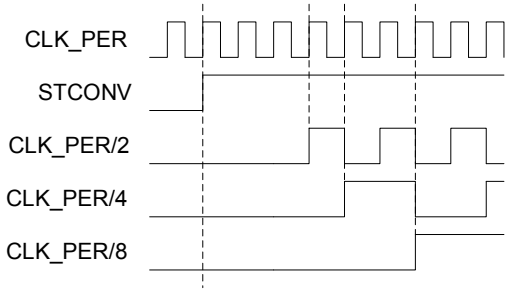
The ADC requires an input clock frequency between 50 kHz and 1.5 MHz for maximum resolution. If a lower resolution than 10 bits is selected, the input clock frequency to the ADC can be higher than 1.5 MHz to get a higher sample rate.

The ADC module contains a prescaler which generates the ADC clock (CLK_ADC) from any CPU clock (CLK_PER) above 100 kHz. The prescaling is selected by writing to the Prescaler bits (PRESC) in the Control C register (ADCn.CTRLC). The prescaler starts counting from the moment the ADC is switched on by writing a '1' to the ENABLE bit in ADCn.CTRLA. The prescaler keeps running as long as the ENABLE bit is one. The prescaler counter is reset to zero when the ENABLE bit is zero.

When initiating a conversion by writing a '1' to the Start Conversion bit (STCONV) in the Command register (ADCn.COMMAND) or from event, the conversion starts at the following rising edge of the CLK_ADC clock cycle. The prescaler is kept reset as long as there is no ongoing conversion. This assures a fixed delay from the trigger to the actual start of a conversion in CLK_PER cycles as:

$$\text{StartDelay} = \frac{\text{PRESC}_{\text{factor}}}{2} + 2$$

Figure 29-7. Start Conversion and Clock Generation



29.3.2.3 Conversion Timing

A normal conversion takes 13 CLK_ADC cycles. The actual sample-and-hold takes place two CLK_ADC cycles after the start of a conversion. Start of conversion is initiated by writing a '1' to the STCONV bit in ADC.COMMAND. When a conversion is complete, the result is available in the Result register (ADC.RES), and the Result Ready interrupt flag is set (RESRDY in ADC.INTFLAG). The interrupt flag will

Mode	Description	Condition		Typ.	Max.	Unit
			V_{DD}=3V	0.9	-	mA
		CLK_CPU=5 MHz (OSC20M div4)	V_{DD}=5V	1.2	-	mA
			V_{DD}=3V	0.6	-	mA
			V_{DD}=2V	0.4	-	mA
		CLK_CPU=32 KHz (OSCULP32K)	V_{DD}=5V	5.4	-	µA
			V_{DD}=3V	2.6	-	µA
			V_{DD}=2V	1.7	-	µA

Table 31-5. Power Consumption in Power-Down, Standby, and Reset Mode

Mode	Description	Condition		Typ. 25°C	Max. 85°C	Max. 125°C	Unit
Standby	Standby power consumption	RTC running at 1.024 kHz from internal OSCULP32K	V_{DD}=3V	0.71	6.0	8.0	µA
Power-down/ Standby	Power-down/Standby power consumption are the same when all peripherals are stopped	All peripherals stopped	V_{DD}=3V	0.1	5.0	7.0	µA
Reset	Reset power consumption	Reset line pulled down	V_{DD}=3V	100	-	-	µA

31.5 Wake-Up Time

Wake-up time from Sleep mode is measured from the edge of the wake-up signal to the first instruction executed.

Operating conditions:

- V_{DD} = 3V
- T = 25°C
- OSC20M as system clock source, unless otherwise specified

Table 31-6. Start-Up, Reset, and Wake-Up Time from OSC20M

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
t_{wakeup}	Start-up time from any Reset release		-	200	-	µs
	Wake-up from Idle mode	OSC20M @ 20 MHz; V_{DD}=5V	-	1	-	
		OSC20M @ 10 MHz; V_{DD}=3V	-	2	-	

32.3 VREF Characteristics

Figure 32-31. Internal 0.55V Reference vs. Temperature

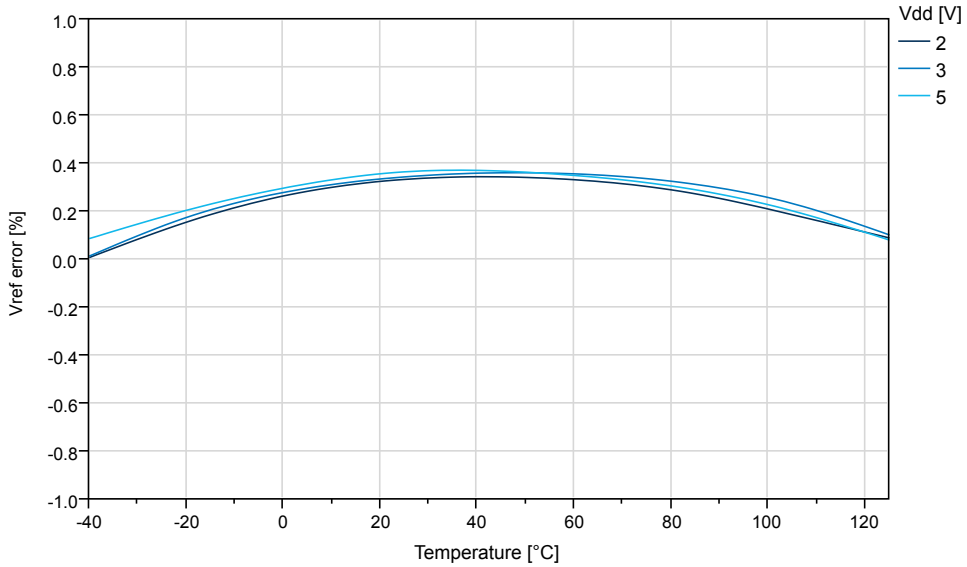
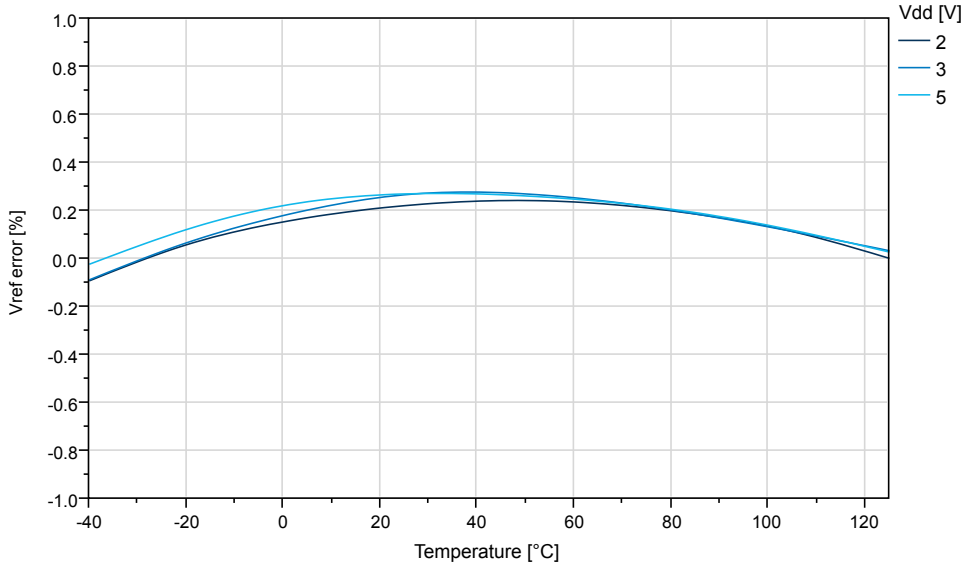


Figure 32-32. Internal 1.1V Reference vs. Temperature



39. Data Sheet Revision History

Note: The data sheet revision is independent of the die revision and the device variant (last letter of the ordering number).

39.1 Revision History

Revision A (2/2018): Initial release.