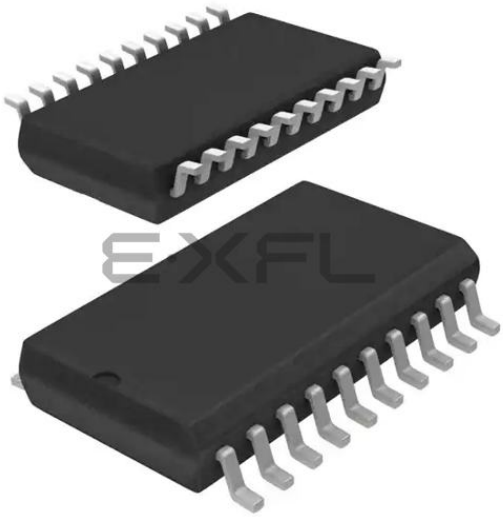

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

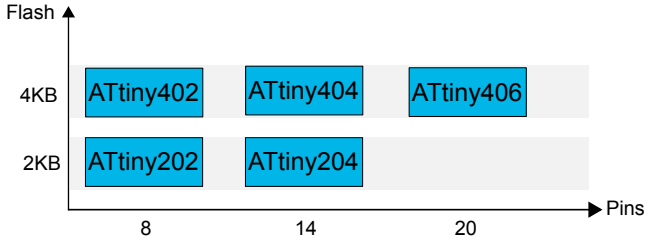
Details	
Product Status	Active
Core Processor	AVR
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	18
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/attiny406-snr

1. tinyAVR® 0-Series Overview

The figure below shows the tinyAVR 0-series, laying out pin count variants and memory sizes:

- Vertical migration can be done upwards without code modification since these devices are pin compatible and provide the same or additional features. Downward migration may require code modification due to fewer available instances of some peripherals.
- Horizontal migration to the left reduces the pin count and therefore, the available features.

Figure 1-1. Device Family Overview

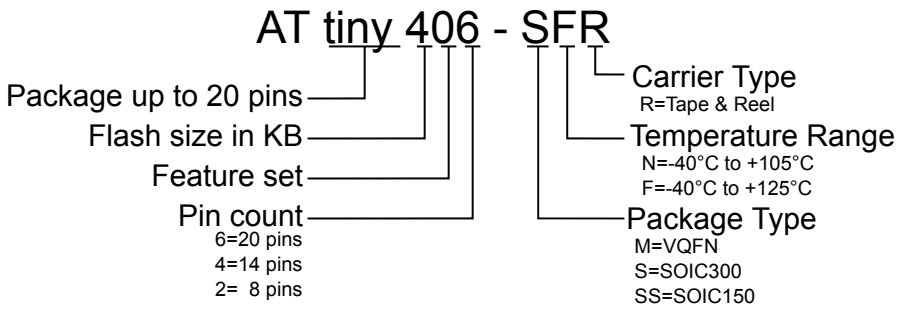


The fully compatible variants of the ATtiny devices, that is the vertical migration option shown in the figure above, come with both smaller and larger Flash memories.

Devices with different Flash memory size typically also have different SRAM and EEPROM.

The name of a device of the ATtiny family contains information as depicted below (not all options are available):

Figure 1-2. Device Designations

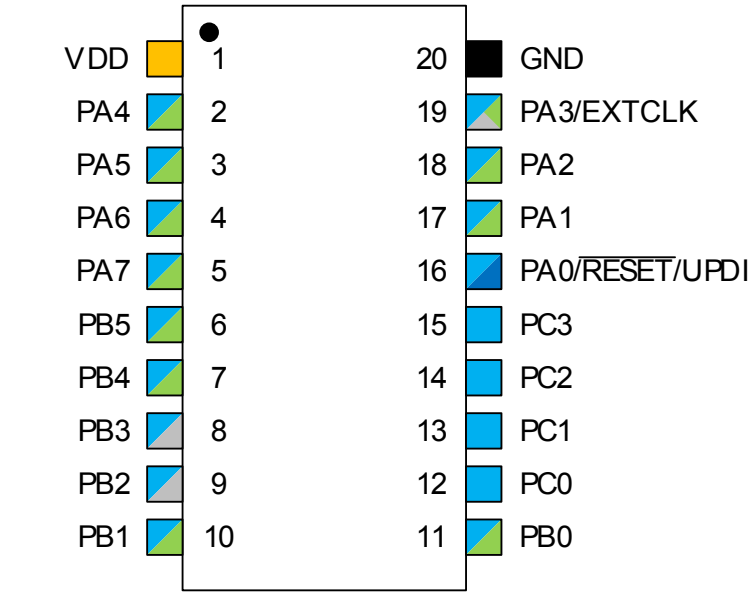


1.1 Configuration Summary

1.1.1 Peripheral Summary

Table 1-1. Peripheral Summary

	ATtiny406
Pins	20
SRAM	256B
Flash	4 KB


VDD 1
PA4 2
PA5 3
PA6 4
PA7 5
PB5 6
PB4 7
PB3 8
PB2 9
PB1 10
20 GND
19 PA3/EXTCLK
18 PA2
17 PA1
16 PA0/RESET/UPDI
15 PC3
14 PC2
13 PC1
12 PC0
11 PB0

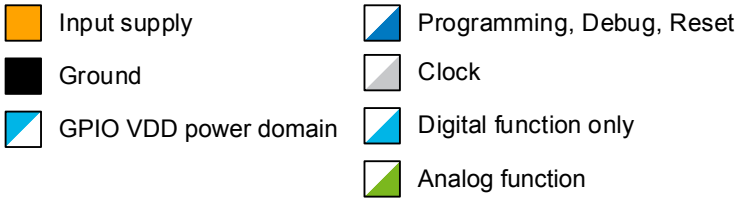
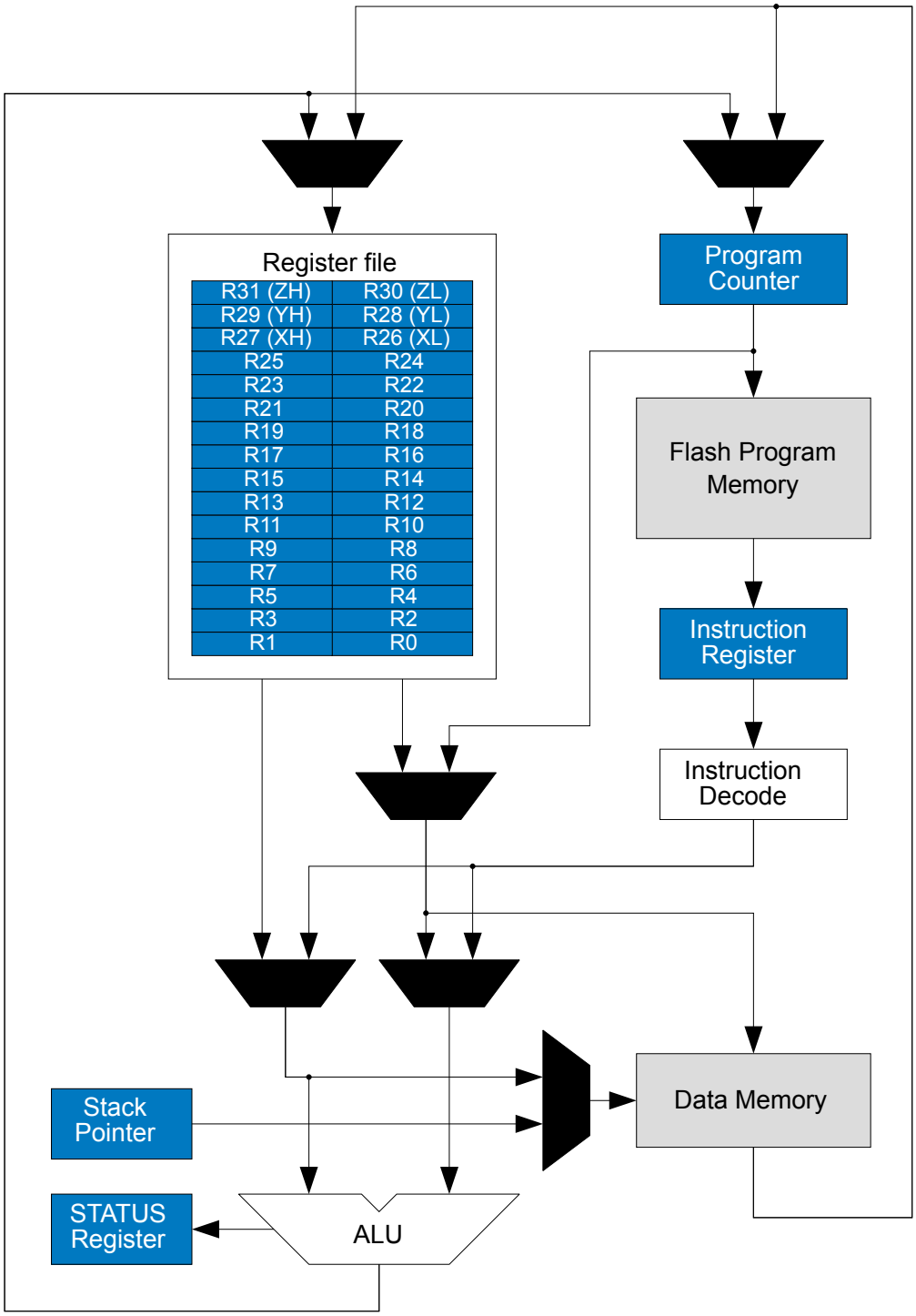

Input supply
Ground
GPIO VDD power domain
Programming, Debug, Reset
Clock
Digital function only
Analog function

Figure 8-1. AVR CPU Architecture



The Arithmetic Logic Unit (ALU) supports arithmetic and logic operations between registers or between a constant and a register. Also, single-register operations can be executed in the ALU. After an arithmetic operation, the STATUS register is updated to reflect information about the result of the operation.

The ALU is directly connected to the fast-access register file. The 32 8-bit general purpose working registers all have single clock cycle access time allowing single-cycle arithmetic logic unit operation

It is possible to try writing to these registers any time, but the values are not altered.

The following registers are under CCP:

Table 10-2. CLKCTRL - Registers Under Configuration Change Protection

Register	Key
CLKCTRL.MCLKCTRLB	IOREG
CLKCTRL.MCLKLOCK	IOREG
CLKCTRL.MCLKCTRLA	IOREG
CLKCTRL.OSC20MCTRLA	IOREG
CLKCTRL.OSC20MCALIBA	IOREG
CLKCTRL.OSC20MCALIBB	IOREG
CLKCTRL.OSC32KCTRLA	IOREG

Related Links

Sequence for Write Operation to Configuration Change Protected I/O Registers

10.5.8 32 KHz Oscillator Control A

Name: OSC32KCTRLA
Offset: 0x18
Reset: 0x00
Property: Configuration Change Protection

Bit	7	6	5	4	3	2	1	0
							RUNSTDBY	
Access							R/W	
Reset							0	

Bit 1 – RUNSTDBY Run Standby
This bit forces the oscillator ON in all modes, even when unused by the system. In Standby Sleep mode this can be used to ensure immediate wake-up and not waiting for the oscillator start-up time.

When not requested by peripherals, no oscillator output is provided.

It takes four oscillator cycles to open the clock gate after a request but the oscillator analog start-up time will be removed when this bit is set.

Changes of the signal on a pin can trigger an interrupt. The exact conditions are defined by writing to the Input/Sense bit field (ISC) in PORT.PINnCTRL.

When setting or changing interrupt settings, take these points into account:

- If an INVEN bit is toggled in the same cycle as the interrupt setting, the edge caused by the inversion toggling may not cause an interrupt request.
- If an input is disabled while synchronizing an interrupt, that interrupt may be requested on re-enabling the input, even if it is re-enabled with a different interrupt setting.
- If the interrupt setting is changed while synchronizing an interrupt, that interrupt may not be accepted.
- Only a few pins support full asynchronous interrupt detection, see I/O Multiplexing and Considerations. These limitations apply for waking the system from sleep:

Interrupt Type	Fully Asynchronous Pins	Other Pins
BOTHEDGES	Will wake system	Will wake system
RISING	Will wake system	Will not wake system
FALLING	Will wake system	Will not wake system
LEVEL	Will wake system	Will wake system

Related Links

I/O Multiplexing and Considerations

16.3.3 Interrupts

Table 16-3. Available Interrupt Vectors and Sources

Offset	Name	Vector Description	Conditions
0x00	PORTx	PORT A, B, C interrupt	INTn in PORT.INTFLAGS is raised as configured by ISC bit in PORT.PINnCTRL.

Each port pin n can be configured as an interrupt source. Each interrupt can be individually enabled or disabled by writing to ISC in PORT.PINCTRL.

When an interrupt condition occurs, the corresponding interrupt flag is set in the Interrupt Flags register of the peripheral (*peripheral*.INTFLAGS).

An interrupt request is generated when the corresponding interrupt is enabled and the interrupt flag is set. The interrupt request remains active until the interrupt flag is cleared. See the peripheral's INTFLAGS register for details on how to clear interrupt flags.

18. Voltage Reference (VREF)

18.1 Features

- Programmable Voltage Reference Sources:
  - One for each ADC peripheral
  - One for each AC peripheral
- Each Reference Source Supports Five Different Voltages:
  - 0.55V
  - 1.1V
  - 1.5V
  - 2.5V
  - 4.3V

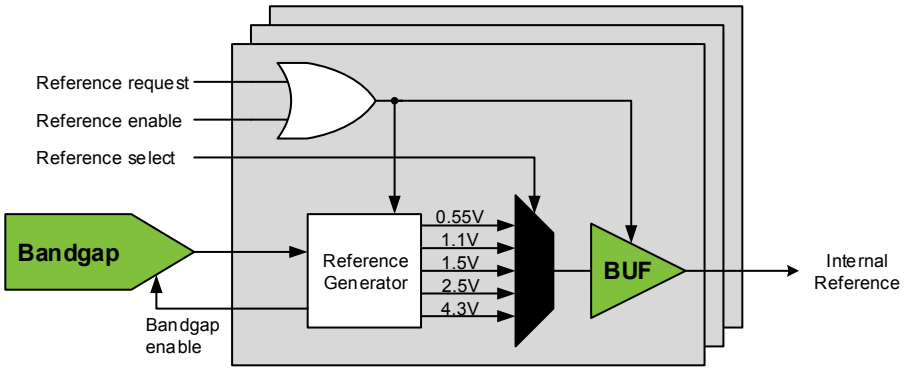
18.2 Overview

The Voltage Reference (VREF) peripheral provides control registers for the voltage reference sources used by several peripherals. The user can select the reference voltages for the ADC0 by writing to the ADC0 Reference Select bit field (ADC0REFSEL) in the Control A register (VREF.CTRLA), and for AC0 by writing to the AC0 Reference Select bit field DAC0REFSEL in VREF.CTRLA.

A voltage reference source is enabled automatically when requested by a peripheral. The user can enable the reference voltage sources (and thus, override the automatic disabling of unused sources) by writing to the respective Force Enable bit (ADC0REFEN) in the Control B register (VREF.CTRLB). This may be desirable to decrease start-up time, at the cost of increased power consumption.

18.2.1 Block Diagram

Figure 18-1. VREF Block Diagram



18.3 Functional Description

18.3.1 Initialization

The default configuration will enable the respective source when the ADC0, AC0 is requesting a reference voltage. The default reference voltages are 0.55V but can be configured by writing to the

19.2.3.2 I/O Lines and Connections
Not applicable.

19.2.3.3 Interrupts
Not applicable.

19.2.3.4 Events
Not applicable.

19.2.3.5 Debug Operation
When run-time debugging, this peripheral will continue normal operation. Halting the CPU in Debugging mode will halt normal operation of the peripheral.

When halting the CPU in Debug mode, the WDT counter is reset.

When starting the CPU again and the WDT was operating in Window mode, the first closed window time-out period will be disabled, and a Normal mode time-out period is executed.

Related Links

Window Mode

19.3 Functional Description

19.3.1 Initialization

- The WDT is enabled when a non-zero value is written to the Period bits (PERIOD) in the Control A register (WDT.CTRLA).
- Optional: Write a non-zero value to the Window bits (WINDOW) in WDT.CTRLA to enable Window mode operation.

All bits in the Control A register and the Lock bit (LOCK) in the STATUS register (WDT.STATUS) are write protected by the Configuration Change Protection mechanism.

The Reset value of WDT.CTRLA is defined by a fuse (FUSE.WDTCFG), so the WDT can be enabled at boot time. If this is the case, the LOCK bit in WDT.STATUS is set at boot time.

Related Links

Register Summary - WDT

19.3.2 Operation

19.3.2.1 Normal Mode
In Normal mode operation, a single time-out period is set for the WDT. If the WDT is not reset from software using the `WDR` any time before the time out occurs, the WDT will issue a system Reset.

A new WDT time-out period will be started each time the WDT is reset by `WDR`.

There are 11 possible WDT time-out periods (TO_{WDT}), selectable from 8 ms to 8s by writing to the Period bit field (PERIOD) in the Control A register (WDT.CTRLA).

20.5.2 Control B - Normal Mode

Name: CTRLB
Offset: 0x01
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
		CMP2EN	CMP1EN	CMP0EN	ALUPD	WGMODE[2:0]		
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bits 4, 5, 6 – CMPEN Compare n Enable
In the FRQ or PWM Waveform Generation mode, these bits will override the PORT output register for the corresponding pin.

Value	Description
0	Port output settings for the pin with WOn output respected
1	Port output settings for pin with WOn output overridden in FRQ or PWM Waveform Generation mode

Bit 3 – ALUPD Auto-Lock Update
The Auto-Lock Update feature controls the Lock Update (LUPD) bit in the TCAn.CTRLE register. When ALUPD is written to '1', LUPD will be set to '1' until the Buffer Valid (CMPnBV) bits of all enabled compare channels are '1'. This condition will clear LUPD.

It will remain cleared until the next UPDATE condition, where the buffer values will be transferred to the CMPn registers and LUPD will be set to '1' again. This makes sure that CMPnBUF register values are not transferred to the CMPn registers until all enabled compare buffers are written.

Value	Description
0	LUPD in TCA.CTRLE not altered by system
1	LUPD in TCA.CTRLE set and cleared automatically

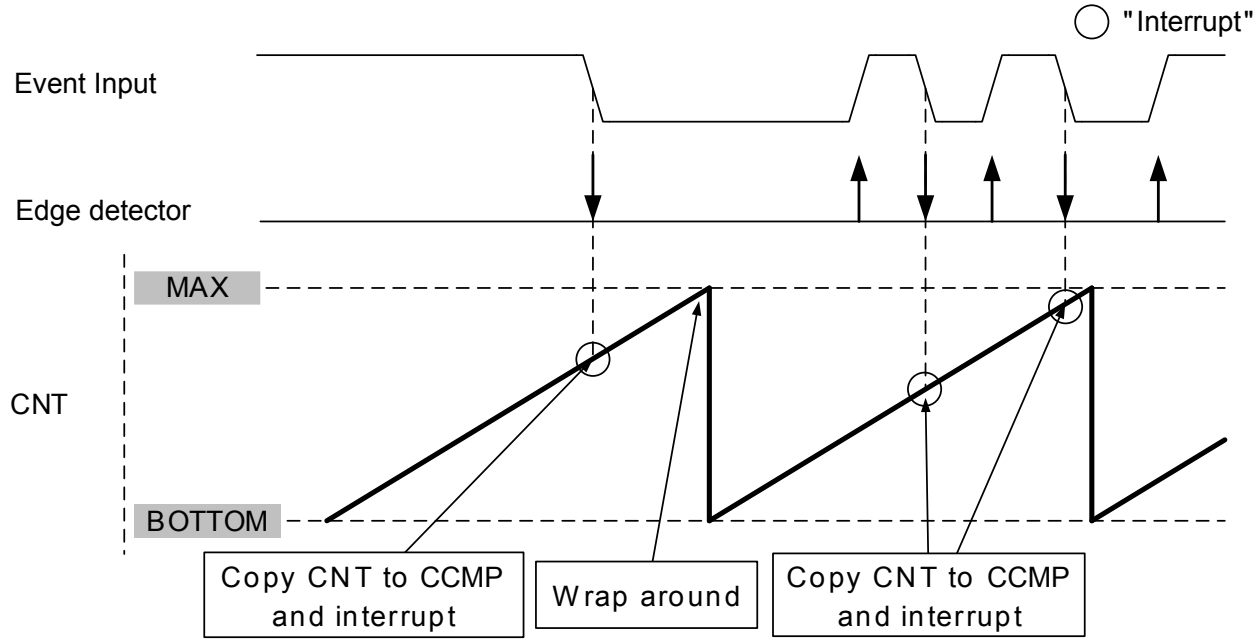
Bits 2:0 – WGMODE[2:0] Waveform Generation Mode
These bits select the Waveform Generation mode and control the counting sequence of the counter, TOP value, UPDATE condition, interrupt condition, and type of waveform that is generated.

No waveform generation is performed in the Normal mode of operation. For all other modes, the result from the waveform generator will only be directed to the port pins if the corresponding CMPnEN bit has been set to enable this. The port pin direction must be set as output.

Table 20-5. Timer Waveform Generation Mode

WGMODE[2:0]	Group Configuration	Mode of Operation	Top	Update	OVF
000	NORMAL	Normal	PER	TOP	TOP
001	FRQ	Frequency	CMP0	TOP	TOP
010	-	Reserved	-	-	-
011	SINGLESLOPE	Single-slope PWM	PER	BOTTOM	BOTTOM

Figure 21-4. Input Capture on Event



It is recommended to write zero to the TCBn.CNT register when entering this mode from any other mode.

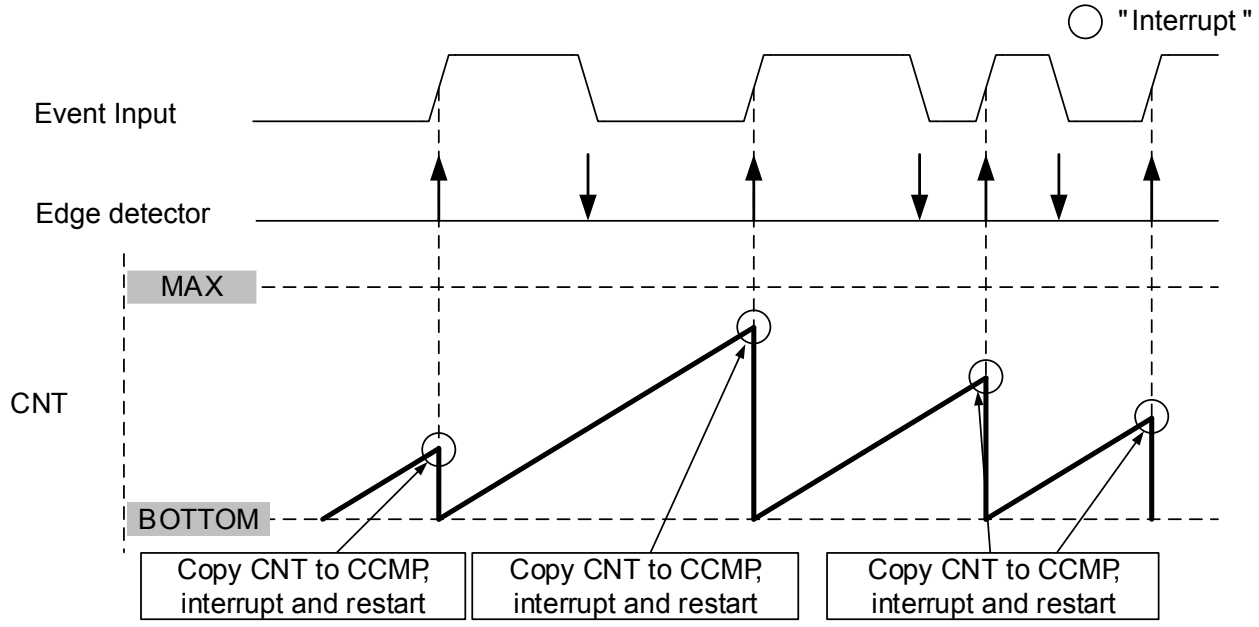
Input Capture Frequency Measurement Mode

In this mode, the TCB captures the counter value and restarts on either a positive or negative edge of the event input signal.

The interrupt flag is automatically cleared after the high byte of the Compare/Capture register (TCBn.CCMP) has been read, and an interrupt request is generated.

The figure below illustrates this mode when configured to act on rising edge.

Figure 21-5. Input Capture Frequency Measurement



- Event 3: Clock period = 1024 RTC clock cycles
- Event 4: Clock period = 512 RTC clock cycles
- Event 5: Clock period = 256 RTC clock cycles
- Event 6: Clock period = 128 RTC clock cycles
- Event 7: Clock period = 64 RTC clock cycles

The event users are configured by the Event System (EVSYS).

Related Links

Event System (EVSYS)

22.6 Interrupts

Table 22-2. Available Interrupt Vectors and Sources

Offset	Name	Vector Description	Conditions
0x00	RTC	Real-time counter overflow and compare match interrupt	• Overflow (OVF): The counter has reached its top value and wrapped to zero. • Compare (CMP): Match between the counter value and the compare register.
0x02	PIT	Periodic Interrupt Timer interrupt	A time period has passed, as configured in RTC_PITCTRLA.PERIOD.

When an interrupt condition occurs, the corresponding interrupt flag is set in the Interrupt Flags register of the peripheral (*peripheral*.INTFLAGS).

An interrupt source is enabled or disabled by writing to the corresponding enable bit in the peripheral's Interrupt Control register (*peripheral*.INTCTRL).

An interrupt request is generated when the corresponding interrupt source is enabled and the interrupt flag is set. The interrupt request remains active until the interrupt flag is cleared. See the peripheral's INTFLAGS register for details on how to clear interrupt flags.

Related Links

CPU Interrupt Controller (CPUINT)

INTCTRL

PITINTCTRL

22.7 Sleep Mode Operation

The RTC will continue to operate in Idle Sleep mode. It will run in Standby Sleep mode if the RUNSTDBY bit in RTC.CTRLA is set.

The PIT will continue to operate in any sleep mode.

Related Links

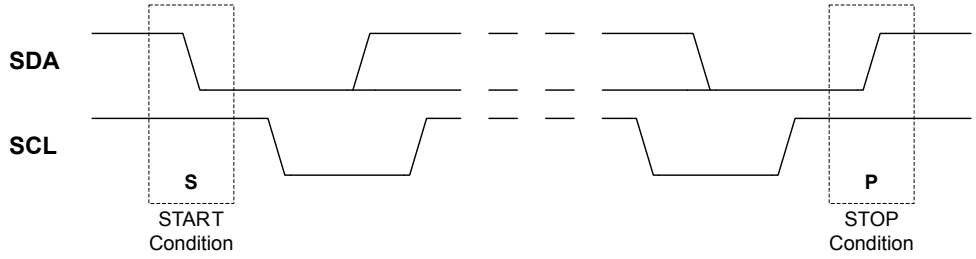
CTRLA

The master provides the clock signal for the transaction, but a device connected to the bus is allowed to stretch the low-level period of the clock to decrease the clock speed.

25.3.2.1 Start and Stop Conditions

Two unique bus conditions are used for marking the beginning (Start) and end (Stop) of a transaction. The master issues a Start condition (S) by indicating a high-to-low transition on the SDA line while the SCL line is kept high. The master completes the transaction by issuing a Stop condition (P), indicated by a low-to-high transition on the SDA line while the SCL line is kept high.

Figure 25-4. Start and Stop Conditions

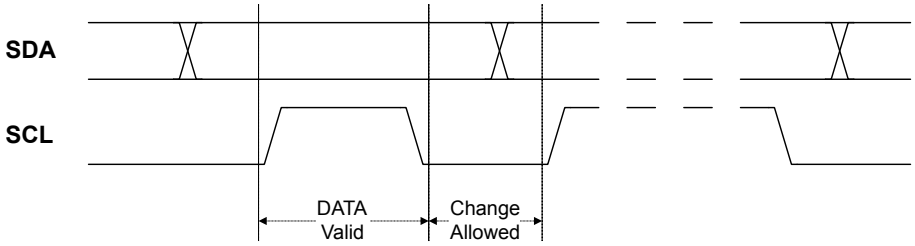


Multiple Start conditions can be issued during a single transaction. A Start condition that is not directly following a Stop condition is called a repeated Start condition (Sr).

25.3.2.2 Bit Transfer

As illustrated by Figure 25-5, a bit transferred on the SDA line must be stable for the entire high period of the SCL line. Consequently, the SDA value can only be changed during the low period of the clock. This is ensured in hardware by the TWI module.

Figure 25-5. Data Validity



Combining bit transfers result in the formation of address and data packets. These packets consist of eight data bits (one byte) with the Most Significant bit transferred first, plus a single-bit not-Acknowledge (NACK) or Acknowledge (ACK) response. The addressed device signals ACK by pulling the SCL line low during the ninth clock cycle, and signals NACK by leaving the line SCL high.

25.3.2.3 Address Packet

After the Start condition, a 7-bit address followed by a read/write (R/$\overline{W}$) bit is sent. This is always transmitted by the master. A slave recognizing its address will ACK the address by pulling the data line low for the next SCL cycle, while all other slaves should keep the TWI lines released and wait for the next Start and address. The address, R/$\overline{W}$ bit, and Acknowledge bit combined is the address packet. Only one address packet for each Start condition is allowed, also when 10-bit addressing is used.

The R/$\overline{W}$ bit specifies the direction of the transaction. If the R/$\overline{W}$ bit is low, it indicates a master write transaction, and the master will transmit its data after the slave has acknowledged its address. If the R/$\overline{W}$ bit is high, it indicates a master read transaction, and the slave will transmit its data after acknowledging its address.

28.5.2 Mux Control A

Name: MUXCTRLA
Offset: 0x02
Reset: 0x00
Property: -

AC.MUXCTRLA controls analog comparator muxes

Bit	7	6	5	4	3	2	1	0
	INVERT				MUXPOS		MUXNEG[1:0]	
Access	R/W				R/W		R/W	R/W
Reset	0				0		0	0

Bit 7 – INVERT Invert AC Output
Writing a '1' to this bit enables inversion of the output of the AC. This effectively inverts the input to all the peripherals connected to the signal, and affects the internal status signals.

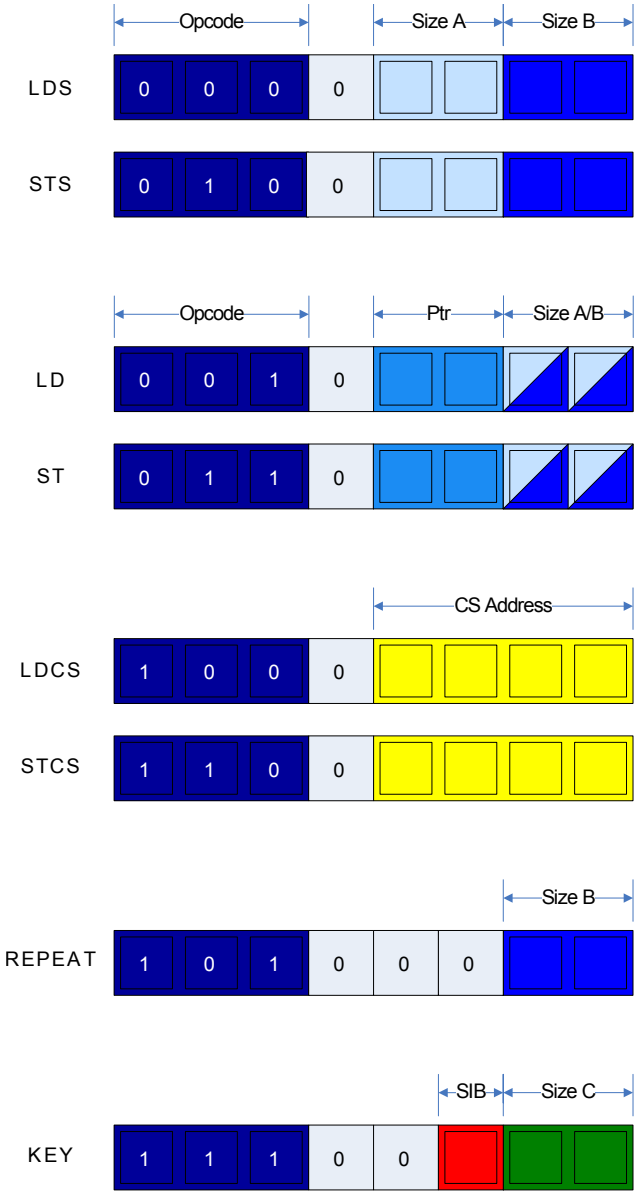
Bit 3 – MUXPOS Positive Input MUX Selection
Writing to this bit field selects the input signal to the positive input of the AC.

Value	Name	Description
0x0	AINP0	Positive Pin 0
0x1	AINP1	Positive Pin 1

Bits 1:0 – MUXNEG[1:0] Negative Input MUX Selection
Writing to this bit field selects the input signal to the negative input of the AC.

Value	Name	Description
0x0	AINN0	Negative Pin 0
0x1	AINN1	Negative Pin 1
0x2	VREF	Voltage Reference
0x3	Reserved	Reserved

Figure 30-8. UPDI Instruction Set Overview



OPCODE	
0 0 0	LDS
0 0 1	LD
0 1 0	STS
0 1 1	ST
1 0 0	LDCS (LDS Control/Status)
1 0 1	REPEAT
1 1 0	STCS (STS Control/Status)
1 1 1	KEY

Size A - Address size	
0 0	Byte
0 1	Word (2 Bytes)
1 0	Reserved
1 1	Reserved

Ptr - Pointer access	
0 0	*(ptr)
0 1	*(ptr++)
1 0	ptr
1 1	Reserved

Size B - Data size	
0 0	Byte
0 1	Word (2 Bytes)
1 0	Reserved
1 1	Reserved

CS Address (CS - Control/Status reg.)	
0 0 0 0	Reg 0
0 0 0 1	Reg 1
0 0 1 0	Reg 2
0 0 1 1	Reg 3
0 1 0 0	Reg 4 (ASI CS space)
.....	
1 1 1 1	Reserved

Size C - Key size	
0 0	64 bits (8 Bytes)
0 1	128 bits (16 Bytes)
1 0	Reserved
1 1	Reserved

SIB – System Information Block sel.	
0	Receive KEY
1	Send SIB

1. Enter the USERROW-Write KEY located in Table 30-6 by using the `KEY` instruction. See Table 30-6 for the UROWWRITE signature.
2. **Optional:** Read the UROWWRITE bit field in UPDI.ASI_KEY_STATUS to see that the KEY has been activated.
3. Write the Reset signature into the UPDI.ASI_RESET_REQ register. This will issue a System Reset.
4. Write 0x00 to the Reset signature in the UPDI.ASI_RESET_REQ register to clear the System Reset.
5. Read the UROWPROG bit in UPDI.ASI_SYS_STATUS.
6. User Row Programming can start when UROWPROG == 1. If UROWPROG == 0, go to point 5 again.
7. The writable area has a size of one EEPROM page, 32 bytes, and it is only possible to write User Row data to the first 32 byte addresses of the RAM. Addressing outside this memory range will result in a non-executed write. The data will map 1:1 with the User Row space when the data is copied into the User Row upon completion of the Programming sequence.
8. When all User Row data has been written to the RAM, write the UROWWRITEFINAL bit in UPDI.ASI_SYS_CTRLA.
9. Read the UROWPROG bit in UPDI.ASI_SYS_STATUS.
10. The User Row Programming is completed when UROWPROG == 0. If UROWPROG == 1, go to point 9 again.
11. Write the UROWWRITE bit in UPDI.ASI_KEY_STATUS.
12. Write the Reset signature into the UPDI.ASI_RESET_REQ register. This will issue a System Reset.
13. Write 0x00 to the Reset signature in the UPDI.ASI_RESET_REQ register to clear the System Reset.
14. User Row Programming is complete.

It is not possible to read back data from the SRAM in this mode. Only writing to the first 32 bytes of the SRAM is allowed.

30.3.8 Events

The UPDI is connected to the Event System (EVSYS) as described in the register *Asynchronous Channel n Generator Selection*.

The UPDI can generate the following output events:

- SYNCH Character Positive Edge Event

This event is set on the UPDI clock for each detected positive edge in the SYNCH character, and it is not possible to disable this event from the UPDI. The recommended application for this event is system clock frequency measurement through the UPDI. Section System Clock Measurement with UPDI provides the details on how to set up the system for this operation.

Related Links

Event System (EVSYS)

30.3.9 Sleep Mode Operation

The UPDI physical layer runs independently of all Sleep modes and the UPDI is always accessible for a connected debugger independent of the device Sleep mode. If the system enters a Sleep mode that turns the CPU clock OFF, the UPDI will not be able to access the system bus and read memories and peripherals. The UPDI physical layer clock is unaffected by the Sleep mode settings, as long as the UPDI

30.4 Register Summary - UPDI

Offset	Name	Bit Pos.								
0x00	STATUSA	7:0	UPDIREV[3:0]							
0x01	STATUSB	7:0						PESIG[2:0]		
0x02	CTRLA	7:0	IBDLY		PARD	DTD	RSD	GTVAL[2:0]		
0x03	CTRLB	7:0				NACKDIS	CCDETDIS	UPDIDIS		
0x04 ... 0x06	Reserved									
0x07	ASI_KEY_STATUS	7:0			UROWWRITE	NVMPROG	CHIPERASE			
0x08	ASI_RESET_REQ	7:0	RSTREQ[7:0]							
0x09	ASI_CTRLA	7:0							UPDICLKSEL[1:0]	
0x0A	ASI_SYS_CTRLA	7:0							UROWWRITE_FINAL	CLKREQ
0x0B	ASI_SYS_STATUS	7:0			RSTSYS	INSLEEP	NVMPROG	UROWPROG		LOCKSTATUS
0x0C	ASI_CRC_STATUS	7:0						CRC_STATUS[2:0]		

30.5 Register Description

These registers are readable only through the UPDI with special instructions and are NOT readable through the CPU.

Registers at offset addresses 0x0-0x3 are the UPDI Physical configuration registers.

Registers at offset addresses 0x4-0xC are the ASI level registers.

30.5.6 ASI Reset Request

Name: ASI_RESET_REQ
Offset: 0x08
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
	RSTREQ[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – RSTREQ[7:0] Reset Request
A Reset is signalized to the System when writing the Reset signature 0x59h to this address.

Writing any other signature to this register will clear the Reset.

When reading this register, reading bit RSTREQ[0] will tell if the UPDI is holding an active Reset on the system. If this bit is '1', the UPDI has an active Reset request to the system. All other bits will read as '0'.

The UPDI will not be reset when issuing a System Reset from this register.

Figure 32-3. ATtiny406: Active Supply Current vs. Temperature (f=20 MHz OSC20M)

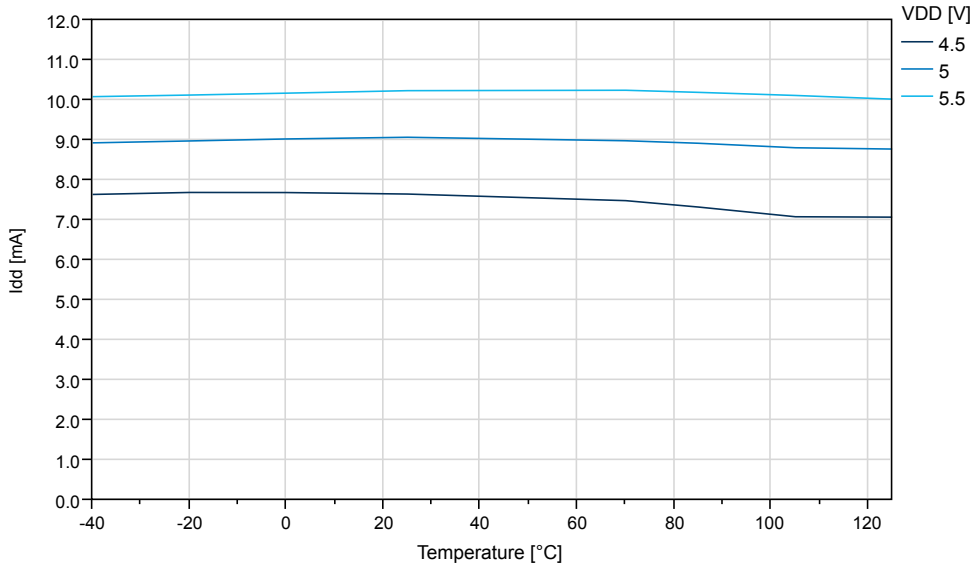


Figure 32-4. ATtiny406: Active Supply Current vs. V_{DD} (f=[1.25, 20] MHz OSC20M) at T=25°C

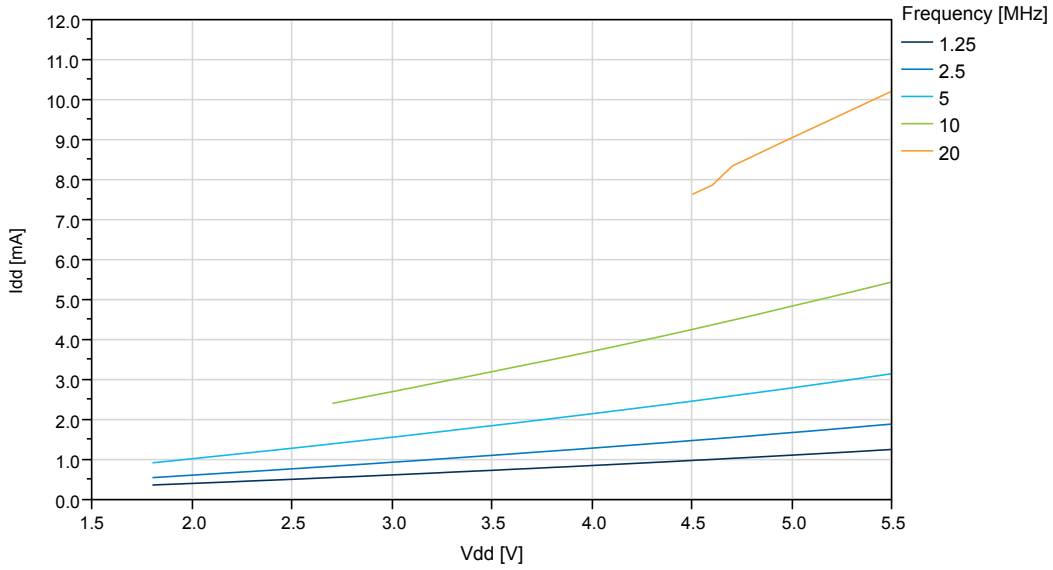


Figure 32-39. BOD Threshold vs. Temperature (Level 2.6V)

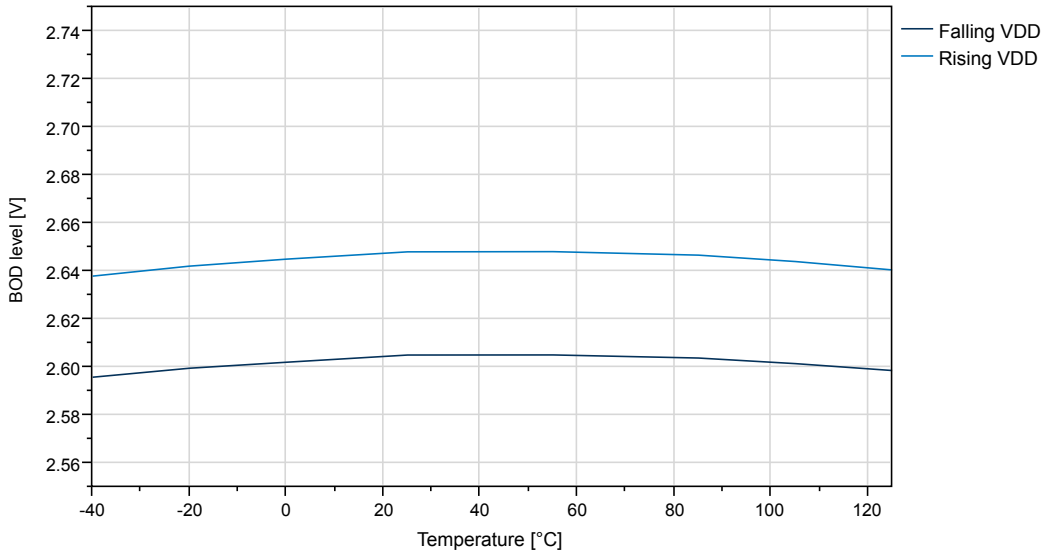
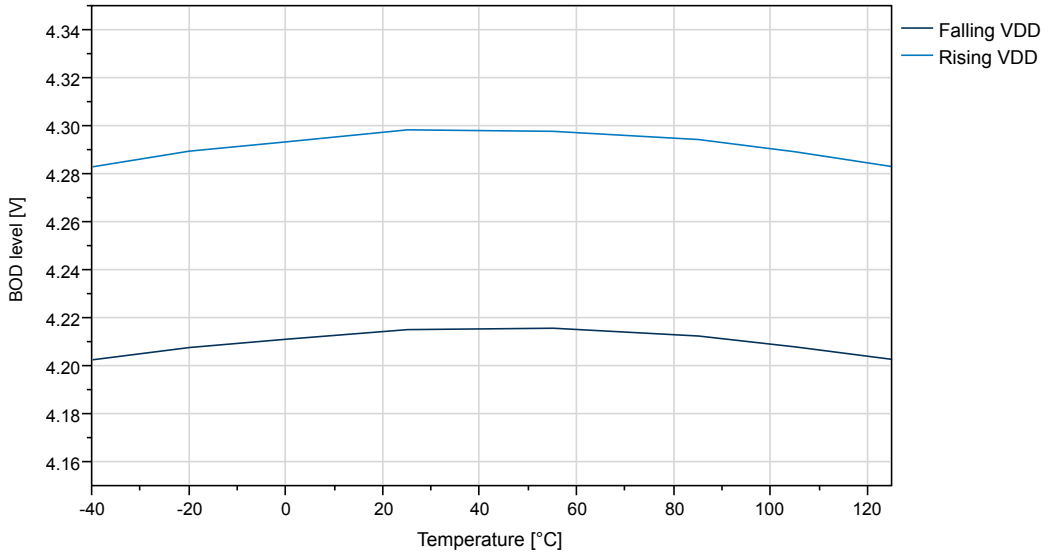


Figure 32-40. BOD Threshold vs. Temperature (Level 4.3V)



32.6 AC Characteristics

Figure 32-51. Hysteresis vs. V_{CM} - 10 mV (V_{DD}=5V)

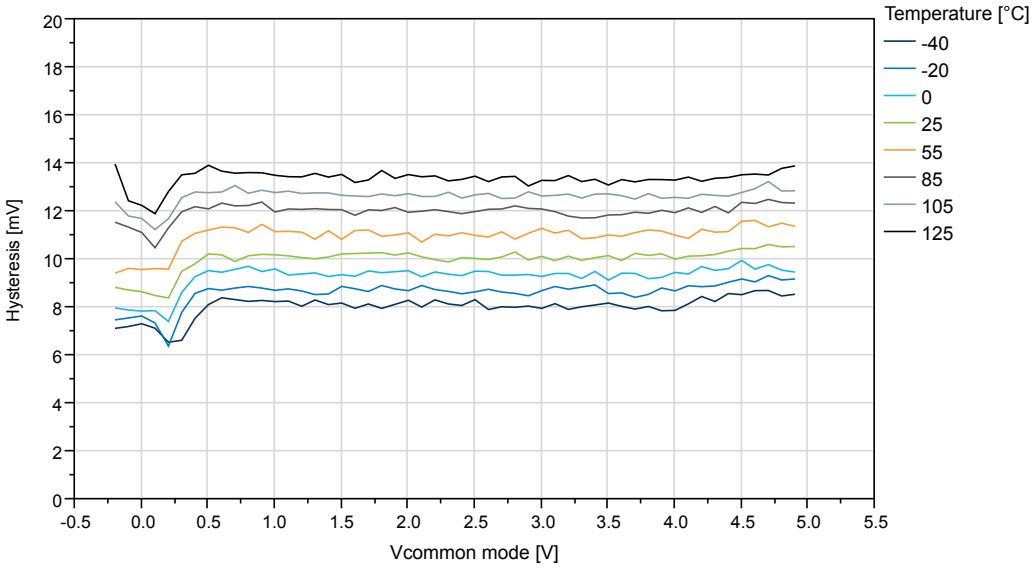


Figure 32-52. Hysteresis vs. V_{CM} - 10 mV to 50 mV (V_{DD}=5V, T=25°C)