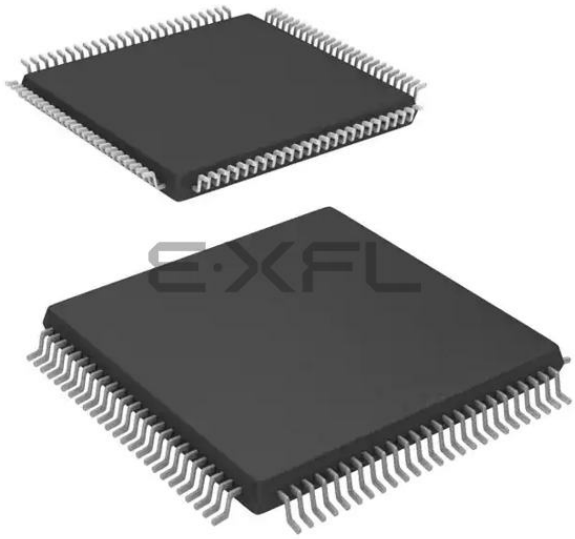
Infineon Technologies - CY8C3444AXI-116 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	EBI/EMI, I²C, LINbus, SPI, UART/USART
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	62
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3444axi-116

Figure 1-1 illustrates the major components of the CY8C34 family. They are:

- 8051 CPU Subsystem
- Nonvolatile Subsystem
- Programming, Debug, and Test Subsystem
- Inputs and Outputs
- Clocking
- Power
- Digital Subsystem
- Analog Subsystem

PSoC's digital subsystem provides half of its unique configurability. It connects a digital signal from any peripheral to any pin through the Digital System Interconnect (DSI). It also provides functional flexibility through an array of small, fast, low power Universal Digital Blocks (UDBs). PSoC Creator provides a library of pre-built and tested standard digital peripherals (UART, SPI, LIN, PRS, CRC, timer, counter, PWM, AND, OR, and so on) that are mapped to the UDB array. The designer can also easily create a digital circuit using boolean primitives by means of graphical design entry. Each UDB contains Programmable Array Logic (PAL)/Programmable Logic Device (PLD) functionality, together with a small state machine engine to support a wide variety of peripherals.

In addition to the flexibility of the UDB array, PSoC also provides configurable digital blocks targeted at specific functions. For the CY8C34 family these blocks can include four 16-bit timer, counter, and PWM blocks; I^2C slave, master, and multi-master; Full-Speed USB; and Full CAN 2.0b.

For more details on the peripherals see the "Example Peripherals" section on page 35 of this data sheet. For information on UDBs, DSI, and other digital blocks, see the "Digital Subsystem" section on page 35 of this data sheet.

PSoC's analog subsystem is the second half of its unique configurability. All analog performance is based on a highly accurate absolute voltage reference with less than 0.9% error over temperature and voltage. The configurable analog subsystem includes:

- Analog muxes
- Comparators
- Voltage references
- Analog-to-Digital Converter (ADC)
- Digital-to-Analog Converters (DACs)

All GPIO pins can route analog signals into and out of the device using the internal analog bus. This allows the device to interface up to 62 discrete analog signals. The heart of the analog subsystem is a fast, accurate, configurable Delta-Sigma ADC with these features:

- Less than 100 µV offset
- A gain error of 0.2%
- Integral Non Linearity (INL) less than 1 LSB
- Differential Non Linearity (DNL) less than 1 LSB
- Signal-to-noise ratio (SNR) better than 70 dB (Delta-Sigma) in 12-bit mode

This converter addresses a wide variety of precision analog applications including some of the most demanding sensors.

Two high speed voltage or current DACs support 8-bit output signals at update rate of 8 Msps in current DAC (IDAC) and 1 Msps in voltage DAC (VDAC). They can be routed out of any GPIO pin. You can create higher resolution voltage PWM DAC outputs using the UDB array. This can be used to create a pulse width modulated (PWM) DAC of up to 10 bits, at up to 48 kHz. The digital DACs in each UDB support PWM, PRS, or delta-sigma algorithms with programmable widths.

In addition to the ADC and DACs, the analog subsystem provides multiple:

- Uncommitted opamps
- Configurable Switched Capacitor/Continuous Time (SC/CT) blocks. These support:
  - Transimpedance amplifiers
  - Programmable gain amplifiers
  - Mixers
  - Other similar analog components

See the "Analog Subsystem" section on page 48 of this data sheet for more details.

PSoC's 8051 CPU subsystem is built around a single cycle pipelined 8051 8-bit processor running at up to 50 MHz. The CPU subsystem includes a programmable nested vector interrupt controller, DMA controller, and RAM. PSoC's nested vector interrupt controller provides low latency by allowing the CPU to vector directly to the first address of the interrupt service routine, bypassing the jump instruction required by other architectures. The DMA controller enables peripherals to exchange data without CPU involvement. This allows the CPU to run slower (saving power) or use those CPU cycles to improve the performance of firmware algorithms. The single cycle 8051 CPU runs ten times faster than a standard 8051 processor. The processor speed itself is configurable allowing active power consumption to be tuned for specific applications.

PSoC's nonvolatile subsystem consists of flash, byte-writeable EEPROM, and nonvolatile configuration options. It provides up to 64 KB of on-chip flash. The CPU can reprogram individual blocks of flash, enabling boot loaders. The designer can enable an Error Correcting Code (ECC) for high reliability applications. A powerful and flexible protection model secures the user's sensitive information, allowing selective memory block locking for read and write protection. Up to 2 KB of byte-writable EEPROM is available on-chip to store application data. Additionally, selected configuration options such as boot speed and pin drive mode are stored in nonvolatile memory. This allows settings to activate immediately after power on reset (POR).

The three types of PSoC I/O are extremely flexible. All I/Os have many drive modes that are set at POR. PSoC also provides up to four I/O voltage domains through the Vddio pins. Every GPIO has analog I/O, LCD drive[1], CapSense[4], flexible interrupt generation, slew rate control, and digital I/O capability. The SIOs on PSoC allow Voh to be set independently of Vddio when used as outputs. When SIOs are in input mode they are high impedance. This is true even when the device is not powered or when the pin voltage goes above the supply voltage. This makes the SIO ideally suited for use on an I^2C bus where the PSoC may not be powered when other devices on the bus are. The SIO pins also have high current sink capability for applications such as LED drives. The programmable input threshold feature of the SIO can be used to make the SIO function as a general purpose analog comparator. For devices with Full-Speed USB the USB physical interface is also provided (USBIO). When not using USB these pins may also be used for limited digital functionality and device programming. All the features of the PSoC I/Os are covered in detail in the "I/O System and Routing" section on page 29 of this data sheet.

The PSoC device incorporates flexible internal clock generators, designed for high stability and factory trimmed for high accuracy. The Internal Main Oscillator (IMO) is the master clock base for the system, and has 1% accuracy at 3 MHz. The IMO can be configured to run from 3 MHz up to 24 MHz. Multiple clock derivatives can be generated from the main clock frequency to meet application needs. The device provides a PLL to generate system clock frequencies up to 50 MHz from the IMO, external crystal, or external reference clock. It also contains a separate, very low power Internal Low Speed Oscillator (ILO) for the sleep and watchdog timers. A 32.768 kHz external watch crystal is also supported for use in Real Time Clock (RTC) applications. The clocks, together with programmable clock dividers, provide the flexibility to integrate most timing requirements.

The CY8C34 family supports a wide supply operating range from 1.71 to 5.5V. This allows operation from regulated supplies such as 1.8 ± 5%, 2.5V ±10%, 3.3V ± 10%, or 5.0V ± 10%, or directly from a wide range of battery types. In addition, it provides an integrated high efficiency synchronous boost converter that can power the device from supply voltages as low as 0.5V. This enables the device to be powered directly from a single battery or solar cell. In addition, the designer can use the boost converter to generate other voltages required by the device, such as a 3.3V supply for LCD glass drive. The boost's output is available on the Vboost pin, allowing other devices in the application to be powered from the PSoC.

PSoC supports a wide range of low power modes. These include a 200 nA hibernate mode with RAM retention and a 1 µA sleep mode with real time clock (RTC). In the second mode the optional 32.768 kHz watch crystal runs continuously and maintains an accurate RTC.

Power to all major functional blocks, including the programmable digital and analog peripherals, can be controlled independently by firmware. This allows low power background processing when some peripherals are not in use. This, in turn, provides a total device current of only 1.2 mA when the CPU is running at 6 MHz or 0.8 mA running at 3 MHz.

The details of the PSoC power modes are covered in the "Power System" section on page 25 of this data sheet.

PSoC uses JTAG (4 wire) or Serial Wire Debug (SWD) (2 wire) interfaces for programming, debug, and test. The 1-wire Single Wire Viewer (SWV) may also be used for "printf" style debugging. By combining SWD and SWV, the designer can implement a full debugging interface with just three pins. Using these standard interfaces enables the designer to debug or program the PSoC with a variety of hardware solutions from Cypress or third party vendors. PSoC supports on-chip break points and 4 KB instruction and data race memory for debug. Details of the programming, test, and debugging interfaces are discussed in the "Programming, Debug Interfaces, Resources" section on page 57 of this data sheet.

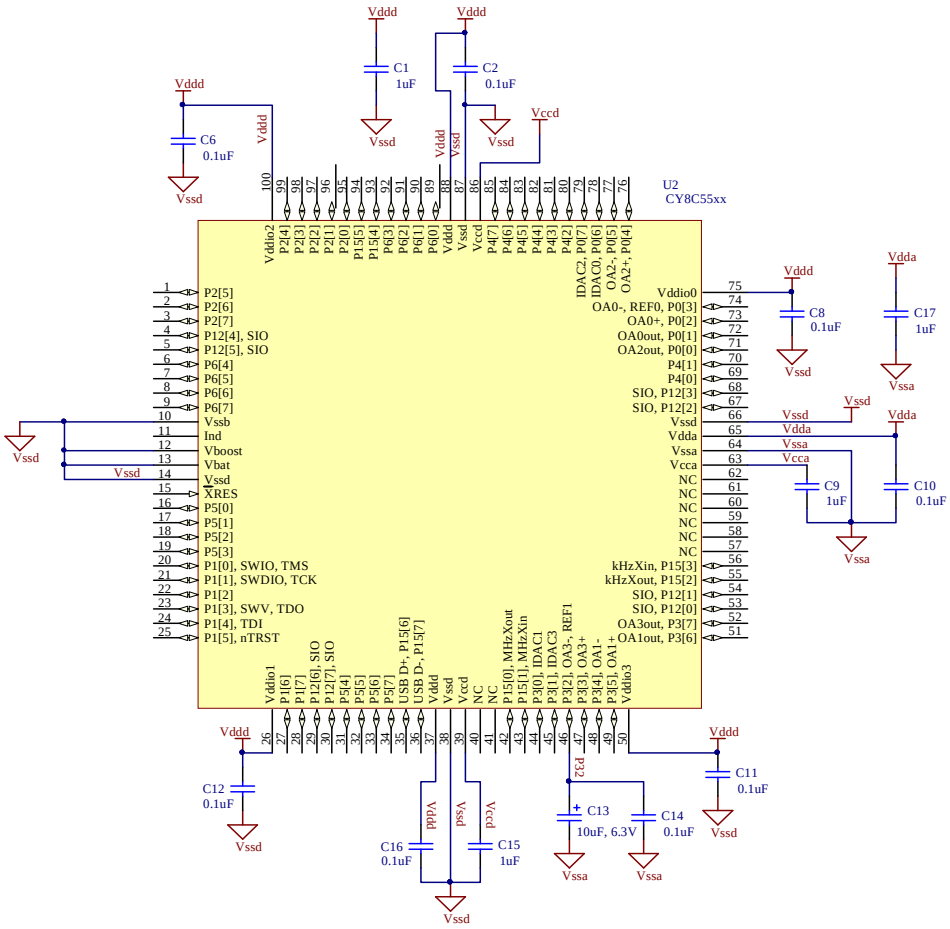
2. Pinouts

The Vddio pin that supplies a particular set of pins is indicated by the black lines drawn on the pinout diagrams in Figure 2-1 through Figure 2-4. Using the Vddio pins, a single PSoC can support multiple interface voltage levels, eliminating the need for off-chip level shifters. Each Vddio may sink up to 100 mA total to its associated I/O pins and opamps. On the 68 pin and 100 pin devices each set of Vddio associated pins may sink up to 100 mA. The 48 pin device may sink up to 100 mA total for all Vddio0 plus Vddio2 associated I/O pins and 100 mA total for all Vddio1 plus Vddio3 associated I/O pins.

Figure 2-5 and Figure 2-6 show an example schematic and an example PCB layout, for the 100-pin TQFP part, for optimal analog performance on a 2-layer board.

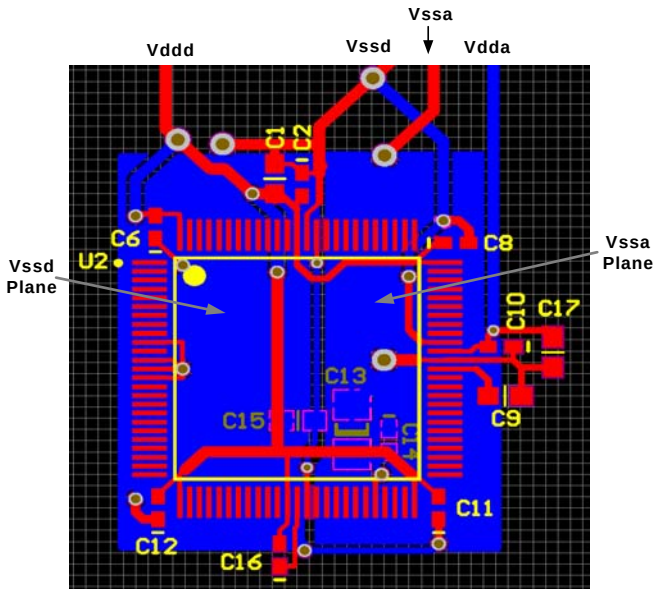
- The two pins labeled Vddd must be connected together.
- The two pins labeled Vccd must be connected together, with capacitance added, as shown in Figure 2-5 and Power System on page 25. The trace between the two Vccd pins should be as short as possible.
- The two pins labeled Vssd must be connected together.

Figure 2-5. Example Schematic for 100-Pin TQFP Part with Power Connections



Note The two Vccd pins must be connected together with as short a trace as possible. A trace under the device is recommended, as shown in Figure 2-6.

Figure 2-6. Example PCB Layout for 100-Pin TQFP Part for Optimal Analog Performance



3. Pin Descriptions

IDAC0, IDAC2. Low resistance output pin for high current DACs (IDAC).

OpAmp0out, OpAmp2out. High current output of uncommitted opamp[4].

Extref0, Extref1. External reference input to the analog system.

OpAmp0-, OpAmp2-. Inverting input to uncommitted opamp.

OpAmp0+, OpAmp2+. Noninverting input to uncommitted opamp.

GPIO. General purpose I/O pin provides interfaces to the CPU, digital peripherals, analog peripherals, interrupts, LCD segment drive, and CapSense[4].

I2C0: SCL, I2C1: SCL. I^2C SCL line providing wake from sleep on an address match. Any I/O pin can be used for I^2C SCL if wake from sleep is not required.

I2C0: SDA, I2C1: SDA. I^2C SDA line providing wake from sleep on an address match. Any I/O pin can be used for I^2C SDA if wake from sleep is not required.

Ind. Inductor connection to boost pump.

kHz XTAL: Xo, kHz XTAL: Xi. 32.768 kHz crystal oscillator pin.

MHz XTAL: Xo, MHz XTAL: Xi. 4 to 33 MHz crystal oscillator pin.

nTRST. Optional JTAG Test Reset programming and debug port connection to reset the JTAG connection.

SIO. Special I/O provides interfaces to the CPU, digital peripherals and interrupts with a programmable high threshold voltage, analog comparator, high sink current, and high impedance state when the device is unpowered.

SWDCK. Serial Wire Debug Clock programming and debug port connection.

SWDIO. Serial Wire Debug Input and Output programming and debug port connection.

SWV. Single Wire Viewer debug output.

TCK. JTAG Test Clock programming and debug port connection.

TDI. JTAG Test Data In programming and debug port connection.

TDO. JTAG Test Data Out programming and debug port connection.

TMS. JTAG Test Mode Select programming and debug port connection.

USBIO, D+. Provides D+ connection directly to a USB 2.0 bus. May be used as a digital I/O pin. Pins are No Connect (NC) on devices without USB.[2]

USBIO, D-. Provides D- connection directly to a USB 2.0 bus. May be used as a digital I/O pin. Pins are No Connect (NC) on devices without USB.[2]

Vboost. Power sense connection to boost pump.

Vbat. Battery supply to boost pump.

Vcca. Output of analog core regulator and input to analog core. Requires a 1 µF capacitor to Vssa. Regulator output not for external use.

Vccd. Output of digital core regulator and input to digital core. The two Vccd pins must be shorted together, with the trace between them as short as possible, and a 1 µF capacitor to Vssd; see Power System on page 25. Regulator output not for external use.

Note
4. GPIOs with OpAmp outputs are not recommended for use with CapSense.

Table 4-3. Data Transfer Instructions (continued)

Mnemonic	Description	Bytes	Cycles
MOV @Ri, Direct	Move direct byte to indirect RAM	2	3
MOV @Ri, #data	Move immediate data to indirect RAM	2	2
MOV DPTR, #data16	Load data pointer with 16 bit constant	3	3
MOVC A, @A+DPTR	Move code byte relative to DPTR to accumulator	1	5
MOVC A, @A + PC	Move code byte relative to PC to accumulator	1	4
MOVX A,@Ri	Move external RAM (8 bit) to accumulator	1	3
MOVX A, @DPTR	Move external RAM (16 bit) to accumulator	1	2
MOVX @Ri, A	Move accumulator to external RAM (8 bit)	1	4
MOVX @DPTR, A	Move accumulator to external RAM (16 bit)	1	3
PUSH Direct	Push direct byte onto stack	2	3
POP Direct	Pop direct byte from stack	2	2
XCH A, Rn	Exchange register with accumulator	1	2
XCH A, Direct	Exchange direct byte with accumulator	2	3
XCH A, @Ri	Exchange indirect RAM with accumulator	1	3
XCHD A, @Ri	Exchange low order indirect digit RAM with accumulator	1	3

Table 4-4. Boolean Instructions

Mnemonic	Description	Bytes	Cycles
CLR C	Clear carry	1	1
CLR bit	Clear direct bit	2	3
SETB C	Set carry	1	1
SETB bit	Set direct bit	2	3
CPL C	Complement carry	1	1
CPL bit	Complement direct bit	2	3
ANL C, bit	AND direct bit to carry	2	2
ANL C, /bit	AND complement of direct bit to carry	2	2
ORL C, bit	OR direct bit to carry	2	2
ORL C, /bit	OR complement of direct bit to carry	2	2
MOV C, bit	Move direct bit to carry	2	2
MOV bit, C	Move carry to direct bit	2	3
JC rel	Jump if carry is set	2	3
JNC rel	Jump if no carry is set	2	3
JB bit, rel	Jump if direct bit is set	3	5
JNB bit, rel	Jump if direct bit is not set	3	5
JBC bit, rel	Jump if direct bit is set and clear bit	3	5

4.4.4.7 Nested DMA

One TD may modify another TD, as the TD configuration space is memory mapped similar to any other peripheral. For example, a first TD loads a second TD's configuration and then calls the second TD. The second TD moves data as required by the application. When complete, the second TD calls the first TD, which again updates the second TD's configuration. This process repeats as often as necessary.

4.5 Interrupt Controller

The interrupt controller provides a mechanism for hardware resources to change program execution to a new address, independent of the current task being executed by the main code. The interrupt controller provides enhanced features not found on original 8051 interrupt controllers:

- 32 interrupt vectors
- Jumps directly to ISR anywhere in code space with dynamic vector addresses
- Multiple sources for each vector
- Flexible interrupt to vector matching
- Each interrupt vector is independently enabled or disabled
- Each interrupt can be dynamically assigned one of eight priorities
- Eight level nestable interrupts
- Multiple I/O interrupt vectors
- Software can send interrupts
- Software can clear pending interrupts

When an interrupt is pending, the current instruction is completed and the program counter is pushed onto the stack. Code execution then jumps to the program address provided by the vector. After the ISR is completed, a RETI instruction is executed and returns execution to the instruction following the previously interrupted instruction. To do this the RETI instruction pops the program counter from the stack.

If the same priority level is assigned to two or more interrupts, the interrupt with the lower vector number is executed first. Each interrupt vector may choose from three interrupt sources: Fixed Function, DMA, and UDB. The fixed function interrupts are direct connections to the most common interrupt sources and provide the lowest resource cost connection. The DMA interrupt sources provide direct connections to the two DMA interrupt sources provided per DMA channel. The third interrupt source for vectors is from the UDB digital routing array. This allows any digital signal available to the UDB array to be used as an interrupt source. Fixed function interrupts and all interrupt sources may be routed to any interrupt vector using the UDB interrupt source connections.

Table 4-8. Interrupt Vector Table

#	Fixed Function	DMA	UDB
0	LVD	phub_termout0[0]	udb_intr[0]
1	ECC	phub_termout0[1]	udb_intr[1]
2	Reserved	phub_termout0[2]	udb_intr[2]
3	Sleep (Pwr Mgr)	phub_termout0[3]	udb_intr[3]
4	PICU[0]	phub_termout0[4]	udb_intr[4]
5	PICU[1]	phub_termout0[5]	udb_intr[5]
6	PICU[2]	phub_termout0[6]	udb_intr[6]
7	PICU[3]	phub_termout0[7]	udb_intr[7]
8	PICU[4]	phub_termout0[8]	udb_intr[8]
9	PICU[5]	phub_termout0[9]	udb_intr[9]
10	PICU[6]	phub_termout0[10]	udb_intr[10]
11	PICU[12]	phub_termout0[11]	udb_intr[11]
12	PICU[15]	phub_termout0[12]	udb_intr[12]
13	Comparators Combined	phub_termout0[13]	udb_intr[13]
14	Switched Caps Combined	phub_termout0[14]	udb_intr[14]
15	I^2C	phub_termout0[15]	udb_intr[15]
16	CAN	phub_termout1[0]	udb_intr[16]
17	Timer/Counter0	phub_termout1[1]	udb_intr[17]
18	Timer/Counter1	phub_termout1[2]	udb_intr[18]
19	Timer/Counter2	phub_termout1[3]	udb_intr[19]
20	Timer/Counter3	phub_termout1[4]	udb_intr[20]
21	USB SOF Int	phub_termout1[5]	udb_intr[21]
22	USB Arb Int	phub_termout1[6]	udb_intr[22]
23	USB Bus Int	phub_termout1[7]	udb_intr[23]
24	USB Endpoint[0]	phub_termout1[8]	udb_intr[24]
25	USB Endpoint Data	phub_termout1[9]	udb_intr[25]
26	Reserved	phub_termout1[10]	udb_intr[26]
27	Reserved	phub_termout1[11]	udb_intr[27]
28	Reserved	phub_termout1[12]	udb_intr[28]
29	Decimator Int	phub_termout1[13]	udb_intr[29]
30	PHUB Error Int	phub_termout1[14]	udb_intr[30]
31	EEPROM Fault Int	phub_termout1[15]	udb_intr[31]

5. Memory

5.1 Static RAM

CY8C34 Static RAM (SRAM) is used for temporary data storage. Up to 8 KB of SRAM is provided and can be accessed by the 8051 or the DMA controller. See the “Memory Map” section on page 19. Simultaneous access of SRAM by the 8051 and the DMA controller is possible if different 4 KB blocks are accessed.

5.2 Flash Program Memory

Flash memory in PSoC devices provides nonvolatile storage for user firmware, user configuration data, bulk data storage, and optional ECC data. The main flash memory area contains up to 64 KB of user program space.

Up to an additional 8 KB of flash space is available for Error Correcting Codes (ECC). If ECC is not used this space can store device configuration data and bulk user data. User code may not be run out of the ECC flash memory section. ECC can correct one bit error and detect two bit errors per 8 bytes of firmware memory; an interrupt can be generated when an error is detected.

Flash is read in units of rows; each row is 9 bytes wide with 8 bytes of data and 1 byte of ECC data. When a row is read, the data bytes are copied into an 8-byte instruction buffer. The CPU fetches its instructions from this buffer, for improved CPU performance.

Flash programming is performed through a special interface and preempts code execution out of flash. The flash programming interface performs flash erasing, programming and setting code protection levels. Flash In System Serial Programming (ISSP), typically used for production programming, is possible through both the SWD and JTAG interfaces. In-system programming, typically used for bootloaders, is also possible using serial interfaces such as I^2C, USB, UART, and SPI, or any communications protocol.

5.3 Flash Security

All PSoC devices include a flexible flash protection model that prevents access and visibility to on-chip flash memory. This prevents duplication or reverse engineering of proprietary code. Flash memory is organized in blocks, where each block contains 256 bytes of program or data and 32 bytes of ECC or configuration data. A total of up to 256 blocks are provided on 64 KB flash devices.

The device offers the ability to assign one of four protection levels to each row of flash. Table 5-1 lists the protection modes available. Flash protection levels can only be changed by performing a complete flash erase. The Full Protection and Field Upgrade settings disable external access (through a debugging tool such as PSoC Creator, for example). If your application requires code update through a boot loader, then use the Field Upgrade setting. Use the Unprotected setting only when no security is needed in your application. The PSoC device also offers an advanced security feature called Device Security which permanently disables all test, programming, and debug ports, protecting your application from external access (see the “Device Security” section on page 58). For more information on how to take full advantage of the security features in PSoC, see the PSoC 3 TRM.

Table 5-1. Flash Protection

Protection Setting	Allowed	Not Allowed
Unprotected	External read and write + internal read and write	-
Factory Upgrade	External write + internal read and write	External read
Field Upgrade	Internal read and write	External read and write
Full Protection	Internal read	External read and write + internal write

Disclaimer

Note the following details of the flash code protection features on Cypress devices.

Cypress products meet the specifications contained in their particular Cypress data sheets. Cypress believes that its family of products is one of the most secure families of its kind on the market today, regardless of how they are used. There may be methods, unknown to Cypress, that can breach the code protection features. Any of these methods, to our knowledge, would be dishonest and possibly illegal. Neither Cypress nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Cypress is willing to work with the customer who is concerned about the integrity of their code. Code protection is constantly evolving. We at Cypress are committed to continuously improving the code protection features of our products.

5.4 EEPROM

PSoC EEPROM memory is a byte addressable nonvolatile memory. The CY8C34 has up to 2 KB of EEPROM memory to store user data. Reads from EEPROM are random access at the byte level. Reads are done directly; writes are done by sending write commands to an EEPROM programming interface. CPU code execution can continue from flash during EEPROM writes. EEPROM is erasable and writeable at the row level. The EEPROM is divided into 128 rows of 16 bytes each.

The CPU can not execute out of EEPROM. There is no ECC hardware associated with EEPROM. If ECC is required it must be handled in firmware.

5.5 External Memory Interface

CY8C34 provides an External Memory Interface (EMIF) for connecting to external memory devices. The connection allows read and write accesses to external memories. The EMIF operates in conjunction with UDBs, I/O ports, and other hardware to generate external memory address and control signals.

Figure 5-1 is the EMIF block diagram. The EMIF supports synchronous and asynchronous memories. The CY8C34 supports only one type of external memory device at a time.

External memory can be accessed via the 8051 xdata space; up to 24 address bits can be used. See “xdata Space” section on page 21. The memory can be 8 or 16 bits wide.

Table 6-2. Power Modes

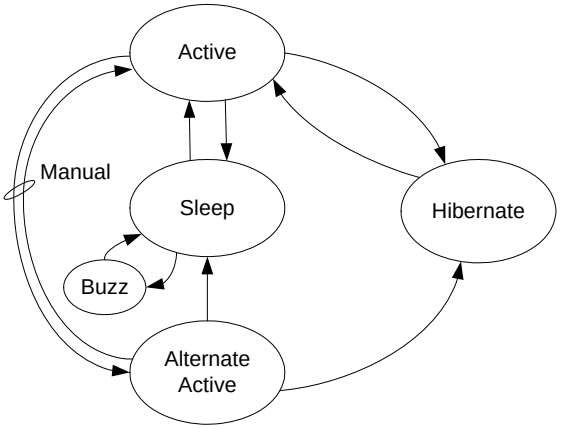
Power Modes	Description	Entry Condition	Wakeup Source	Active Clocks	Regulator
Active	Primary mode of operation, all peripherals available (programmable)	Wakeup, reset, manual register entry	Any interrupt	Any (programmable)	All regulators available. Digital and analog regulators can be disabled if external regulation used.
Alternate Active	Similar to Active mode, and is typically configured to have fewer peripherals active to reduce power. One possible configuration is to turn off the CPU and flash, and run peripherals at full speed	Manual register entry	Any interrupt	Any (programmable)	All regulators available. Digital and analog regulators can be disabled if external regulation used.
Sleep	All subsystems automatically disabled	Manual register entry	Comparator, PICU, I^2C, RTC, CTW, LVD	ILO/kHzECO	Both digital and analog regulators buzzed. Digital and analog regulators can be disabled if external regulation used.
Hibernate	All subsystems automatically disabled Lowest power consuming mode with all peripherals and internal regulators disabled, except hibernate regulator is enabled Configuration and memory contents retained	Manual register entry	PICU		Only hibernate regulator active.

Table 6-3. Power Modes Wakeup Time and Power Consumption

Sleep Modes	Wakeup Time	Current (typ)	Code Execution	Digital Resources	Analog Resources	Clock Sources Available	Wakeup Sources	Reset Sources
Active	-	1.2 mA[1]	Yes	All	All	All	-	All
Alternate Active	-	TBD	User defined	All	All	All	-	All
Sleep	<15 µs	1 µA	No	I^2C	Comparator	ILO/kHzECO	Comparator, PICU, I^2C, RTC, CTW, LVD	XRES, LVD, WDR
Hibernate	<100 µs	200 nA	No	None	None	None	PICU	XRES

1. IMO 6 MHz, CPU 6 MHz, all peripherals disabled.

Figure 6-5. Power Mode Transitions

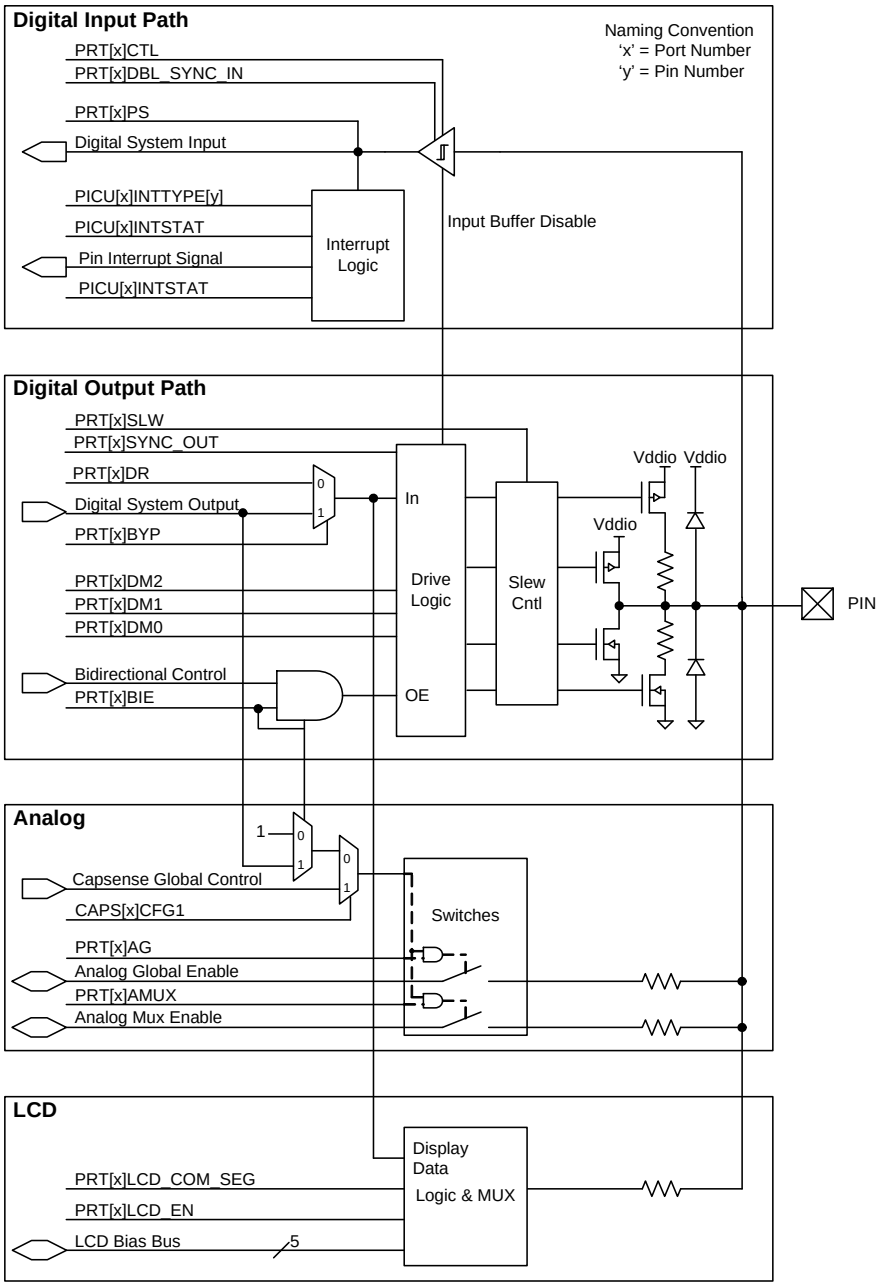


6.2.1.1 Active Mode

Active mode is the primary operating mode of the device. When in active mode, the active configuration template bits control which available resources are enabled or disabled. When a resource is disabled, the digital clocks are gated, analog bias currents are disabled, and leakage currents are reduced as appropriate. User firmware can dynamically control subsystem power by setting and clearing bits in the active configuration template. The CPU can disable itself, in which case the CPU is automatically reenabled at the next wakeup event.

When a wakeup event occurs, the global mode is always returned to active, and the CPU is automatically enabled, regardless of its template settings. Active mode is the default global power mode upon boot.

Figure 6-8. GPIO Block Diagram



- Resistive Pull Up or Resistive Pull Down

  Resistive pull up or pull down, respectively, provides a series resistance in one of the data states and strong drive in the other. Pins can be used for digital input and output in these modes. Interfacing to mechanical switches is a common application for these modes.

- Open Drain, Drives High and Open Drain, Drives Low

  Open drain modes provide high impedance in one of the data states and strong drive in the other. Pins can be used for digital input and output in these modes. A common application for these modes is driving the I^2C bus signal lines.

- Strong Drive

  Provides a strong CMOS output drive in either high or low state. This is the standard output mode for pins. Strong Drive mode pins must not be used as inputs under normal circumstances. This mode is often used to drive digital output signals or external FETs.

- Resistive Pull Up and Pull Down

  Similar to the resistive pull up and resistive pull down modes except the pin is always in series with a resistor. The high data state is pull up while the low data state is pull down. This mode is most often used when other signals that may cause shorts can drive the bus.

6.4.2 Pin Registers

Registers to configure and interact with pins come in two forms that may be used interchangeably.

All I/O registers are available in the standard port form, where each bit of the register corresponds to one of the port pins. This register form is efficient for quickly reconfiguring multiple port pins at the same time.

I/O registers are also available in pin form, which combines the eight most commonly used port register bits into a single register for each pin. This enables very fast configuration changes to individual pins with a single register write.

6.4.3 Bidirectional Mode

High speed bidirectional capability allows pins to provide both the high impedance digital drive mode for input signals and a second user selected drive mode such as strong drive (set using PRTxDM[2:0] registers) for output signals on the same pin, based on the state of an auxiliary control bus signal. The bidirectional capability is useful for processor busses and communications interfaces such as the SPI Slave MISO pin that requires dynamic hardware control of the output buffer.

The auxiliary control bus routes up to 16 UDB or digital peripheral generated output enable signals to one or more pins.

6.4.4 Slew Rate Limited Mode

GPIO and SIO pins have fast and slow output slew rate options for strong and open drain drive modes, not resistive drive modes. Because it results in reduced EMI, the slow edge rate option is recommended for signals that are not speed critical, generally less than 1 MHz. The fast slew rate is for signals between 1 MHz and 33 MHz. The slew rate is individually configurable for each pin, and is set by the PRTxSLW registers.

6.4.5 Pin Interrupts

All GPIO and SIO pins are able to generate interrupts to the system. All eight pins in each port interface to their own Port Interrupt Control Unit (PICU) and associated interrupt vector. Each pin of the port is independently configurable to detect rising edge, falling edge, both edge interrupts, or to not generate an interrupt.

Depending on the configured mode for each pin, each time an interrupt event occurs on a pin, its corresponding status bit of the interrupt status register is set to “1” and an interrupt request is sent to the interrupt controller. Each PICU has its own interrupt vector in the interrupt controller and the pin status register providing easy determination of the interrupt source down to the pin level.

Port pin interrupts remain active in all sleep modes allowing the PSoC device to wake from an externally generated interrupt.

While level sensitive interrupts are not directly supported; Universal Digital Blocks (UDB) provide this functionality to the system when needed.

6.4.6 Input Buffer Mode

GPIO and SIO input buffers can be configured at the port level for the default CMOS input thresholds or the optional LVTTL input thresholds. All input buffers incorporate Schmitt triggers for input hysteresis. Additionally, individual pin input buffers can be disabled in any drive mode.

6.4.7 I/O Power Supplies

Up to four I/O pin power supplies are provided depending on the device and package. Each I/O supply must be less than or equal to the voltage on the chip’s analog (Vdda) pin. This feature allows users to provide different I/O voltage levels for different pins on the device. Refer to the specific device package pinout to determine Vddio capability for a given port and pin.

The SIO port pins support an additional regulated high output capability, as described in Adjustable Output Level.

6.4.8 Analog Connections

These connections apply only to GPIO pins. All GPIO pins may be used as analog inputs or outputs. The analog voltage present on the pin must not exceed the Vddio supply voltage to which the GPIO belongs. Each GPIO may connect to one of the analog global busses or to one of the analog mux buses to connect any pin to any internal analog resource such as ADC or comparators. In addition, select pins provide direct connections to specific analog features such as the high current DACs or uncommitted opamps.

6.4.9 CapSense

This section applies only to GPIO pins. All GPIO pins may be used to create CapSense buttons and sliders[4]. See the “CapSense” section on page 56 for more information.

6.4.10 LCD Segment Drive

This section applies only to GPIO pins. All GPIO pins may be used to generate Segment and Common drive signals for direct glass drive of LCD glass. See the “LCD Direct Drive” section on page 55 for details.

8.1 Analog Routing

The CY8C34 family of devices has a flexible analog routing architecture that provides the capability to connect GPIOs and different analog blocks, and also route signals between different analog blocks. One of the strong points of this flexible routing architecture is that it allows dynamic routing of input and output connections to the different analog blocks.

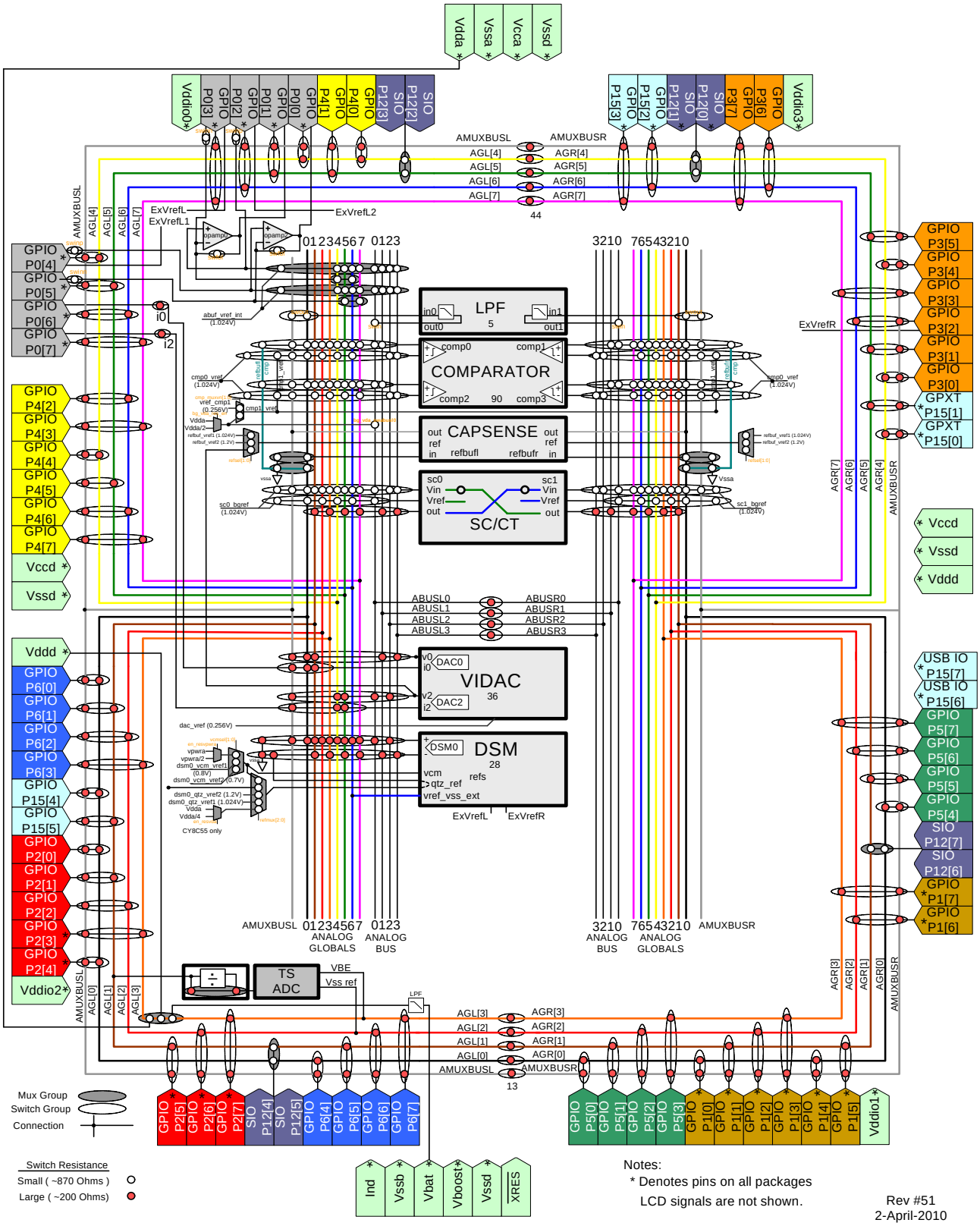
8.1.1 Features

- Flexible, configurable analog routing architecture
- 16 Analog globals (AG) and two analog mux buses (AMUXBUS) to connect GPIOs and the analog blocks
- Each GPIO is connected to one analog global and one analog mux bus
- 8 Analog local buses (abus) to route signals between the different analog blocks
- Multiplexers and switches for input and output selection of the analog blocks

8.1.2 Functional Description

Analog globals (AGs) and analog mux buses (AMUXBUS) provide analog connectivity between GPIOs and the various analog blocks. There are 16 AGs in the CY8C34 family. The analog routing architecture is divided into four quadrants as shown in Figure 8-2. Each quadrant has four analog globals (AGL[0..3], AGL[4..7], AGR[0..3], AGR[4..7]). Each GPIO is connected to the corresponding AG through an analog switch. The analog mux bus is a shared routing resource that connects to every GPIO through an analog switch. There are two AMUXBUS routes in CY8C34, one in the left half (AMUXBUSL) and one in the right half (AMUXBUSR), as shown in Figure 8-2.

Figure 8-2. CY8C34 Analog Interconnect



8.3 Comparators

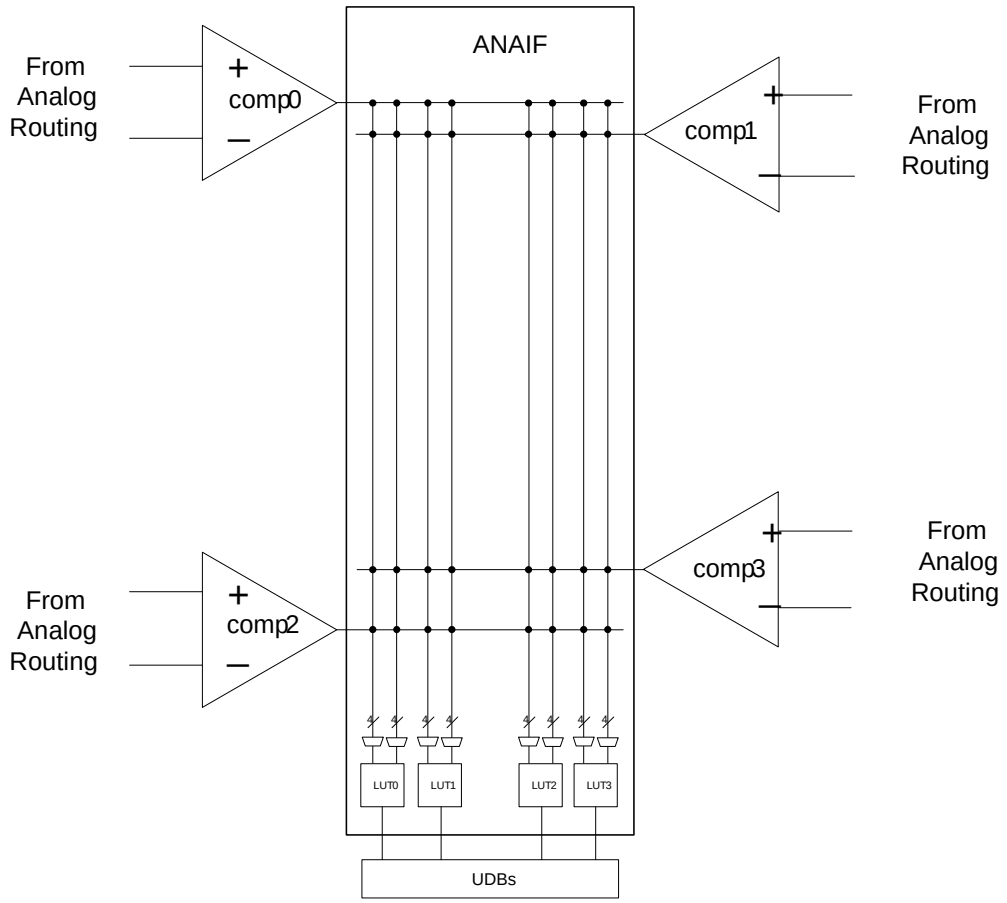
The CY8C34 family of devices contains four comparators in a device. Comparators have these features:

- Input offset factory trimmed to less than 5 mV
- Rail-to-rail common mode input range (Vssa to Vdda)
- Speed and power can be traded off by using one of three modes: fast, slow, or ultra low power
- Comparator outputs can be routed to look up tables to perform simple logic functions and then can also be routed to digital blocks
- The positive input of the comparators may be optionally passed through a low pass filter. Two filters are provided
- Comparator inputs can be connections to GPIO, DAC outputs and SC block outputs

8.3.1 Input and Output Interface

The positive and negative inputs to the comparators come from the analog global buses, the analog mux line, the analog local bus and precision reference through multiplexers. The output from each comparator could be routed to any of the two input LUTs. The output of that LUT is routed to the UDB Digital System Interface.

Figure 8-4. Analog Comparator



8.3.2 LUT

The CY8C34 family of devices contains four LUTs. The LUT is a two input, one output lookup table that is driven by any one or two of the comparators in the chip. The output of any LUT is routed to the digital system interface of the UDB array. From the digital system interface of the UDB array, these signals can be connected to UDBs, DMA controller, I/O, or the interrupt controller.

The LUT control word written to a register sets the logic function on the output. The available LUT functions and the associated control word is shown in Table 8-1.

The TIA configuration is used for applications where an external sensor's output is current as a function of some type of stimulus such as temperature, light, magnetic flux etc. In a common application, the voltage DAC output can be connected to the VREF TIA input to allow calibration of the external sensor bias current by adjusting the voltage DAC output voltage.

8.6 LCD Direct Drive

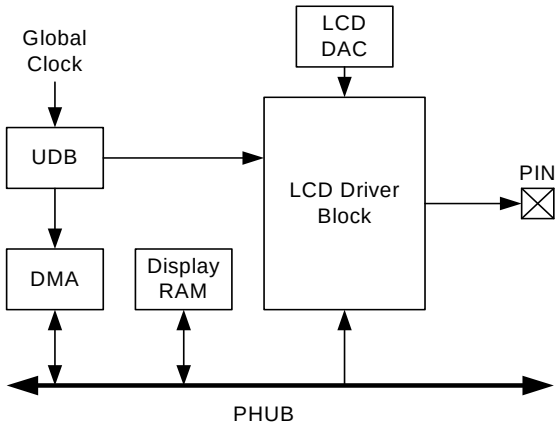
The PSoC Liquid Crystal Display (LCD) driver system is a highly configurable peripheral designed to allow PSoC to directly drive a broad range of LCD glass. All voltages are generated on chip, eliminating the need for external components. With a high multiplex ratio of up to 1/16, the CY8C34 family LCD driver system can drive a maximum of 736 segments. The PSoC LCD driver module was also designed with the conservative power budget of portable devices in mind, enabling different LCD drive modes and power down modes to conserve power.

PSoC Creator provides an LCD segment drive component. The component wizard provides easy and flexible configuration of LCD resources. You can specify pins for segments and commons along with other options. The software configures the device to meet the required specifications. This is possible because of the programmability inherent to PSoC devices.

Key features of the PSoC LCD segment system are:

- LCD panel direct driving
- Type A (standard) and Type B (low power) waveform support
- Wide operating voltage range support (2V to 5V) for LCD panels
- Static, 1/2, 1/3, 1/4, 1/5 bias voltage levels
- Internal bias voltage generation through internal resistor ladder
- Up to 62 total common and segment outputs
- Up to 1/16 multiplex for a maximum of 16 backplane/common outputs
- Up to 62 front plane/segment outputs for direct drive
- Drives up to 736 total segments (16 backplane x 46 front plane)
- Up to 64 levels of software controlled contrast
- Ability to move display data from memory buffer to LCD driver through DMA (without CPU intervention)
- Adjustable LCD refresh rate from 10 Hz to 150 Hz
- Ability to invert LCD display for negative image
- Three LCD driver drive modes, allowing power optimization

Figure 8-9. LCD System



8.6.1 LCD Segment Pin Driver

Each GPIO pin contains an LCD driver circuit. The LCD driver buffers the appropriate output of the LCD DAC to directly drive the glass of the LCD. A register setting determines whether the pin is a common or segment. The pin's LCD driver then selects one of the six bias voltages to drive the I/O pin, as appropriate for the display data.

8.6.2 Display Data Flow

The LCD segment driver system reads display data and generates the proper output voltages to the LCD glass to produce the desired image. Display data resides in a memory buffer in the system SRAM. Each time you need to change the common and segment driver voltages, the next set of pixel data moves from the memory buffer into the Port Data Registers via DMA.

8.6.3 UDB and LCD Segment Control

A UDB is configured to generate the global LCD control signals and clocking. This set of signals is routed to each LCD pin driver through a set of dedicated LCD global routing channels. In addition to generating the global LCD control signals, the UDB also produces a DMA request to initiate the transfer of the next frame of LCD data.

8.6.4 LCD DAC

The LCD DAC generates the contrast control and bias voltage for the LCD system. The LCD DAC produces up to five LCD drive voltages plus ground, based on the selected bias ratio. The bias voltages are driven out to GPIO pins on a dedicated LCD bias bus, as required.

11.2 Device Level Specifications

Specifications are valid for -40°C ≤ T_A ≤ 85°C and T_J ≤ 100°C, except where noted. Specifications are valid for 1.71V to 5.5V, except where noted.

11.2.1 Device Level Specifications

Table 11-2. DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{DDA}	Analog supply voltage and input to analog core regulator	Analog core regulator enabled	1.8		5.5	V
V_{DDA}	Analog supply voltage, analog regulator bypassed	Analog core regulator disabled	1.71	1.8	1.89	V
V_{DDD}	Digital supply voltage relative to Vssd	Digital core regulator enabled	1.8		V_{DDA}	V
V_{DDD}	Digital supply voltage, digital regulator bypassed	Digital core regulator disabled	1.71	1.8	1.89	V
Vddio[5]	I/O supply voltage relative to Vssio		1.71		V_{DDA}	V
Vcca	Direct analog core voltage input (Analog regulator bypass)	Analog core regulator disabled	1.71	1.8	1.89	V
Vccd	Direct digital core voltage input (Digital regulator bypass)	Digital core regulator disabled	1.71	1.8	1.89	V
Vbat	Voltage supplied to boost converter		0.5		5.5	V
	Active Mode, V_{DD} = 1.71V - 5.5V					
Idd[6]	Execute from CPU instruction buffer. See "Flash Program Memory" on page 18.					
	CPU at 3 MHz	T= -40°C				mA
		T= 25°C		0.8		mA
		T= 85°C				mA
	CPU at 6 MHz	T= -40°C				mA
		T= 25°C		1.2		mA
		T= 85°C				mA
	CPU at 12 MHz	T= -40°C				mA
		T= 25°C		2.0		mA
		T= 85°C				mA
	CPU at 24 MHz	T= -40°C				mA
		T= 25°C		3.5		mA
		T= 85°C				mA
	CPU at 50 MHz	T= -40°C				mA
		T= 25°C		6.6		mA
		T= 85°C				mA

11.3 Power Regulators

Specifications are valid for -40°C ≤ T_A ≤ 85°C and T_J ≤ 100°C, except where noted. Specifications are valid for 1.71V to 5.5V, except where noted.

11.3.1 Digital Core Regulator

Table 11-4. Digital Core Regulator DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{DDD}	Input voltage		1.8	-	5.5	V
Vccd	Output voltage		-	1.80	-	V
	Regulator output capacitor	±10%, X5R ceramic or better. The two Vccd pins must be shorted together, with as short a trace as possible, see Power System on page 25	-	1	-	µF

11.3.2 Analog Core Regulator

Table 11-5. Analog Core Regulator DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{DDA}	Input voltage		1.8	-	5.5	V
Vcca	Output voltage		-	1.80	-	V
	Regulator output capacitor	±10%, X5R ceramic or better	-	1	-	µF

11.3.3 Inductive Boost Regulator

Table 11-6. Inductive Boost Regulator DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Vbat	Input voltage	Includes startup	0.5	-	5.5	V
Iboost	Load current[10, 11]	Vin=1.6-5.5V, Vout=1.6-5.5V, external diode	-	-	50	mA
		Vin=1.6-3.6V, Vout=1.6-3.6V, internal diode	-	-	75	mA
		Vin=0.8-1.6V, Vout=1.6-3.6V, internal diode	-	-	30	mA
		Vin=0.8-1.6V, Vout=3.6-5.5V, external diode	-	-	20	mA
		Vin=0.5-0.8V, Vout=1.6-3.6V, internal diode	-	-	15	mA
Lboost	Boost inductor	10 µH spec'd	4.7	10	47	µH
Cboost	Filter capacitor[9]	22 µF || 0.1 µF spec'd	10	22	47	µF
If	External Schottky diode average forward current	External Schottky diode is required for Vboost > 3.6V	1	-	-	A
Vr	External Schottky diode peak reverse voltage	External Schottky diode is required for Vboost > 3.6V	20	-	-	V
Ilpk	Inductor peak current		-	-	700	mA
	Quiescent current	Boost active mode	-	200	-	µA
		Boost standby mode, 32 khz external crystal oscillator, Iboost ≤ 1 µA	-	12	-	µA

Notes
10. For output voltages above 3.6V, an external diode is required.
11. Maximum output current applies for output voltages ≤ 4x input voltage.

11.6 Digital Peripherals

Specifications are valid for -40°C ≤ T_A ≤ 85°C and T_J ≤ 100°C, except where noted. Specifications are valid for 1.71V to 5.5V, except where noted.

11.6.1 Timer

Table 11-42. Timer DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Block current consumption	16-bit timer, at listed input clock frequency	-	-	-	µA
	3 MHz		-	8	-	µA
	12 MHz		-	30	-	µA
	50 MHz		-	120	-	µA

Table 11-43. Timer AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Operating frequency		DC	-	50	MHz
	Capture pulse width (Internal)		21	-	-	ns
	Capture pulse width (external)		42	-	-	ns
	Timer resolution		21	-	-	ns
	Enable pulse width		21	-	-	ns
	Enable pulse width (external)		42	-	-	ns
	Reset pulse width		21	-	-	ns
	Reset pulse width (external)		42	-	-	ns

11.6.2 Counter

Table 11-44. Counter DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Block current consumption	16-bit counter, at listed input clock frequency	-	-	-	µA
	3 MHz		-	8	-	µA
	12 MHz		-	30	-	µA
	50 MHz		-	120	-	µA

Table 11-45. Counter AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Operating frequency		DC	-	50	MHz
	Capture pulse		21	-	-	ns
	Resolution		21	-	-	ns
	Pulse width		21	-	-	ns
	Pulse width (external)		42			ns
	Enable pulse width		21	-	-	ns
	Enable pulse width (external)		42	-	-	ns
	Reset pulse width		21	-	-	ns
	Reset pulse width (external)		42	-	-	ns

11.9.3 Internal Low Speed Oscillator

Table 11-79. ILO DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Icc	Operating current	Fout = 1 kHz	-	0.3	1.7	µA
		Fout = 33 kHz	-	1.0	2.6	µA
		Fout = 100 kHz	-	1.0	2.6	µA
	Leakage current	Power down mode	-	2.0	15	nA

Table 11-80. ILO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Startup time	Turbo mode	-	-	2	ms
	Startup time	Non-turbo mode, pd_mode = 0	-	-	2	ms
	Startup time	Non-turbo mode, pd_mode = 1	-	-	15	ms
	Duty cycle		47	50	53	%
Filo	ILO frequencies (trimmed)					
	100 kHz		45	100	200	kHz
	1 kHz		0.5	1	2	kHz
	ILO frequencies (untrimmed)					
	100 kHz		30	100	300	kHz
	1 kHz		0.3	1	3.5	kHz

11.9.4 External Crystal Oscillator

Table 11-81. ECO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F	Crystal frequency range		4	-	33	MHz
DC	Duty cycle[9]		40	50	60	%

11.9.5 External Clock Reference

Table 11-82. External Clock Reference AC Specifications[9]

Parameter	Description	Conditions	Min	Typ	Max	Units
	External frequency range		0	-	33	MHz
	Input duty cycle range	Measured at Vddio/2	30	50	70	%
	Input edge rate	Vil to Vih	0.1	-	-	V/ns

Figure 13-1. 48-Pin (300 mil) SSOP Package Outline

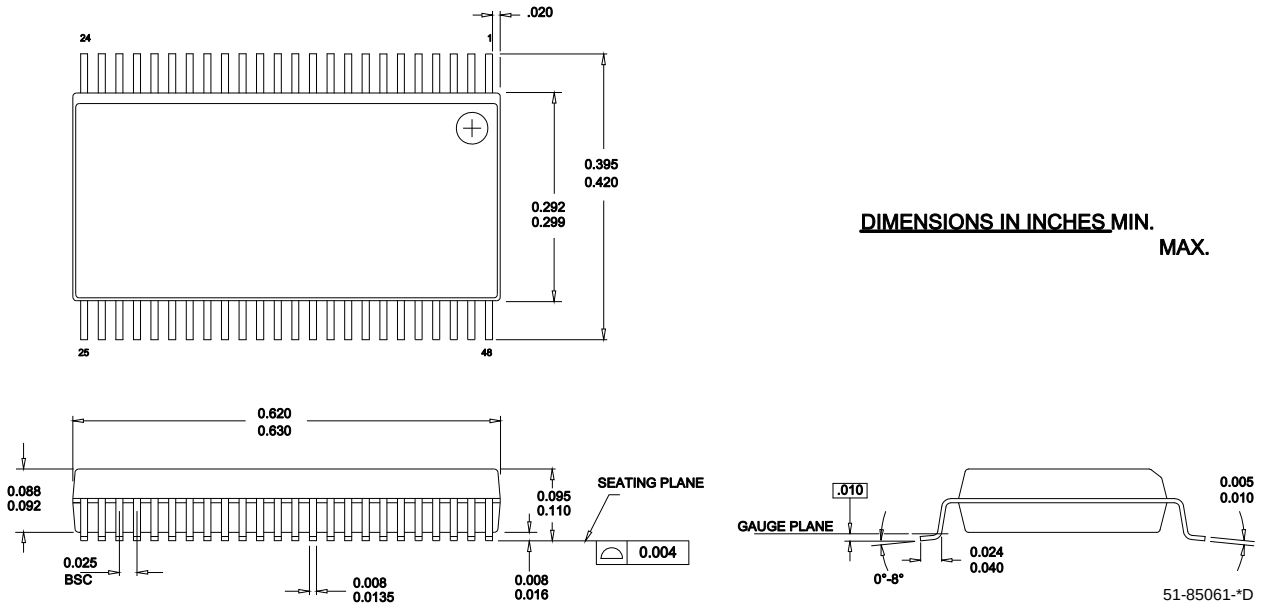
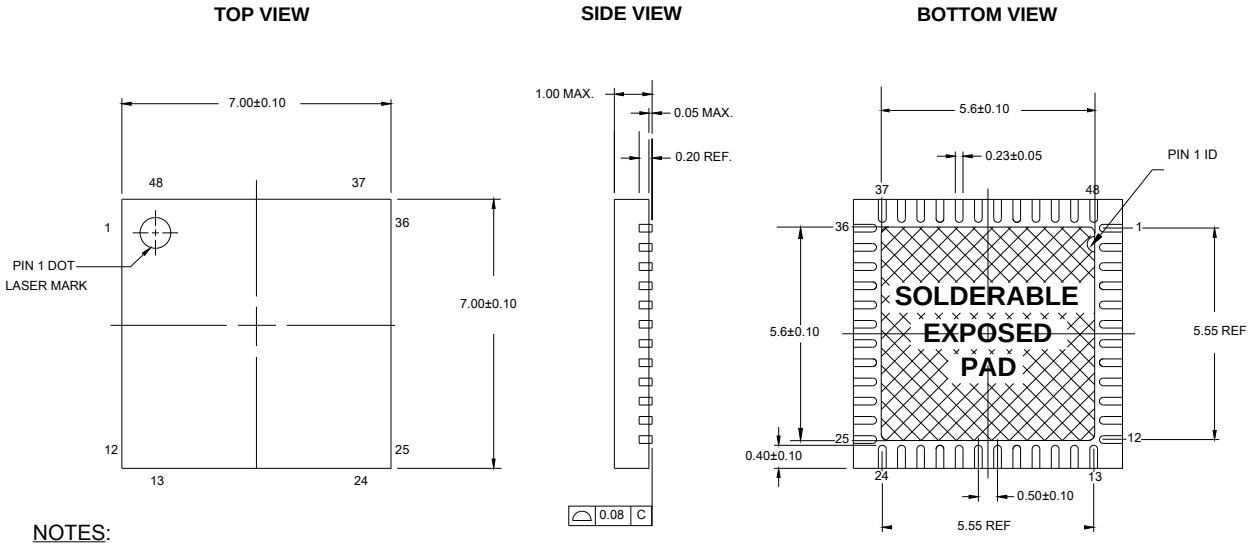


Figure 13-2. 48-Pin QFN Package Outline



NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 0.13g
4. ALL DIMENSIONS ARE IN MM [MIN/MAX]
5. PACKAGE CODE

PART #	DESCRIPTION
LT48D	LEAD FREE

001- 45616 *B

Description Title: PSoC® 3: CY8C34 Family Data Sheet Programmable System-on-Chip (PSoC®) Document Number: 001-53304				
*D	2903576	04/01/10	MKEA	Updated Vb pin in PCB Schematic Updated Tstartup parameter in AC Specifications table Added Load regulation and Line regulation parameters to Inductive Boost Regulator DC Specifications table Updated Icc parameter in LCD Direct Drive DC Specs table In page 1, updated internal oscillator range under Precision programmable clocking to start from 3 MHz Updated Iout parameter in LCD Direct Drive DC Specs table Updated Table 6-2 and Table 6-3 Removed DFB block in Figure 1-1. Added bullets on CapSense in page 1; added CapSense column in Section 12 Removed some references to footnote [1] Changed INC_Rn cycles from 3 to 2 (Table 4-1) Added footnote in PLL AC Specification table Added PLL intermediate frequency row with footnote in PLL AC Specs table Added UDBs subsection under 11.6 Digital Peripherals Updated Figure 2-6 (PCB Layout) Updated Pin Descriptions section and modified Figures 6-6, 6-8, 6-9 Updated LVD in Tables 6-2 and 6-3; modified Low power modes bullet in page 1 Added note to Figures 2-5 and 6-2; Updated Figure 6-2 to add capacitors for V_{DDA} and V_{DDD} pins. Updated boost converter section (6.2.2) Updated Tstartup values in Table 11-3. Removed IPOR rows from Table 11-67. Updated 6.3.1.1, Power Voltage Level Monitors. Updated section 5.2 and Table 11-2 to correct suggestion of execution from flash. Updated IMO max frequency in Figure 6-1, Table 11-77, and Table 11-78. Updated Vref specs in Table 11-21. Updated IDAC uncompensated gain error in Table 11-25. Updated Delay from Interrupt signal input to ISR code execution from ISR code in Table 11-57. Removed other line in table. Added sentence to last paragraph of section 6.1.1.3. Updated Tresp, high and low power modes, in Table 11-24. Updated f_TCK values in Table 11-72 and f_SWDCK values in Table 11-73. Updated SNR condition in Table 11-20. Updated sleep wakeup time in Table 6-3 and Tsleep in Table 11-3. Added 1.71V <= V_{DDD} < 3.3V, SWD over USBIO pins value to Table 11-73. Removed mention of hibernate reset (HRES) from page 1 features, Table 6-3, Section 6.2.1.4, Section 6.3, and Section 6.3.1.1. Change PPOR/PRES to TBDs in Section 6.3.1.1, Section 6.4.1.6 (changed PPOR to reset), Table 11-3 (changed PPOR to PRES), Table 11-67 (changed title, values TBD), and Table 11-68 (changed PPOR_TR to PRES_TR). Added sentence saying that LVD circuits can generate a reset to Section 6.3.1.1. Changed Idd values on page 1, page 5, and Table 11-2. Changed resume time value in Section 6.2.1.3. Changed ESD HBM value in Table 11-1. Changed sample rate row in Table 11-20. Removed V_{DDA} = 1.65V rows and changed BWag value in Table 11-22. Changed Vioff values and changed CMRR value in Table 11-23. Changed INL max value in Table 11-27. Added max value to the Quiescent current specs in Tables 11-29 and 11-31. Changed occurrences of “Block” to “Row” and deleted the “ECC not included” footnote in Table 11-55. Changed max response time value in Tables 11-68 and 11-70. Changed the Startup time in Table 11-78. Added condition to intermediate frequency row in Table 11-84. Added row to Table 11-68. Added brown out note to Section 11.8.1.