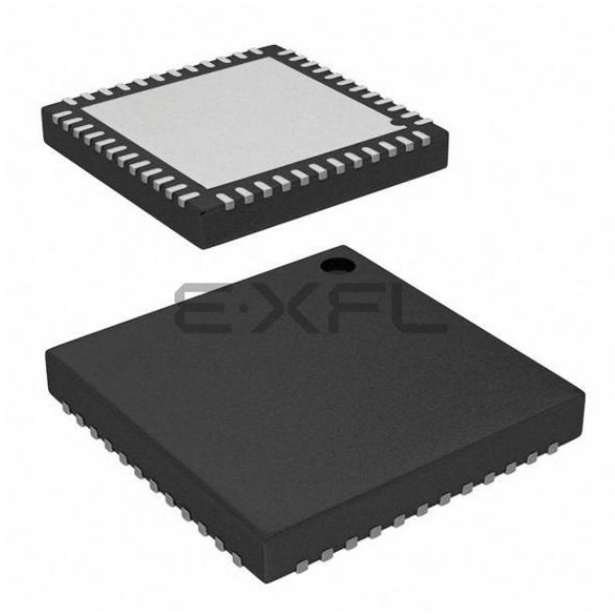

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	EBI/EMI, I²C, LINbus, SPI, UART/USART, USB
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3445lti-089

Figure 1-1 illustrates the major components of the CY8C34 family. They are:

- 8051 CPU Subsystem
- Nonvolatile Subsystem
- Programming, Debug, and Test Subsystem
- Inputs and Outputs
- Clocking
- Power
- Digital Subsystem
- Analog Subsystem

PSoC's digital subsystem provides half of its unique configurability. It connects a digital signal from any peripheral to any pin through the Digital System Interconnect (DSI). It also provides functional flexibility through an array of small, fast, low power Universal Digital Blocks (UDBs). PSoC Creator provides a library of pre-built and tested standard digital peripherals (UART, SPI, LIN, PRS, CRC, timer, counter, PWM, AND, OR, and so on) that are mapped to the UDB array. The designer can also easily create a digital circuit using boolean primitives by means of graphical design entry. Each UDB contains Programmable Array Logic (PAL)/Programmable Logic Device (PLD) functionality, together with a small state machine engine to support a wide variety of peripherals.

In addition to the flexibility of the UDB array, PSoC also provides configurable digital blocks targeted at specific functions. For the CY8C34 family these blocks can include four 16-bit timer, counter, and PWM blocks; I^2C slave, master, and multi-master; Full-Speed USB; and Full CAN 2.0b.

For more details on the peripherals see the "Example Peripherals" section on page 35 of this data sheet. For information on UDBs, DSI, and other digital blocks, see the "Digital Subsystem" section on page 35 of this data sheet.

PSoC's analog subsystem is the second half of its unique configurability. All analog performance is based on a highly accurate absolute voltage reference with less than 0.9% error over temperature and voltage. The configurable analog subsystem includes:

- Analog muxes
- Comparators
- Voltage references
- Analog-to-Digital Converter (ADC)
- Digital-to-Analog Converters (DACs)

All GPIO pins can route analog signals into and out of the device using the internal analog bus. This allows the device to interface up to 62 discrete analog signals. The heart of the analog subsystem is a fast, accurate, configurable Delta-Sigma ADC with these features:

- Less than 100 µV offset
- A gain error of 0.2%
- Integral Non Linearity (INL) less than 1 LSB
- Differential Non Linearity (DNL) less than 1 LSB
- Signal-to-noise ratio (SNR) better than 70 dB (Delta-Sigma) in 12-bit mode

This converter addresses a wide variety of precision analog applications including some of the most demanding sensors.

Two high speed voltage or current DACs support 8-bit output signals at update rate of 8 Msps in current DAC (IDAC) and 1 Msps in voltage DAC (VDAC). They can be routed out of any GPIO pin. You can create higher resolution voltage PWM DAC outputs using the UDB array. This can be used to create a pulse width modulated (PWM) DAC of up to 10 bits, at up to 48 kHz. The digital DACs in each UDB support PWM, PRS, or delta-sigma algorithms with programmable widths.

In addition to the ADC and DACs, the analog subsystem provides multiple:

- Uncommitted opamps
- Configurable Switched Capacitor/Continuous Time (SC/CT) blocks. These support:
  - Transimpedance amplifiers
  - Programmable gain amplifiers
  - Mixers
  - Other similar analog components

See the "Analog Subsystem" section on page 48 of this data sheet for more details.

PSoC's 8051 CPU subsystem is built around a single cycle pipelined 8051 8-bit processor running at up to 50 MHz. The CPU subsystem includes a programmable nested vector interrupt controller, DMA controller, and RAM. PSoC's nested vector interrupt controller provides low latency by allowing the CPU to vector directly to the first address of the interrupt service routine, bypassing the jump instruction required by other architectures. The DMA controller enables peripherals to exchange data without CPU involvement. This allows the CPU to run slower (saving power) or use those CPU cycles to improve the performance of firmware algorithms. The single cycle 8051 CPU runs ten times faster than a standard 8051 processor. The processor speed itself is configurable allowing active power consumption to be tuned for specific applications.

4.3.1.5 Program Branching Instructions

The 8051 supports a set of conditional and unconditional jump instructions that help to modify the program execution flow. Table 4-5 shows the list of jump instructions.

Table 4-5. Jump Instructions

Mnemonic	Description	Bytes	Cycles
ACALL addr11	Absolute subroutine call	2	4
LCALL addr16	Long subroutine call	3	4
RET	Return from subroutine	1	4
RETI	Return from interrupt	1	4
AJMP addr11	Absolute jump	2	3
LJMP addr16	Long jump	3	4
SJMP rel	Short jump (relative address)	2	3
JMP @A + DPTR	Jump indirect relative to DPTR	1	5
JZ rel	Jump if accumulator is zero	2	4
JNZ rel	Jump if accumulator is nonzero	2	4
CJNE A,Direct, rel	Compare direct byte to accumulator and jump if not equal	3	5
CJNE A, #data, rel	Compare immediate data to accumulator and jump if not equal	3	4
CJNE Rn, #data, rel	Compare immediate data to register and jump if not equal	3	4
CJNE @Ri, #data, rel	Compare immediate data to indirect RAM and jump if not equal	3	5
DJNZ Rn,rel	Decrement register and jump if not zero	2	4
DJNZ Direct, rel	Decrement direct byte and jump if not zero	3	5
NOP	No operation	1	1

4.4 DMA and PHUB

The PHUB and the DMA controller are responsible for data transfer between the CPU and peripherals, and also data transfers between peripherals. The PHUB and DMA also control device configuration during boot. The PHUB consists of:

- A central hub that includes the DMA controller, arbiter, and router
- Multiple spokes that radiate outward from the hub to most peripherals

There are two PHUB masters: the CPU and the DMA controller. Both masters may initiate transactions on the bus. The DMA channels can handle peripheral communication without CPU intervention. The arbiter in the central hub determines which DMA channel is the highest priority if there are multiple requests.

4.4.1 PHUB Features

- CPU and DMA controller are both bus masters to the PHUB
- Eight Multi-layer AHB Bus parallel access paths (spokes) for peripheral access
- Simultaneous CPU and DMA access to peripherals located on different spokes
- Simultaneous DMA source and destination burst transactions on different spokes
- Supports 8, 16, 24, and 32-bit addressing and data

Table 4-6. PHUB Spokes and Peripherals

PHUB Spokes	Peripherals
0	SRAM
1	IOs, PICU, EMIF
2	PHUB local configuration, Power manager, Clocks, IC, SWV, EEPROM, Flash programming interface
3	Analog interface and trim, Decimator
4	USB, CAN, I^2C, Timers, Counters, and PWMs
5	Reserved
6	UDBs group 1
7	UDBs group 2

4.4.2 DMA Features

- 24 DMA channels
- Each channel has one or more Transaction Descriptors (TDs) to configure channel behavior. Up to 128 total TDs can be defined
- TDs can be dynamically updated
- Eight levels of priority per channel
- Any digitally routable signal, the CPU, or another DMA channel, can trigger a transaction
- Each channel can generate up to two interrupts per transfer
- Transactions can be stalled or canceled
- Supports transaction size of infinite or 1 to 64k bytes
- TDs may be nested and/or chained for complex transactions

4.4.3 Priority Levels

The CPU always has higher priority than the DMA controller when their accesses require the same bus resources. Due to the system architecture, the CPU can never starve the DMA. DMA channels of higher priority (lower priority number) may interrupt current DMA transfers. In the case of an interrupt, the current transfer is allowed to complete its current transaction. To ensure latency limits when multiple DMA accesses are requested simultaneously, a fairness algorithm guarantees an interleaved minimum percentage of bus bandwidth for priority levels 2 through 7. Priority levels 0 and 1 do not take part in the fairness algorithm and may use 100% of the bus bandwidth. If a tie occurs on two DMA requests of the same priority level, a simple round robin method is used to evenly share the allocated bandwidth. The round robin allocation can be disabled for each DMA channel, allowing it to always be at the head of the line. Priority levels 2 to 7 are guaranteed the minimum bus bandwidth shown in Table 4-7 after the CPU and DMA priority levels 0 and 1 have satisfied their requirements.

Table 4-7. Priority Levels

Priority Level	% Bus Bandwidth
0	100.0
1	100.0
2	50.0
3	25.0
4	12.5
5	6.2
6	3.1
7	1.5

When the fairness algorithm is disabled, DMA access is granted based solely on the priority level; no bus bandwidth guarantees are made.

4.4.4 Transaction Modes Supported

The flexible configuration of each DMA channel and the ability to chain multiple channels allow the creation of both simple and complex use cases. General use cases include, but are not limited to:

4.4.4.1 Simple DMA

In a simple DMA case, a single TD transfers data between a source and sink (peripherals or memory location).

4.4.4.2 Auto Repeat DMA

Auto repeat DMA is typically used when a static pattern is repetitively read from system memory and written to a peripheral. This is done with a single TD that chains to itself.

4.4.4.3 Ping Pong DMA

A ping pong DMA case uses double buffering to allow one buffer to be filled by one client while another client is consuming the data previously received in the other buffer. In its simplest form, this is done by chaining two TDs together so that each TD calls the opposite TD when complete.

4.4.4.4 Circular DMA

Circular DMA is similar to ping pong DMA except it contains more than two buffers. In this case there are multiple TDs; after the last TD is complete it chains back to the first TD.

4.4.4.5 Scatter Gather DMA

In the case of scatter gather DMA, there are multiple noncontiguous sources or destinations that are required to effectively carry out an overall DMA transaction. For example, a packet may need to be transmitted off of the device and the packet elements, including the header, payload, and trailer, exist in various noncontiguous locations in memory. Scatter gather DMA allows the segments to be concatenated together by using multiple TDs in a chain. The chain gathers the data from the multiple locations. A similar concept applies for the reception of data onto the device. Certain parts of the received data may need to be scattered to various locations in memory for software processing convenience. Each TD in the chain specifies the location for each discrete element in the chain.

4.4.4.6 Packet Queuing DMA

Packet queuing DMA is similar to scatter gather DMA but specifically refers to packet protocols. With these protocols, there may be separate configuration, data, and status phases associated with sending or receiving a packet.

For instance, to transmit a packet, a memory mapped configuration register can be written inside a peripheral, specifying the overall length of the ensuing data phase. The CPU can set up this configuration information anywhere in system memory and copy it with a simple TD to the peripheral. After the configuration phase, a data phase TD (or a series of data phase TDs) can begin (potentially using scatter gather). When the data phase TD(s) finish, a status phase TD can be invoked that reads some memory mapped status information from the peripheral and copies it to a location in system memory specified by the CPU for later inspection. Multiple sets of configuration, data, and status phase “subchains” can be strung together to create larger chains that transmit multiple packets in this way. A similar concept exists in the opposite direction to receive the packets.

- Resistive Pull Up or Resistive Pull Down

  Resistive pull up or pull down, respectively, provides a series resistance in one of the data states and strong drive in the other. Pins can be used for digital input and output in these modes. Interfacing to mechanical switches is a common application for these modes.

- Open Drain, Drives High and Open Drain, Drives Low

  Open drain modes provide high impedance in one of the data states and strong drive in the other. Pins can be used for digital input and output in these modes. A common application for these modes is driving the I^2C bus signal lines.

- Strong Drive

  Provides a strong CMOS output drive in either high or low state. This is the standard output mode for pins. Strong Drive mode pins must not be used as inputs under normal circumstances. This mode is often used to drive digital output signals or external FETs.

- Resistive Pull Up and Pull Down

  Similar to the resistive pull up and resistive pull down modes except the pin is always in series with a resistor. The high data state is pull up while the low data state is pull down. This mode is most often used when other signals that may cause shorts can drive the bus.

6.4.2 Pin Registers

Registers to configure and interact with pins come in two forms that may be used interchangeably.

All I/O registers are available in the standard port form, where each bit of the register corresponds to one of the port pins. This register form is efficient for quickly reconfiguring multiple port pins at the same time.

I/O registers are also available in pin form, which combines the eight most commonly used port register bits into a single register for each pin. This enables very fast configuration changes to individual pins with a single register write.

6.4.3 Bidirectional Mode

High speed bidirectional capability allows pins to provide both the high impedance digital drive mode for input signals and a second user selected drive mode such as strong drive (set using PRTxDM[2:0] registers) for output signals on the same pin, based on the state of an auxiliary control bus signal. The bidirectional capability is useful for processor busses and communications interfaces such as the SPI Slave MISO pin that requires dynamic hardware control of the output buffer.

The auxiliary control bus routes up to 16 UDB or digital peripheral generated output enable signals to one or more pins.

6.4.4 Slew Rate Limited Mode

GPIO and SIO pins have fast and slow output slew rate options for strong and open drain drive modes, not resistive drive modes. Because it results in reduced EMI, the slow edge rate option is recommended for signals that are not speed critical, generally less than 1 MHz. The fast slew rate is for signals between 1 MHz and 33 MHz. The slew rate is individually configurable for each pin, and is set by the PRTxSLW registers.

6.4.5 Pin Interrupts

All GPIO and SIO pins are able to generate interrupts to the system. All eight pins in each port interface to their own Port Interrupt Control Unit (PICU) and associated interrupt vector. Each pin of the port is independently configurable to detect rising edge, falling edge, both edge interrupts, or to not generate an interrupt.

Depending on the configured mode for each pin, each time an interrupt event occurs on a pin, its corresponding status bit of the interrupt status register is set to “1” and an interrupt request is sent to the interrupt controller. Each PICU has its own interrupt vector in the interrupt controller and the pin status register providing easy determination of the interrupt source down to the pin level.

Port pin interrupts remain active in all sleep modes allowing the PSoC device to wake from an externally generated interrupt.

While level sensitive interrupts are not directly supported; Universal Digital Blocks (UDB) provide this functionality to the system when needed.

6.4.6 Input Buffer Mode

GPIO and SIO input buffers can be configured at the port level for the default CMOS input thresholds or the optional LVTTL input thresholds. All input buffers incorporate Schmitt triggers for input hysteresis. Additionally, individual pin input buffers can be disabled in any drive mode.

6.4.7 I/O Power Supplies

Up to four I/O pin power supplies are provided depending on the device and package. Each I/O supply must be less than or equal to the voltage on the chip’s analog (Vdda) pin. This feature allows users to provide different I/O voltage levels for different pins on the device. Refer to the specific device package pinout to determine Vddio capability for a given port and pin.

The SIO port pins support an additional regulated high output capability, as described in Adjustable Output Level.

6.4.8 Analog Connections

These connections apply only to GPIO pins. All GPIO pins may be used as analog inputs or outputs. The analog voltage present on the pin must not exceed the Vddio supply voltage to which the GPIO belongs. Each GPIO may connect to one of the analog global busses or to one of the analog mux buses to connect any pin to any internal analog resource such as ADC or comparators. In addition, select pins provide direct connections to specific analog features such as the high current DACs or uncommitted opamps.

6.4.9 CapSense

This section applies only to GPIO pins. All GPIO pins may be used to create CapSense buttons and sliders[4]. See the “CapSense” section on page 56 for more information.

6.4.10 LCD Segment Drive

This section applies only to GPIO pins. All GPIO pins may be used to generate Segment and Common drive signals for direct glass drive of LCD glass. See the “LCD Direct Drive” section on page 55 for details.

7. Digital Subsystem

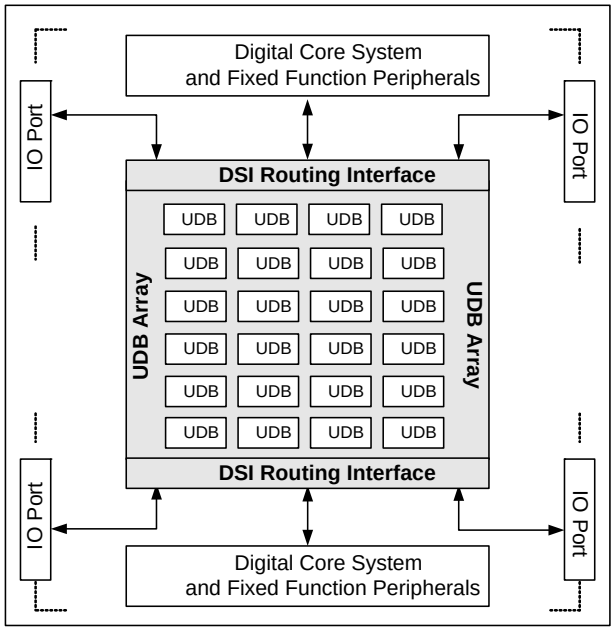
The digital programmable system creates application specific combinations of both standard and advanced digital peripherals and custom logic functions. These peripherals and logic are then interconnected to each other and to any pin on the device, providing a high level of design flexibility and IP security.

The features of the digital programmable system are outlined here to provide an overview of capabilities and architecture. Designers do not need to interact directly with the programmable digital system at the hardware and register level. PSoC Creator provides a high level schematic capture graphical interface to automatically place and route resources similar to PLDs.

The main components of the digital programmable system are:

- Universal Digital Blocks (UDB) - These form the core functionality of the digital programmable system. UDBs are a collection of uncommitted logic (PLD) and structural logic (Datapath) optimized to create all common embedded peripherals and customized functionality that are application or design specific.
- Universal Digital Block Array - UDB blocks are arrayed within a matrix of programmable interconnect. The UDB array structure is homogeneous and allows for flexible mapping of digital functions onto the array. The array supports extensive and flexible routing interconnects between UDBs and the Digital System Interconnect.
- Digital System Interconnect (DSI) - Digital signals from Universal Digital Blocks (UDBs), fixed function peripherals, I/O pins, interrupts, DMA, and other system core signals are attached to the Digital System Interconnect to implement full featured device connectivity. The DSI allows any digital function to any pin or other feature routability when used with the Universal Digital Block Array.

Figure 7-1. CY8C34 Digital Programmable Architecture



7.1 Example Peripherals

The flexibility of the CY8C34 family's Universal Digital Blocks (UDBs) and Analog Blocks allow the user to create a wide range of components (peripherals). The most common peripherals were built and characterized by Cypress and are shown in the PSoC Creator component catalog, however, users may also create their own custom components using PSoC Creator. Using PSoC Creator, users may also create their own components for reuse within their organization, for example sensor interfaces, proprietary algorithms, and display interfaces.

The number of components available through PSoC Creator is too numerous to list in the data sheet, and the list is always growing. An example of a component available for use in CY8C34 family, but, not explicitly called out in this data sheet is the UART component.

7.1.1 Example Digital Components

The following is a sample of the digital components available in PSoC Creator for the CY8C34 family. The exact amount of hardware resources (UDBs, routing, RAM, flash) used by a component varies with the features selected in PSoC Creator for the component.

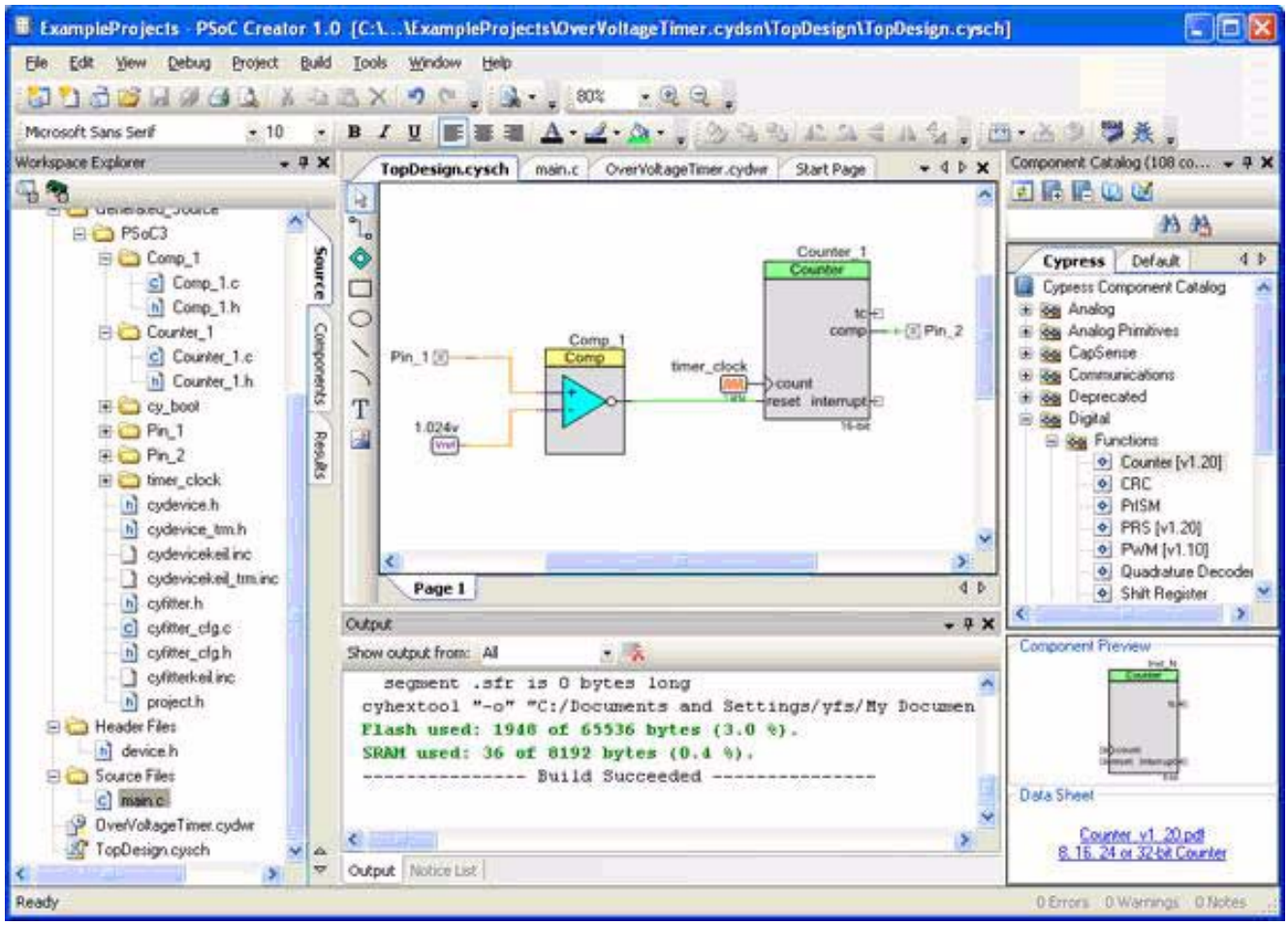
- Communications
  - I^2C
  - UART
  - SPI
- Functions
  - EMIF
  - PWMs
  - Timers
  - Counters
- Logic
  - NOT
  - OR
  - XOR
  - AND

7.1.2 Example Analog Components

The following is a sample of the analog components available in PSoC Creator for the CY8C34 family. The exact amount of hardware resources (SC/CT blocks, routing, RAM, flash) used by a component varies with the features selected in PSoC Creator for the component.

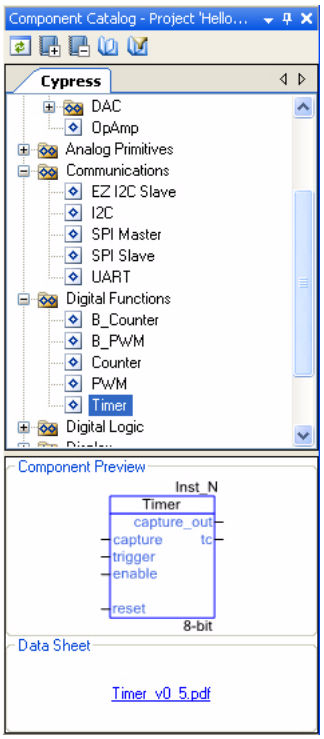
- Amplifiers
  - TIA
  - PGA
  - opamp
- ADC
  - Delta-Sigma
- DACs
  - Current
  - Voltage
  - PWM
- Comparators
- Mixers

Figure 7-2. PSoC Creator Framework



7.1.4.2 Component Catalog

Figure 7-3. Component Catalog



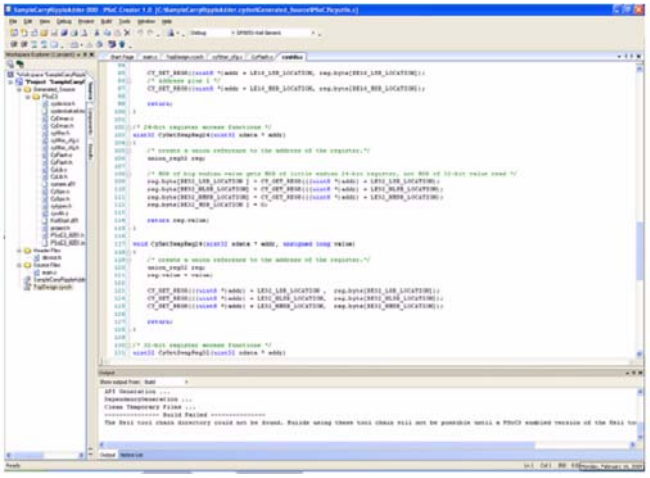
The component catalog is a repository of reusable design elements that select device functionality and customize your PSoC device. It is populated with an impressive selection of content; from simple primitives such as logic gates and device registers, through the digital timers, counters and PWMs, plus analog components such as ADC, DACs, and filters, and communication protocols, such as I^2C, USB, and CAN. See Example Peripherals on page 35 for more details about available peripherals. All content is fully characterized and carefully documented in datasheets with code examples, AC/DC specifications, and user code ready APIs.

7.1.4.3 Design Reuse

The symbol editor gives you the ability to develop reusable components that can significantly reduce future design time. Just draw a symbol and associate that symbol with your proven design. PSoC Creator allows for the placement of the new symbol anywhere in the component catalog along with the content provided by Cypress. You can then reuse your content as many times as you want, and in any number of projects, without ever having to revisit the details of the implementation.

7.1.4.4 Software Development

Figure 7-4. Code Editor

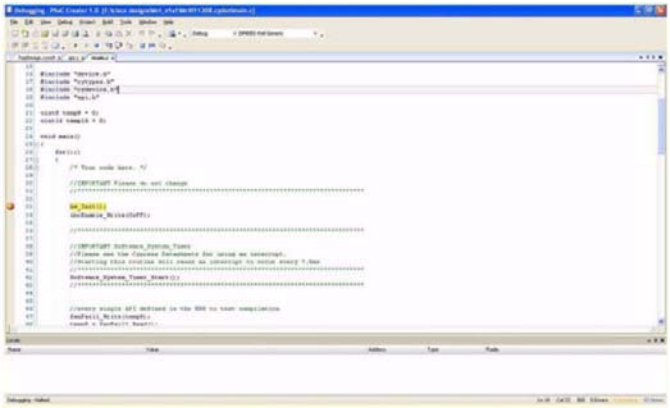


Anchoring the tool is a modern, highly customizable user interface. It includes project management and integrated editors for C and assembler source code, as well the design entry tools.

Project build control leverages compiler technology from top commercial vendors such as ARM® Limited, Keil™, and CodeSourcery (GNU). Free versions of Keil C51 and GNU C Compiler (GCC) for ARM, with no restrictions on code size or end product distribution, are included with the tool distribution. Upgrading to more optimizing compilers is a snap with support for the professional Keil C51 product and ARM RealView™ compiler.

7.1.4.5 Nonintrusive Debugging

Figure 7-5. PSoC Creator Debugger



With JTAG (4-wire) and SWD (2-wire) debug connectivity available on all devices, the PSoC Creator debugger offers full control over the target device with minimum intrusion. Breakpoints and code execution commands are all readily available from toolbar buttons and an impressive lineup of windows—register, locals, watch, call stack, memory and peripherals—make for an unparalleled level of visibility into the system.

- Logical OR
- Logical XOR
- Pass, used to pass a value through the ALU to the shift register, mask, or another UDB register

Independent of the ALU operation, these functions are available:

- Shift left
- Shift right
- Nibble swap
- Bitwise OR mask

7.2.2.3 Conditionals

Each datapath has two compares, with bit masking options. Compare operands include the two accumulators and the two data registers in a variety of configurations. Other conditions include zero detect, all ones detect, and overflow. These conditions are the primary datapath outputs, a selection of which can be driven out to the UDB routing matrix. Conditional computation can use the built in chaining to neighboring UDBs to operate on wider data widths without the need to use routing resources.

7.2.2.4 Variable MSB

The most significant bit of an arithmetic and shift function can be programmatically specified. This supports variable width CRC and PRS functions, and in conjunction with ALU output masking, can implement arbitrary width timers, counters and shift blocks.

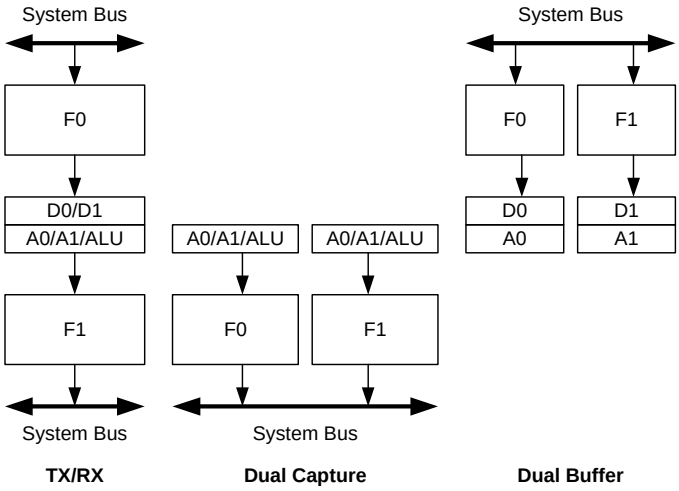
7.2.2.5 Built in CRC/PRS

The datapath has built in support for single cycle Cyclic Redundancy Check (CRC) computation and Pseudo Random Sequence (PRS) generation of arbitrary width and arbitrary polynomial. CRC/PRS functions longer than 8 bits may be implemented in conjunction with PLD logic, or built in chaining may be use to extend the function into neighboring UDBs.

7.2.2.6 Input/Output FIFOs

Each datapath contains two four-byte deep FIFOs, which can be independently configured as an input buffer (system bus writes to the FIFO, datapath internal reads the FIFO), or an output buffer (datapath internal writes to the FIFO, the system bus reads from the FIFO). The FIFOs generate status that are selectable as datapath outputs and can therefore be driven to the routing, to interact with sequencers, interrupts, or DMA.

Figure 7-9. Example FIFO Configurations



7.2.2.7 Chaining

The datapath can be configured to chain conditions and signals such as carries and shift data with neighboring datapaths to create higher precision arithmetic, shift, CRC/PRS functions.

7.2.2.8 Time Multiplexing

In applications that are over sampled, or do not need high clock rates, the single ALU block in the datapath can be efficiently shared with two sets of registers and condition generators. Carry and shift out data from the ALU are registered and can be selected as inputs in subsequent cycles. This provides support for 16-bit functions in one (8-bit) datapath.

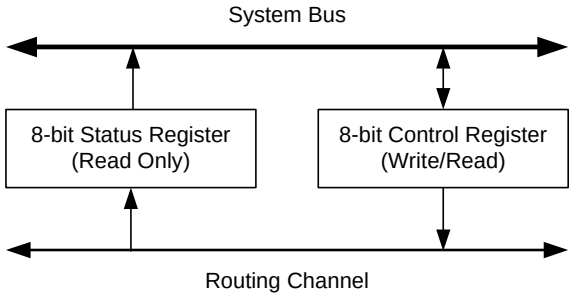
7.2.2.9 Datapath I/O

There are six inputs and six outputs that connect the datapath to the routing matrix. Inputs from the routing provide the configuration for the datapath operation to perform in each cycle, and the serial data inputs. Inputs can be routed from other UDB blocks, other device peripherals, device I/O pins, and so on. The outputs to the routing can be selected from the generated conditions, and the serial data outputs. Outputs can be routed to other UDB blocks, device peripherals, interrupt and DMA controller, I/O pins, and so on.

7.2.3 Status and Control Module

The primary purpose of this circuitry is to coordinate CPU firmware interaction with internal UDB operation.

Figure 7-10. Status and Control Registers



8.1 Analog Routing

The CY8C34 family of devices has a flexible analog routing architecture that provides the capability to connect GPIOs and different analog blocks, and also route signals between different analog blocks. One of the strong points of this flexible routing architecture is that it allows dynamic routing of input and output connections to the different analog blocks.

8.1.1 Features

- Flexible, configurable analog routing architecture
- 16 Analog globals (AG) and two analog mux buses (AMUXBUS) to connect GPIOs and the analog blocks
- Each GPIO is connected to one analog global and one analog mux bus
- 8 Analog local buses (abus) to route signals between the different analog blocks
- Multiplexers and switches for input and output selection of the analog blocks

8.1.2 Functional Description

Analog globals (AGs) and analog mux buses (AMUXBUS) provide analog connectivity between GPIOs and the various analog blocks. There are 16 AGs in the CY8C34 family. The analog routing architecture is divided into four quadrants as shown in Figure 8-2. Each quadrant has four analog globals (AGL[0..3], AGL[4..7], AGR[0..3], AGR[4..7]). Each GPIO is connected to the corresponding AG through an analog switch. The analog mux bus is a shared routing resource that connects to every GPIO through an analog switch. There are two AMUXBUS routes in CY8C34, one in the left half (AMUXBUSL) and one in the right half (AMUXBUSR), as shown in Figure 8-2.

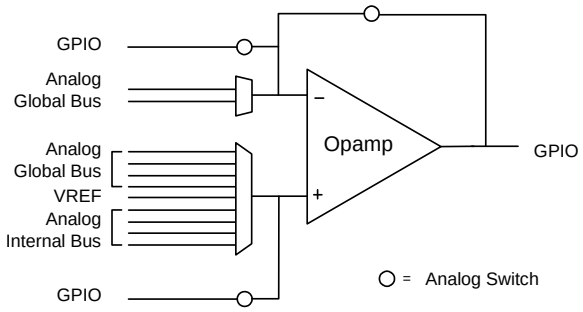
Table 8-1. LUT Function vs. Program Word and Inputs

Control Word	Output (A and B are LUT inputs)
0000b	**FALSE** (‘0’)
0001b	**A** AND **B**
0010b	**A** AND (NOT **B**)
0011b	A
0100b	(NOT **A**) AND **B**
0101b	B
0110b	**A** XOR **B**
0111b	**A** OR **B**
1000b	**A** NOR **B**
1001b	**A** XNOR **B**
1010b	NOT **B**
1011b	**A** OR (NOT **B**)
1100b	NOT **A**
1101b	(NOT **A**) OR **B**
1110b	**A** NAND **B**
1111b	**TRUE** (‘1’)

8.4 Opamps

The CY8C34 family of devices contains two general purpose opamps in a device.

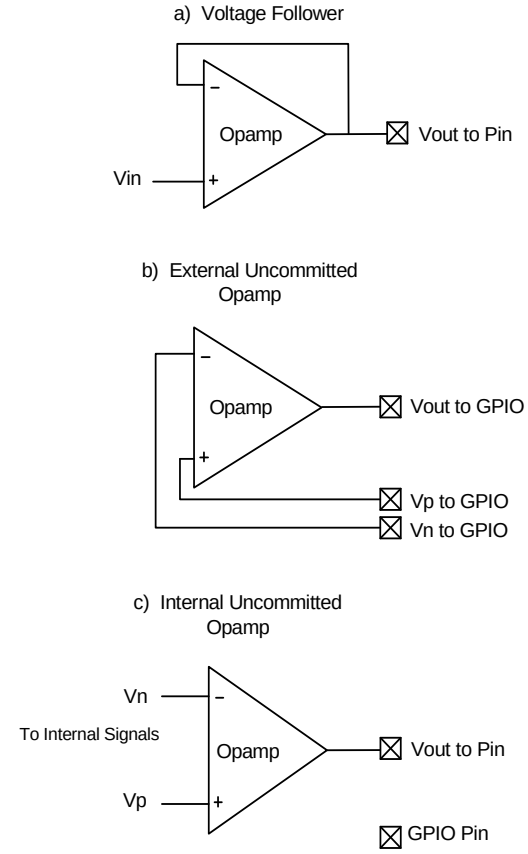
Figure 8-5. Opamp



The opamp is uncommitted and can be configured as a gain stage or voltage follower, or output buffer on external or internal signals.

See Figure 8-6. In any configuration, the input and output signals can all be connected to the internal global signals and monitored with an ADC, or comparator. The configurations are implemented with switches between the signals and GPIO pins.

Figure 8-6. Opamp Configurations



The opamp has three speed modes, slow, medium, and fast. The slow mode consumes the least amount of quiescent power and the fast mode consumes the most power. The inputs are able to swing rail-to-rail. The output swing is capable of rail-to-rail operation at low current output, within 50 mV of the rails. When driving high current loads (about 25 mA) the output voltage may only get within 500 mV of the rails.

8.5 Programmable SC/CT Blocks

The CY8C34 family of devices contains two switched capacitor/continuous time (SC/CT) blocks in a device. Each switched capacitor/continuous time block is built around a single rail-to-rail high bandwidth opamp.

Switched capacitor is a circuit design technique that uses capacitors plus switches instead of resistors to create analog functions. These circuits work by moving charge between capacitors by opening and closing different switches. Nonoverlapping in phase clock signals control the switches, so that not all switches are ON simultaneously.

The PSoC Creator tool offers a user friendly interface, which allows you to easily program the SC/CT blocks. Switch control and clock phase control configuration is done by PSoC Creator so users only need to determine the application use parameters such as gain, amplifier polarity, vref connection, and so on.

The same opamps and block interfaces are also connectable to an array of resistors which allows the construction of a variety of continuous time functions.

The opamp and resistor array is programmable to perform various analog functions including

- Naked Operational Amplifier - Continuous Mode
- Unity-Gain Buffer - Continuous Mode
- Programmable Gain Amplifier (PGA) - Continuous Mode
- Transimpedance Amplifier (TIA) - Continuous Mode
- Up/Down Mixer - Continuous Mode
- Sample and Hold Mixer (NRZ S/H) - Switched Cap Mode
- First Order Analog to Digital Modulator - Switched Cap Mode

8.5.1 Naked Opamp

The Naked Opamp presents both inputs and the output for connection to internal or external signals. The opamp has a unity gain bandwidth greater than 6.0 MHz and output drive current up to 650 µA. This is sufficient for buffering internal signals (such as DAC outputs) and driving external loads greater than 7.5 kohms.

8.5.2 Unity Gain

The Unity Gain buffer is a Naked Opamp with the output directly connected to the inverting input for a gain of 1.00. It has a -3 dB bandwidth greater than 6.0 MHz.

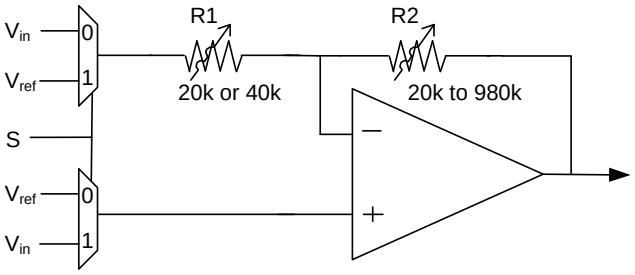
8.5.3 PGA

The PGA amplifies an external or internal signal. The PGA can be configured to operate in inverting mode or noninverting mode. The PGA function may be configured for both positive and negative gains as high as 50 and 49 respectively. The gain is adjusted by changing the values of R1 and R2 as illustrated in Figure 8-7. The schematic in Figure 8-7 shows the configuration and possible resistor settings for the PGA. The gain is switched from inverting and non inverting by changing the shared select value of the both the input muxes. The bandwidth for each gain case is listed in Table 8-2.

Table 8-2. Bandwidth

Gain	Bandwidth
1	6.0 MHz
24	340 kHz
48	220 kHz
50	215 kHz

Figure 8-7. PGA Resistor Settings



The PGA is used in applications where the input signal may not be large enough to achieve the desired resolution in the ADC, or dynamic range of another SC/CT block such as a mixer. The gain is adjustable at runtime, including changing the gain of the PGA prior to each ADC sample.

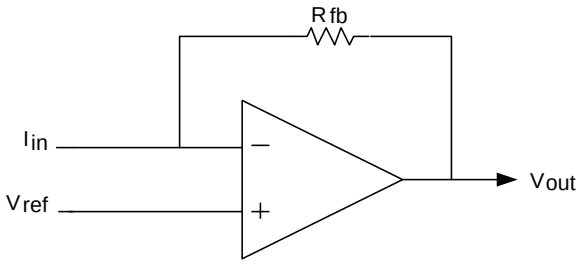
8.5.4 TIA

The Transimpedance Amplifier (TIA) converts an internal or external current to an output voltage. The TIA uses an internal feedback resistor in a continuous time configuration to convert input current to output voltage. For an input current Iin, the output voltage is Iin x Rfb +Vref, where Vref is the value placed on the non inverting input. The feedback resistor Rfb is programmable between 20 KΩ and 1 MΩ through a configuration register. Table 8-3 shows the possible values of Rfb and associated configuration settings.

Table 8-3. Feedback Resistor Settings

Configuration Word	Nominal R_{fb} (KΩ)
000b	20
001b	30
010b	40
011b	60
100b	120
101b	250
110b	500
111b	1000

Figure 8-8. Continuous Time TIA Schematic



11.2 Device Level Specifications

Specifications are valid for -40°C ≤ T_A ≤ 85°C and T_J ≤ 100°C, except where noted. Specifications are valid for 1.71V to 5.5V, except where noted.

11.2.1 Device Level Specifications

Table 11-2. DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{DDA}	Analog supply voltage and input to analog core regulator	Analog core regulator enabled	1.8		5.5	V
V_{DDA}	Analog supply voltage, analog regulator bypassed	Analog core regulator disabled	1.71	1.8	1.89	V
V_{DDD}	Digital supply voltage relative to Vssd	Digital core regulator enabled	1.8		V_{DDA}	V
V_{DDD}	Digital supply voltage, digital regulator bypassed	Digital core regulator disabled	1.71	1.8	1.89	V
Vddio[5]	I/O supply voltage relative to Vssio		1.71		V_{DDA}	V
Vcca	Direct analog core voltage input (Analog regulator bypass)	Analog core regulator disabled	1.71	1.8	1.89	V
Vccd	Direct digital core voltage input (Digital regulator bypass)	Digital core regulator disabled	1.71	1.8	1.89	V
Vbat	Voltage supplied to boost converter		0.5		5.5	V
	Active Mode, V_{DD} = 1.71V - 5.5V					
Idd[6]	Execute from CPU instruction buffer. See "Flash Program Memory" on page 18.					
	CPU at 3 MHz	T= -40°C				mA
		T= 25°C		0.8		mA
		T= 85°C				mA
	CPU at 6 MHz	T= -40°C				mA
		T= 25°C		1.2		mA
		T= 85°C				mA
	CPU at 12 MHz	T= -40°C				mA
		T= 25°C		2.0		mA
		T= 85°C				mA
	CPU at 24 MHz	T= -40°C				mA
		T= 25°C		3.5		mA
		T= 85°C				mA
	CPU at 50 MHz	T= -40°C				mA
		T= 25°C		6.6		mA
		T= 85°C				mA

11.4.2 SIO

Table 11-10. SIO DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Vinref	Input voltage reference (Differential input mode)		0.5	-	0.52 ×Vddio	V
Voutref	Output voltage reference (Regulated output mode)					
		Vddio > 3.7	1	-	Vddio-1	V
		Vddio < 3.7	1	-	Vddio - 0.5	V
Vih	Input voltage high threshold					
	GPIO mode	CMOS input	0.7 × Vddio	-	-	V
	Differential input mode	Hysteresis disabled	Vinref+0.1	-	-	V
Vil	Input voltage low threshold					
	GPIO mode	CMOS input	-	-	0.3 × Vddio	V
	Differential input mode	Hysteresis disabled	-	-	Vinref-0.1	V
Voh	Output voltage high					
	Unregulated mode	Ioh = 4 mA, Vddio = 3.3V	Vddio - 0.4	-	-	V
	Regulated mode	Ioh = 1 mA	Voutref-0.6	-	Voutref+0.2	V
	Regulated mode	Ioh = 0.1 mA	Voutref-0.25	-	Voutref+0.2	V
Vol	Output voltage low					
		Vddio = 3.30V, Iol = 25 mA	-	-	0.8	V
		Vddio = 1.80V, Iol = 4 mA	-	-	0.4	V
Rpullup	Pull up resistor		4	5.6	8	kΩ
Rpulldown	Pull down resistor		4	5.6	8	kΩ
Iil	Input leakage current (absolute value)[9]					
	Vih ≤ Vddsio	25°C, Vddsio = 3.0V, Vih = 3.0V	-	-	14	nA
	Vih > Vddsio	25°C, Vddsio = 0V, Vih = 3.0V	-	-	10	µA
Cin	Input Capacitance[9]		-	-	7	pF
Vh	Input voltage hysteresis (Schmitt-Trigger)[9]	Single ended mode (GPIO mode)	-	40	-	mV
		Differential mode	-	50	-	mV
Idiode	Current through protection diode to Vssio		-	-	100	µA

Table 11-11. SIO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
TriseF	Rise time in Fast Strong Mode (90/10%)[9]	Cload = 25 pF, Vddio = 3.3V	1	-	12	ns
TfallF	Fall time in Fast Strong Mode (90/10%)[9]	Cload = 25 pF, Vddio = 3.3V	1	-	12	ns
TriseS	Rise time in Slow Strong Mode (90/10%)[9]	Cload = 25 pF, Vddio = 3.0V	10	-	75	ns
TfallS	Fall time in Slow Strong Mode (90/10%)[9]	Cload = 25 pF, Vddio = 3.0V	10	-	60	ns

11.5.10 Transimpedance Amplifier

The TIA is created using a SC/CT Analog Block, see the TIA component data sheet in PSoC Creator for full AC/DC specifications, and APIs and example code.

Table 11-33. Transimpedance Amplifier (TIA) DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Vioff	Input offset voltage		-	-	10	mV
Rconv	Conversion resistance[16]					
	R = 20K	40 pF load	-20	-	+30	%
	R = 30K	40 pF load	-20	-	+30	%
	R = 40K	40 pF load	-20	-	+30	%
	R = 80K	40 pF load	-20	-	+30	%
	R = 120K	40 pF load	-20	-	+30	%
	R = 250K	40 pF load	-20	-	+30	%
	R= 500K	40 pF load	-20	-	+30	%
	R = 1M	40 pF load	-20	-	+30	%
	Quiescent current		-	900	-	µA

Table 11-34. Transimpedance Amplifier (TIA) AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Input bandwidth (-3 dB) - 20 pF load[15]					
	R = 20K		1800	-	-	kHz
	R = 120K		330	-	-	kHz
	R = 1M		47	-	-	kHz
	Input bandwidth (3 dB) - 40 pF load					
	R = 20K		1500	-	-	kHz
	R = 120K		300	-	-	kHz
	R = 1M		46	-	-	kHz

Note

16. Conversion resistance values are not calibrated. Calibrated values and details about calibration are provided in PSoC Creator component data sheets. External precision resistors can also be used.

Table 11-59. NVL AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	NVL endurance	Programmed at 25°C	1K	-	-	program/ erase cycles
		Programmed at 0 to 70°C	100	-	-	program/ erase cycles
	NVL data retention time	Programmed at 25°C	20	-	-	years
		Programmed at 0 to 70°C	20	-	-	years

11.7.4 SRAM

Table 11-60. SRAM DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Vsram	SRAM retention voltage		1.2	-	-	V

Table 11-61. SRAM AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Fsram	SRAM operating frequency		DC	-	50	MHz

11.7.5 External Memory Interface

Figure 11-3. Asynchronous Read Cycle Timing

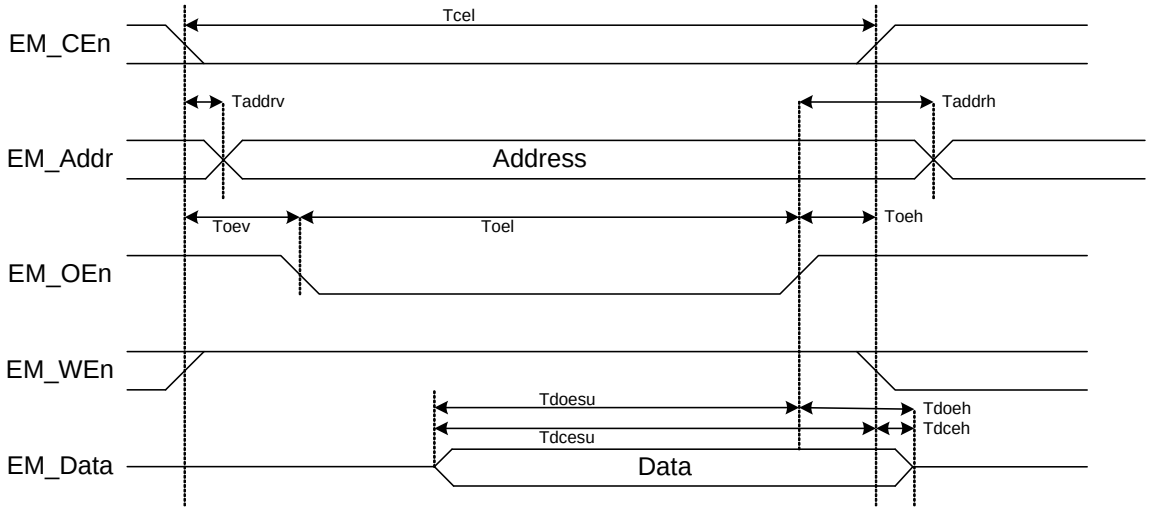


Table 11-62. Asynchronous Read Cycle Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T	EMIF Clock period		30.3	-	-	ns
Tcel	EM_CEn low time		2*T-1	-	2*T+2	ns
Taddrv	EM_CEn low to EM_Addr valid		-	-	5	ns
Taddrh	Address hold time after EM_OEn high		2	-	-	ns
Toev	EM_CEn low to EM_OEn low		-5	-	5	ns

Table 11-62. Asynchronous Read Cycle Specifications (continued)

Parameter	Description	Conditions	Min	Typ	Max	Units
Toel	EM_OEn low time		2*T-1	-	2*T+2	ns
Toeh	EM_OEn high to EM_CEn high hold time		-5	-	5	ns
Tdoesu	Data to EM_OEn high setup time		T+20	-	-	ns
Tdcesu	Data to EM_CEn high setup time		T+20	-	-	ns
Tdoeh	Data hold time after EM_OEn high		3	-	-	ns
Tdceh	Data hold time after EM_CEn high		3	-	-	ns

Figure 11-4. Asynchronous Write Cycle Timing

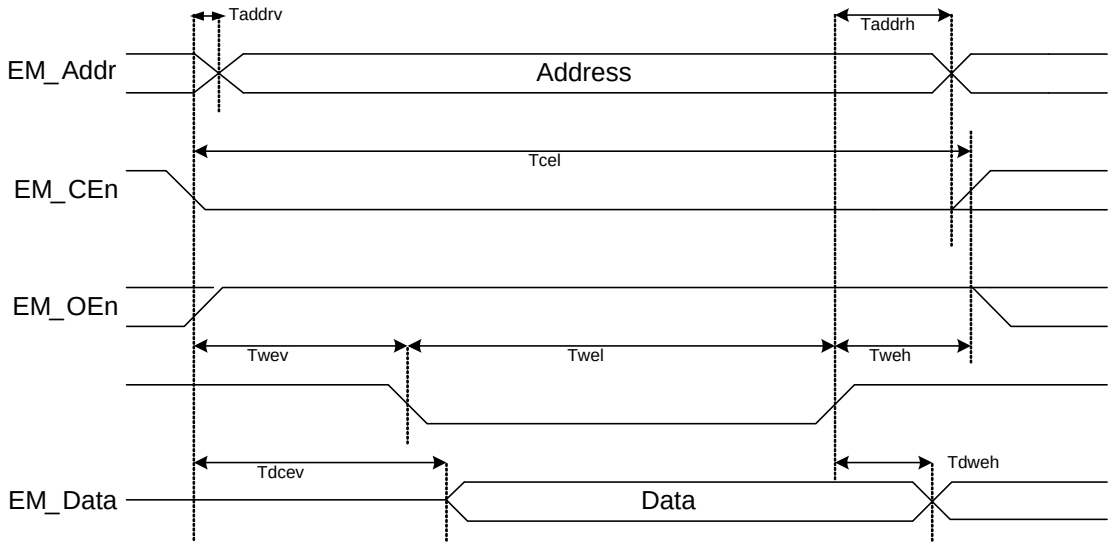


Table 11-63. Asynchronous Write Cycle Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T	EMIF Clock period		30.3	-	-	ns
Taddrv	EM_CEn low to EM_Addr valid		-	-	5	ns
Taddrh	Address hold time after EM_WEn high		T+2	-	-	ns
Tcel	EM_CEn low time		2*T-1	-	2*T+2	ns
Twev	EM_CEn low to EM_WEn low		-5	-	5	ns
Twel	EM_WEn low time		T-1	-	T+2	ns
Tweh	EM_WEn high to EM_CEn high hold time		T	-	-	ns
Tdcev	EM_CEn low to data valid		-	-	7	ns
Tdweh	Data hold time after EM_WEn high		T	-	-	ns

11.8.3 Interrupt Controller

Table 11-71. Interrupt Controller AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Delay from Interrupt signal input to ISR code execution from ISR code	Includes worse case completion of longest instruction DIV with 6 cycles	-	-	25	Tcy CPU

11.8.4 JTAG Interface

Table 11-72. JTAG Interface AC Specifications[9]

Parameter	Description	Conditions	Min	Typ	Max	Units
f_TCK	TCK frequency	$3.3V \le V_{DDD} \le 5V$	-	-	14[20]	MHz
		$1.71V \le V_{DDD} < 3.3V$	-	-	TBD[20]	MHz
T_TDI_setup	TDI, TMS setup before TCK high		0	-	-	ns
T_TDI_hold	TDI, TMS hold after TCK high	T = 1/f_TCK	T/4	-	-	
T_TDO_valid	TCK low to TDO valid	T = 1/f_TCK	2T/5	-	-	
T_TDO_hold	TDO hold after TCK high	T = 1/f_TCK	T/4	-	-	
	TCK to device outputs valid		-	-	TBD	ns

11.8.5 SWD Interface

Table 11-73. SWD Interface AC Specifications[9]

Parameter	Description	Conditions	Min	Typ	Max	Units
f_SWDCK	SWDCLK frequency	$3.3V \le V_{DDD} \le 5V$	-	-	14[21]	MHz
		$1.71V \le V_{DDD} < 3.3V$	-	-	TBD[21]	MHz
		$1.71V \le V_{DDD} < 3.3V$, SWD over USBIO pins	-	-	6[21]	MHz
T_SWDI_setup	SWDIO input setup before SWDCK high	T = 1/f_SWDCK	T/4	-	-	
T_SWDI_hold	SWDIO input hold after SWDCK high	T = 1/f_SWDCK	T/4	-	-	
T_SWDO_valid	SWDCK low to SWDIO output valid	T = 1/f_SWDCK	2T/5	-	-	
T_SWDO_hold	SWDIO output hold after SWDCK high	T = 1/f_SWDCK	T/4	-	-	

11.8.6 SWV Interface

Table 11-74. SWV Interface AC Specifications[9]

Parameter	Description	Conditions	Min	Typ	Max	Units
	SWV mode SWV bit rate		-	-	33	Mbit

Notes
20. f_TCK must also be no more than 1/3 CPU clock frequency.
21. f_SWDCK must also be no more than 1/3 CPU clock frequency.

13. Packaging

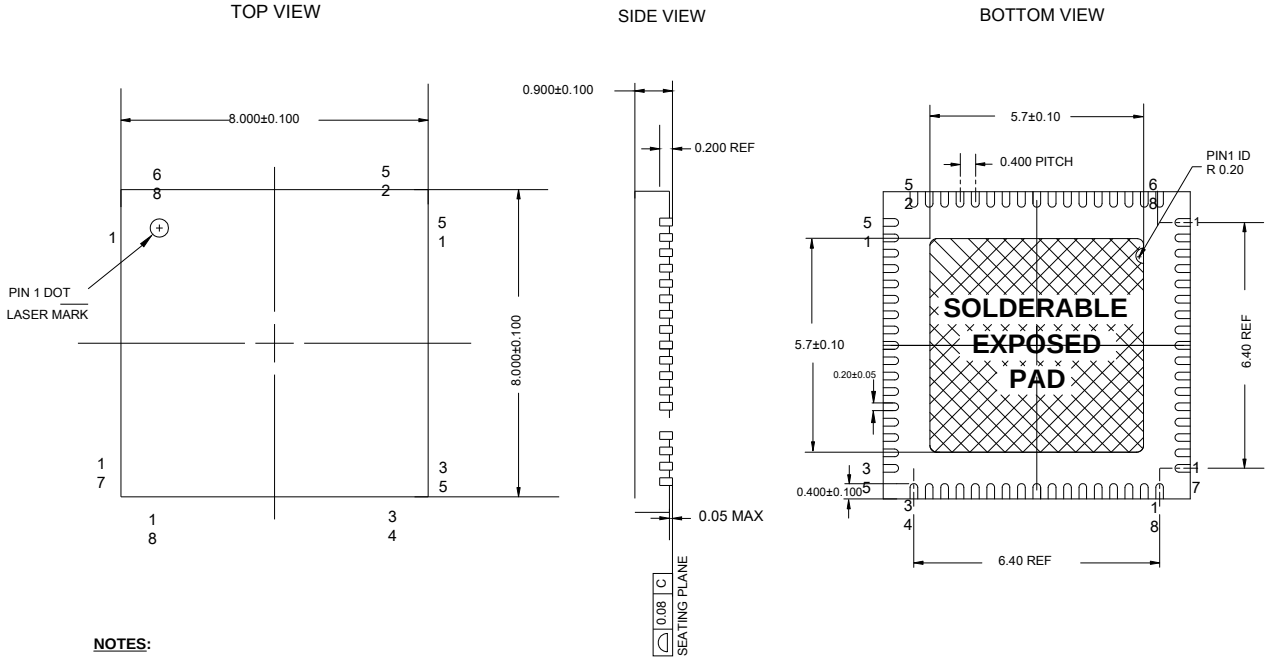
Table 13-1. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Operating ambient temperature		-40	25.00	85	°C
T_J	Operating junction temperature		-40	-	100	°C
Tja	Package θJA (48 SSOP)		-	45.16	-	°C/Watt
Tja	Package θJA (48 QFN)		-	15.94	-	°C/Watt
Tja	Package θJA (68 QFN)		-	11.72	-	°C/Watt
Tja	Package θJA (100 TQFP)		-	30.52	-	°C/Watt
Tjc	Package θJC (48 SSOP)		-	27.84	-	°C/Watt
Tjc	Package θJC (48 QFN)		-	7.05	-	°C/Watt
Tjc	Package θJC (68 QFN)		-	6.32	-	°C/Watt
Tjc	Package θJC (100 TQFP)		-	9.04	-	°C/Watt
	Pb-Free assemblies (20s to 40s) - Sn-Ag-Cu solder paste reflow temperature		235	-	245	°C
	Pb-Free assemblies (20s to 40s) - Sn-Pb solder paste reflow temperature		205	-	220	°C

Table 13-2. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
48-SSOP	MSL 1
48-QFN	MSL 3
68-QFN	MSL 3
100-TQFP	MSL 3

Figure 13-3. 68-Pin QFN 8x8 with 0.4 mm Pitch Package Outline (Sawn Version)

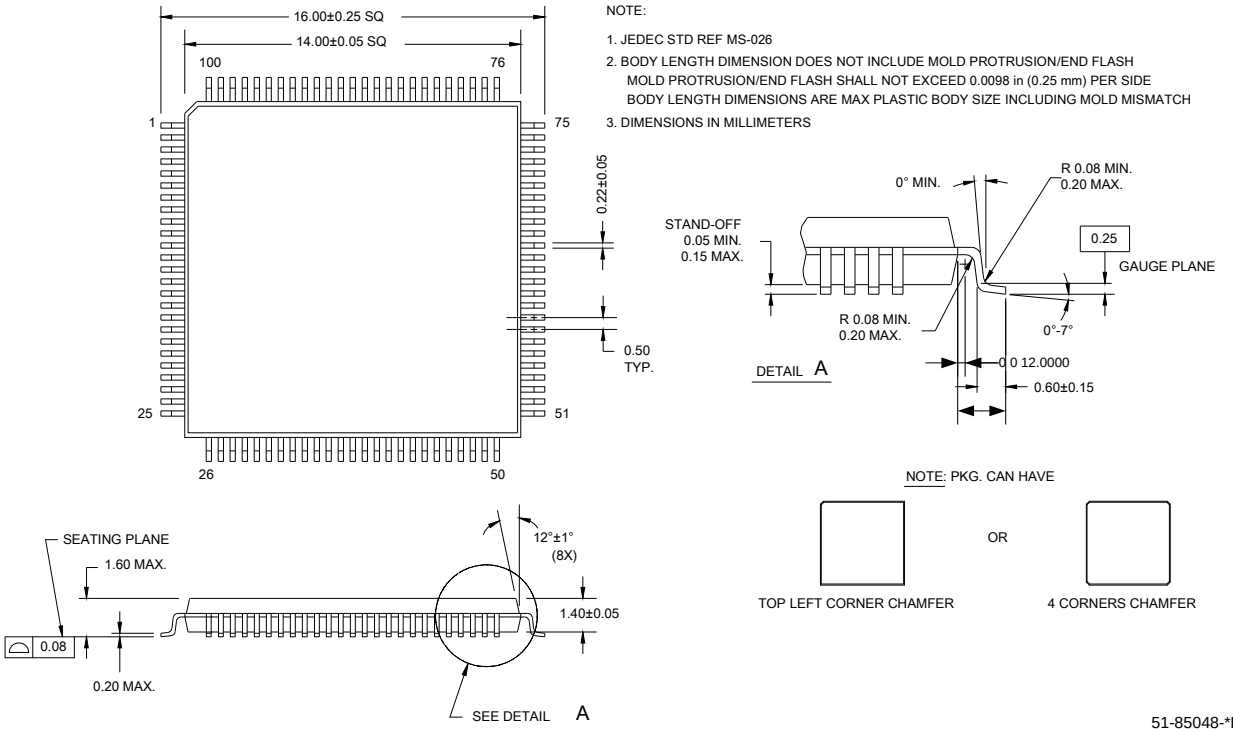


NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 0.17g
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-09618 *C

Figure 13-4. 100-Pin TQFP (14 x 14 x 1.4 mm) Package Outline



51-85048-*D

Description Title: PSoC® 3: CY8C34 Family Data Sheet Programmable System-on-Chip (PSoC®) Document Number: 001-53304				
*D	2903576	04/01/10	MKEA	Updated Vb pin in PCB Schematic Updated Tstartup parameter in AC Specifications table Added Load regulation and Line regulation parameters to Inductive Boost Regulator DC Specifications table Updated Icc parameter in LCD Direct Drive DC Specs table In page 1, updated internal oscillator range under Precision programmable clocking to start from 3 MHz Updated Iout parameter in LCD Direct Drive DC Specs table Updated Table 6-2 and Table 6-3 Removed DFB block in Figure 1-1. Added bullets on CapSense in page 1; added CapSense column in Section 12 Removed some references to footnote [1] Changed INC_Rn cycles from 3 to 2 (Table 4-1) Added footnote in PLL AC Specification table Added PLL intermediate frequency row with footnote in PLL AC Specs table Added UDBs subsection under 11.6 Digital Peripherals Updated Figure 2-6 (PCB Layout) Updated Pin Descriptions section and modified Figures 6-6, 6-8, 6-9 Updated LVD in Tables 6-2 and 6-3; modified Low power modes bullet in page 1 Added note to Figures 2-5 and 6-2; Updated Figure 6-2 to add capacitors for V_{DDA} and V_{DDD} pins. Updated boost converter section (6.2.2) Updated Tstartup values in Table 11-3. Removed IPOR rows from Table 11-67. Updated 6.3.1.1, Power Voltage Level Monitors. Updated section 5.2 and Table 11-2 to correct suggestion of execution from flash. Updated IMO max frequency in Figure 6-1, Table 11-77, and Table 11-78. Updated Vref specs in Table 11-21. Updated IDAC uncompensated gain error in Table 11-25. Updated Delay from Interrupt signal input to ISR code execution from ISR code in Table 11-57. Removed other line in table. Added sentence to last paragraph of section 6.1.1.3. Updated Tresp, high and low power modes, in Table 11-24. Updated f_TCK values in Table 11-72 and f_SWDCK values in Table 11-73. Updated SNR condition in Table 11-20. Updated sleep wakeup time in Table 6-3 and Tsleep in Table 11-3. Added 1.71V <= V_{DDD} < 3.3V, SWD over USBIO pins value to Table 11-73. Removed mention of hibernate reset (HRES) from page 1 features, Table 6-3, Section 6.2.1.4, Section 6.3, and Section 6.3.1.1. Change PPOR/PRES to TBDs in Section 6.3.1.1, Section 6.4.1.6 (changed PPOR to reset), Table 11-3 (changed PPOR to PRES), Table 11-67 (changed title, values TBD), and Table 11-68 (changed PPOR_TR to PRES_TR). Added sentence saying that LVD circuits can generate a reset to Section 6.3.1.1. Changed Idd values on page 1, page 5, and Table 11-2. Changed resume time value in Section 6.2.1.3. Changed ESD HBM value in Table 11-1. Changed sample rate row in Table 11-20. Removed V_{DDA} = 1.65V rows and changed BWag value in Table 11-22. Changed Vioff values and changed CMRR value in Table 11-23. Changed INL max value in Table 11-27. Added max value to the Quiescent current specs in Tables 11-29 and 11-31. Changed occurrences of “Block” to “Row” and deleted the “ECC not included” footnote in Table 11-55. Changed max response time value in Tables 11-68 and 11-70. Changed the Startup time in Table 11-78. Added condition to intermediate frequency row in Table 11-84. Added row to Table 11-68. Added brown out note to Section 11.8.1.