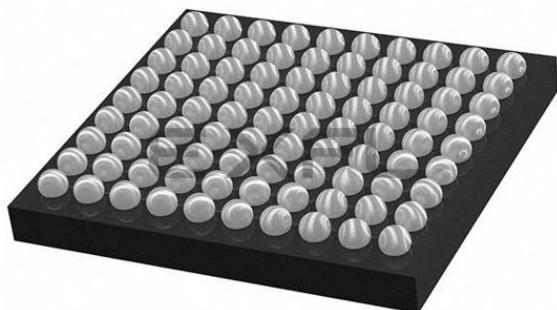




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Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	168MHz
Connectivity	CANbus, EBI/EMI, I ² C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LCD, POR, PWM, WDT
Number of I/O	72
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 13x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	90-UFBGA, WLCSP
Supplier Device Package	90-WLCSP (4.22x3.97)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f405oeiy6btr

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1 Introduction

This datasheet provides the description of the STM32F405xx and STM32F407xx lines of microcontrollers. For more details on the whole STMicroelectronics STM32™ family, please refer to [Section 2.1: Full compatibility throughout the family](#).

The STM32F405xx and STM32F407xx datasheet should be read in conjunction with the STM32F4xx reference manual which is available from the STMicroelectronics website www.st.com.

For information on the Cortex®-M4 core, please refer to the Cortex®-M4 programming manual (PM0214) available from www.st.com.

2.2.26 Audio PLL (PLLI2S)

The devices feature an additional dedicated PLL for audio I²S application. It allows to achieve error-free I²S sampling clock accuracy without compromising on the CPU performance, while using USB peripherals.

The PLLI2S configuration can be modified to manage an I²S sample rate change without disabling the main PLL (PLL) used for CPU, USB and Ethernet interfaces.

The audio PLL can be programmed with very low error to obtain sampling rates ranging from 8 KHz to 192 KHz.

In addition to the audio PLL, a master clock input pin can be used to synchronize the I²S flow with an external PLL (or Codec output).

2.2.27 Secure digital input/output interface (SDIO)

An SD/SDIO/MMC host interface is available, that supports MultiMediaCard System Specification Version 4.2 in three different databus modes: 1-bit (default), 4-bit and 8-bit.

The interface allows data transfer at up to 48 MHz, and is compliant with the SD Memory Card Specification Version 2.0.

The SDIO Card Specification Version 2.0 is also supported with two different databus modes: 1-bit (default) and 4-bit.

The current version supports only one SD/SDIO/MMC4.2 card at any one time and a stack of MMC4.1 or previous.

In addition to SD/SDIO/MMC, this interface is fully compliant with the CE-ATA digital protocol Rev1.1.

2.2.28 Ethernet MAC interface with dedicated DMA and IEEE 1588 support

Peripheral available only on the STM32F407xx devices.

The STM32F407xx devices provide an IEEE-802.3-2002-compliant media access controller (MAC) for ethernet LAN communications through an industry-standard medium-independent interface (MII) or a reduced medium-independent interface (RMII). The STM32F407xx requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). the PHY is connected to the STM32F407xx MII port using 17 signals for MII or 9 signals for RMII, and can be clocked using the 25 MHz (MII) from the STM32F407xx.

Table 7. STM32F40xxx pin and ball definitions (continued)

Pin number						Pin name (function after reset) ⁽¹⁾	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP64	WLCSP90	LQFP100	LQFP144	UFBGA176	LQFP176						
-	-	-	11	H3	17	PF1	I/O	FT	-	FSMC_A1 / I2C2_SCL / EVENTOUT	-
-	-	-	12	H2	18	PF2	I/O	FT	-	FSMC_A2 / I2C2_SMBA / EVENTOUT	-
-	-	-	13	J2	19	PF3	I/O	FT	(4)	FSMC_A3/EVENTOUT	ADC3_IN9
-	-	-	14	J3	20	PF4	I/O	FT	(4)	FSMC_A4/EVENTOUT	ADC3_IN14
-	-	-	15	K3	21	PF5	I/O	FT	(4)	FSMC_A5/EVENTOUT	ADC3_IN15
-	C9	10	16	G2	22	V _{SS}	S	-	-	-	-
-	B8	11	17	G3	23	V _{DD}	S	-	-	-	-
-	-	-	18	K2	24	PF6	I/O	FT	(4)	TIM10_CH1 / FSMC_NIORD/ EVENTOUT	ADC3_IN4
-	-	-	19	K1	25	PF7	I/O	FT	(4)	TIM11_CH1/FSMC_NREG/ EVENTOUT	ADC3_IN5
-	-	-	20	L3	26	PF8	I/O	FT	(4)	TIM13_CH1 / FSMC_NIOWR/ EVENTOUT	ADC3_IN6
-	-	-	21	L2	27	PF9	I/O	FT	(4)	TIM14_CH1 / FSMC_CD/ EVENTOUT	ADC3_IN7
-	-	-	22	L1	28	PF10	I/O	FT	(4)	FSMC_INTR/ EVENTOUT	ADC3_IN8
5	F10	12	23	G1	29	PH0/OSC_IN (PH0)	I/O	FT	-	EVENTOUT	OSC_IN ⁽⁴⁾
6	F9	13	24	H1	30	PH1/OSC_OUT (PH1)	I/O	FT	-	EVENTOUT	OSC_OUT ⁽⁴⁾
7	G10	14	25	J1	31	NRST	I/O	RST	-	-	-
8	E10	15	26	M2	32	PC0	I/O	FT	(4)	OTG_HS_ULPI_STP/ EVENTOUT	ADC123_IN10
9	-	16	27	M3	33	PC1	I/O	FT	(4)	ETH_MDC/ EVENTOUT	ADC123_IN11
10	D10	17	28	M4	34	PC2	I/O	FT	(4)	SPI2_MISO / OTG_HS_ULPI_DIR / ETH_MII_TXD2 /I2S2ext_SD/ EVENTOUT	ADC123_IN12

Table 9. Alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/SPI2/I2S2/I2S2ext	SPI3/I2Sext/I2S3	USART1/2/3/I2S3ext	UART4/5/USART6	CAN1/2/TIM12/13/14	OTG_FS/OTG_HS	ETH	FSMC/SDIO/OTG_FS	DCMI		
Port D	PD0	-	-	-	-	-	-	-	-	-	CAN1_RX	-	-	FSMC_D2	-	-	EVENTOUT
	PD1	-	-	-	-	-	-	-	-	-	CAN1_TX	-	-	FSMC_D3	-	-	EVENTOUT
	PD2	-	-	TIM3_ETR	-	-	-	-	-	UART5_RX	-	-	-	SDIO_CMD	DCMI_D11	-	EVENTOUT
	PD3	-	-	-	-	-	-	-	USART2_CTS	-	-	-	-	FSMC_CLK	-	-	EVENTOUT
	PD4	-	-	-	-	-	-	-	USART2_RTS	-	-	-	-	FSMC_NOE	-	-	EVENTOUT
	PD5	-	-	-	-	-	-	-	USART2_TX	-	-	-	-	FSMC_NWE	-	-	EVENTOUT
	PD6	-	-	-	-	-	-	-	USART2_RX	-	-	-	-	FSMC_NWAIT	-	-	EVENTOUT
	PD7	-	-	-	-	-	-	-	USART2_CK	-	-	-	-	FSMC_NE1/FSMC_NCE2	-	-	EVENTOUT
	PD8	-	-	-	-	-	-	-	USART3_TX	-	-	-	-	FSMC_D13	-	-	EVENTOUT
	PD9	-	-	-	-	-	-	-	USART3_RX	-	-	-	-	FSMC_D14	-	-	EVENTOUT
	PD10	-	-	-	-	-	-	-	USART3_CK	-	-	-	-	FSMC_D15	-	-	EVENTOUT
	PD11	-	-	-	-	-	-	-	USART3_CTS	-	-	-	-	FSMC_A16	-	-	EVENTOUT
	PD12	-	-	TIM4_CH1	-	-	-	-	USART3_RTS	-	-	-	-	FSMC_A17	-	-	EVENTOUT
	PD13	-	-	TIM4_CH2	-	-	-	-	-	-	-	-	-	FSMC_A18	-	-	EVENTOUT
	PD14	-	-	TIM4_CH3	-	-	-	-	-	-	-	-	-	FSMC_D0	-	-	EVENTOUT
	PD15	-	-	TIM4_CH4	-	-	-	-	-	-	-	-	-	FSMC_D1	-	-	EVENTOUT

5.3.5 Embedded reset and power control block characteristics

The parameters given in [Table 19](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 14](#).

Table 19. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.09	2.14	2.19	V
		PLS[2:0]=000 (falling edge)	1.98	2.04	2.08	V
		PLS[2:0]=001 (rising edge)	2.23	2.30	2.37	V
		PLS[2:0]=001 (falling edge)	2.13	2.19	2.25	V
		PLS[2:0]=010 (rising edge)	2.39	2.45	2.51	V
		PLS[2:0]=010 (falling edge)	2.29	2.35	2.39	V
		PLS[2:0]=011 (rising edge)	2.54	2.60	2.65	V
		PLS[2:0]=011 (falling edge)	2.44	2.51	2.56	V
		PLS[2:0]=100 (rising edge)	2.70	2.76	2.82	V
		PLS[2:0]=100 (falling edge)	2.59	2.66	2.71	V
		PLS[2:0]=101 (rising edge)	2.86	2.93	2.99	V
		PLS[2:0]=101 (falling edge)	2.65	2.84	2.92	V
		PLS[2:0]=110 (rising edge)	2.96	3.03	3.10	V
		PLS[2:0]=110 (falling edge)	2.85	2.93	2.99	V
		PLS[2:0]=111 (rising edge)	3.07	3.14	3.21	V
		PLS[2:0]=111 (falling edge)	2.95	3.03	3.09	V
$V_{PVDhyst}^{(1)}$	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power-on/power-down reset threshold	Falling edge	1.60	1.68	1.76	V
		Rising edge	1.64	1.72	1.80	V
$V_{PDRhyst}^{(1)}$	PDR hysteresis	-	-	40	-	mV
V_{BOR1}	Brownout level 1 threshold	Falling edge	2.13	2.19	2.24	V
		Rising edge	2.23	2.29	2.33	V

Figure 26. Typical current consumption versus temperature, Run mode, code with data processing running from Flash (ART accelerator OFF) or RAM, and peripherals OFF

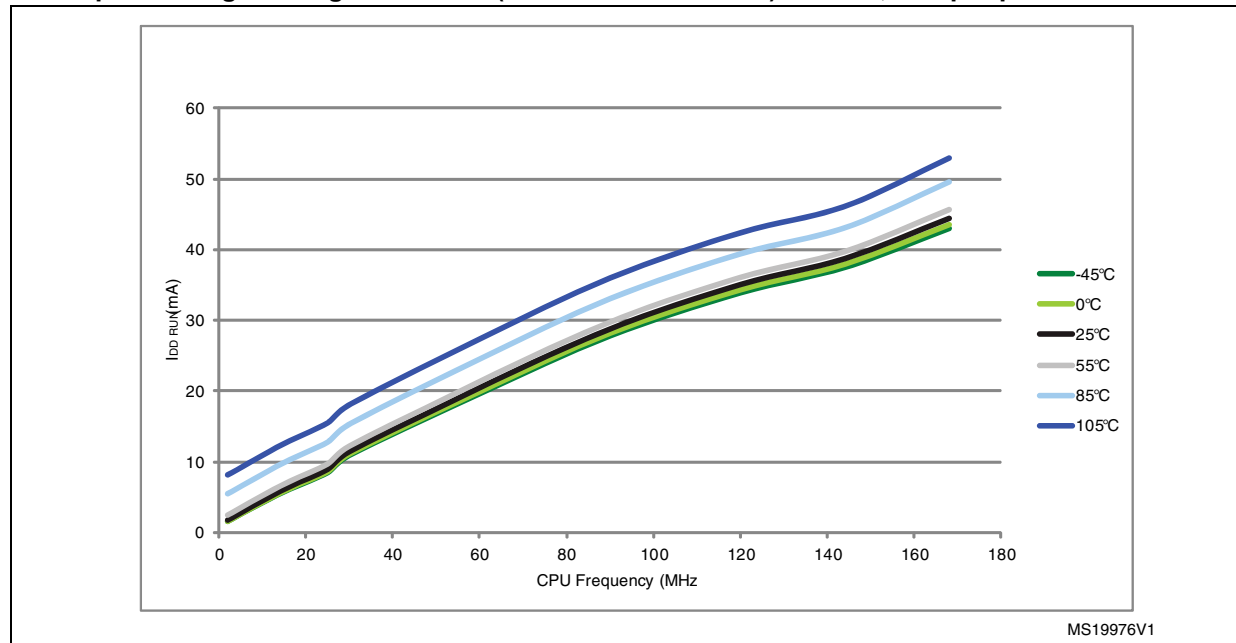


Figure 27. Typical current consumption versus temperature, Run mode, code with data processing running from Flash (ART accelerator OFF) or RAM, and peripherals ON

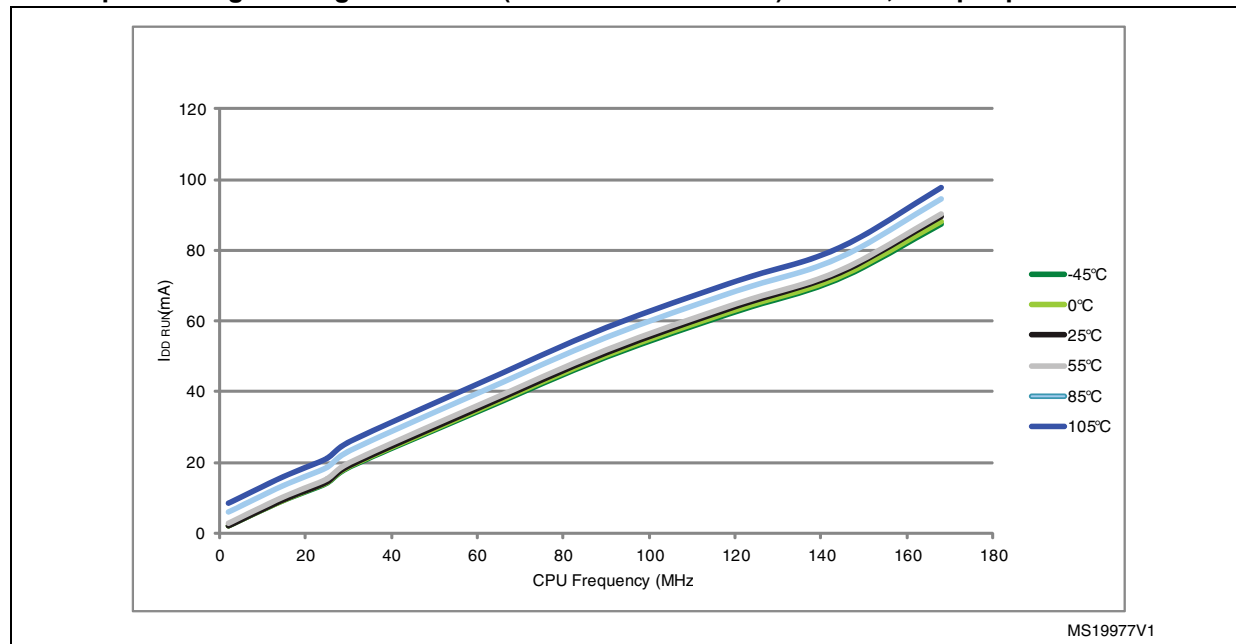


Table 25. Typical and maximum current consumptions in V_{BAT} mode

Symbol	Parameter	Conditions	Typ			Max ⁽¹⁾		Unit
			T _A = 25 °C			T _A = 85 °C	T _A = 105 °C	
			V _{BAT} = 1.8 V	V _{BAT} = 2.4 V	V _{BAT} = 3.3 V	V _{BAT} = 3.6 V		
I _{DD_VBA T}	Backup domain supply current	Backup SRAM ON, low-speed oscillator and RTC ON	1.29	1.42	1.68	6	11	μA
		Backup SRAM OFF, low-speed oscillator and RTC ON	0.62	0.73	0.96	3	5	
		Backup SRAM ON, RTC OFF	0.79	0.81	0.86	5	10	
		Backup SRAM OFF, RTC OFF	0.10	0.10	0.10	2	4	

1. Guaranteed by characterization.

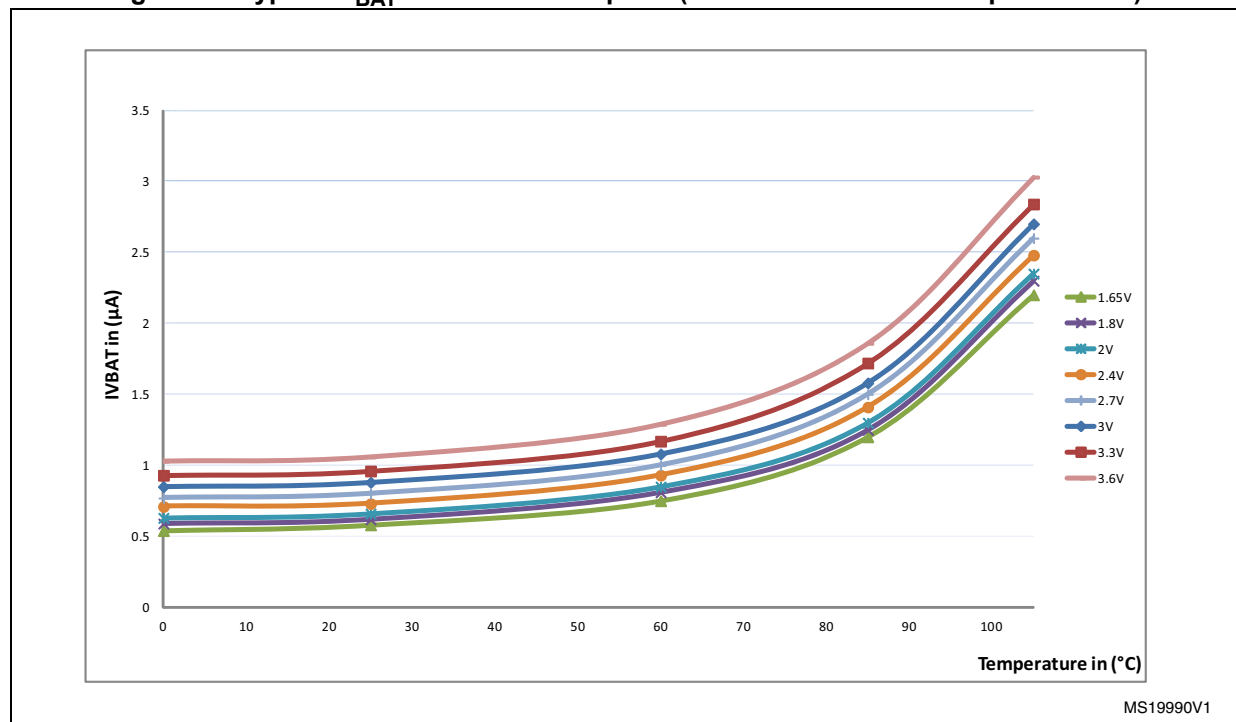
Figure 28. Typical V_{BAT} current consumption (LSE and RTC ON/backup RAM OFF)

Table 37. PLLI2S (audio PLL) characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD(PLLI2S)}^{(4)}$	PLLI2S power consumption on V_{DD}	VCO freq = 100 MHz VCO freq = 432 MHz	0.15 0.45	-	0.40 0.75	mA
$I_{DDA(PLLI2S)}^{(4)}$	PLLI2S power consumption on V_{DDA}	VCO freq = 100 MHz VCO freq = 432 MHz	0.30 0.55	-	0.40 0.85	mA

1. Take care of using the appropriate division factor M to have the specified PLL input clock values.
2. Guaranteed by design.
3. Value given with main PLL running.
4. Guaranteed by characterization.

5.3.11 PLL spread spectrum clock generation (SSCG) characteristics

The spread spectrum clock generation (SSCG) feature allows to reduce electromagnetic interferences (see [Table 44: EMI characteristics](#)). It is available only on the main PLL.

Table 38. SSCG parameters constraint

Symbol	Parameter	Min	Typ	Max ⁽¹⁾	Unit
f_{Mod}	Modulation frequency	-	-	10	KHz
md	Peak modulation depth	0.25	-	2	%
MODEPER * INCSTEP		-	-	$2^{15}-1$	-

1. Guaranteed by design.

Equation 1

The frequency modulation period (MODEPER) is given by the equation below:

$$\text{MODEPER} = \text{round}[f_{\text{PLL_IN}} / (4 \times f_{\text{Mod}})]$$

$f_{\text{PLL_IN}}$ and f_{Mod} must be expressed in Hz.

As an example:

If $f_{\text{PLL_IN}} = 1 \text{ MHz}$, and $f_{\text{MOD}} = 1 \text{ kHz}$, the modulation depth (MODEPER) is given by equation 1:

$$\text{MODEPER} = \text{round}[10^6 / (4 \times 10^3)] = 250$$

Equation 2

Equation 2 allows to calculate the increment step (INCSTEP):

$$\text{INCSTEP} = \text{round}[(2^{15} - 1) \times \text{md} \times \text{PLL_N}] / (100 \times 5 \times \text{MODEPER})$$

$f_{\text{VCO_OUT}}$ must be expressed in MHz.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in [Figure 37](#) and [Table 50](#), respectively.

Unless otherwise specified, the parameters given in [Table 50](#) are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in [Table 14](#).

Table 50. I/O AC characteristics⁽¹⁾⁽²⁾

OSPEEDRy [1:0] bit value ⁽¹⁾	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
00	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 50 \text{ pF}, V_{DD} > 2.70 \text{ V}$	-	-	4	MHz
			$C_L = 50 \text{ pF}, V_{DD} > 1.8 \text{ V}$	-	-	2	
			$C_L = 10 \text{ pF}, V_{DD} > 2.70 \text{ V}$	-	-	8	
			$C_L = 10 \text{ pF}, V_{DD} > 1.8 \text{ V}$	-	-	4	
	$t_{f(\text{IO})\text{out}}/$ $t_{r(\text{IO})\text{out}}$	Output high to low level fall time and output low to high level rise time	$C_L = 50 \text{ pF}, V_{DD} = 1.8 \text{ V to}$ 3.6 V	-	-	100	ns
01	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 50 \text{ pF}, V_{DD} > 2.70 \text{ V}$	-	-	25	MHz
			$C_L = 50 \text{ pF}, V_{DD} > 1.8 \text{ V}$	-	-	12.5	
			$C_L = 10 \text{ pF}, V_{DD} > 2.70 \text{ V}$	-	-	50 ⁽⁴⁾	
			$C_L = 10 \text{ pF}, V_{DD} > 1.8 \text{ V}$	-	-	20	
	$t_{f(\text{IO})\text{out}}/$ $t_{r(\text{IO})\text{out}}$	Output high to low level fall time and output low to high level rise time	$C_L = 50 \text{ pF}, V_{DD} > 2.7 \text{ V}$	-	-	10	ns
			$C_L = 50 \text{ pF}, V_{DD} > 1.8 \text{ V}$	-	-	20	
			$C_L = 10 \text{ pF}, V_{DD} > 2.70 \text{ V}$	-	-	6	
			$C_L = 10 \text{ pF}, V_{DD} > 1.8 \text{ V}$	-	-	10	
10	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 40 \text{ pF}, V_{DD} > 2.70 \text{ V}$	-	-	50 ⁽⁴⁾	MHz
			$C_L = 40 \text{ pF}, V_{DD} > 1.8 \text{ V}$	-	-	25	
			$C_L = 10 \text{ pF}, V_{DD} > 2.70 \text{ V}$	-	-	100 ⁽⁴⁾	
			$C_L = 10 \text{ pF}, V_{DD} > 1.8 \text{ V}$	-	-	50 ⁽⁴⁾	
	$t_{f(\text{IO})\text{out}}/$ $t_{r(\text{IO})\text{out}}$	Output high to low level fall time and output low to high level rise time	$C_L = 40 \text{ pF}, V_{DD} > 2.70 \text{ V}$	-	-	6	ns
			$C_L = 40 \text{ pF}, V_{DD} > 1.8 \text{ V}$	-	-	10	
			$C_L = 10 \text{ pF}, V_{DD} > 2.70 \text{ V}$	-	-	4	
			$C_L = 10 \text{ pF}, V_{DD} > 1.8 \text{ V}$	-	-	6	

Table 50. I/O AC characteristics⁽¹⁾⁽²⁾ (continued)

OSPEEDRy [1:0] bit value ⁽¹⁾	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
11	$F_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 30 \text{ pF}, V_{DD} > 2.70 \text{ V}$	-	-	100 ⁽⁴⁾	MHz
			$C_L = 30 \text{ pF}, V_{DD} > 1.8 \text{ V}$	-	-	50 ⁽⁴⁾	
			$C_L = 10 \text{ pF}, V_{DD} > 2.70 \text{ V}$	-	-	180 ⁽⁴⁾	
			$C_L = 10 \text{ pF}, V_{DD} > 1.8 \text{ V}$	-	-	100 ⁽⁴⁾	
	$t_{f(\text{IO})\text{out}}/$ $t_{r(\text{IO})\text{out}}$	Output high to low level fall time and output low to high level rise time	$C_L = 30 \text{ pF}, V_{DD} > 2.70 \text{ V}$	-	-	4	ns
			$C_L = 30 \text{ pF}, V_{DD} > 1.8 \text{ V}$	-	-	6	
			$C_L = 10 \text{ pF}, V_{DD} > 2.70 \text{ V}$	-	-	2.5	
			$C_L = 10 \text{ pF}, V_{DD} > 1.8 \text{ V}$	-	-	4	
-	$t_{\text{EXTI}pw}$	Pulse width of external signals detected by the EXTI controller		10	-	-	ns

1. Guaranteed by characterization.
2. The I/O speed is configured using the OSPEEDRy[1:0] bits. Refer to the STM32F4xx reference manual for a description of the GPIOx_SPEEDR GPIO port output speed register.
3. The maximum frequency is defined in [Figure 37](#).
4. For maximum frequencies above 50 MHz, the compensation cell should be used.

Figure 37. I/O AC characteristics definition

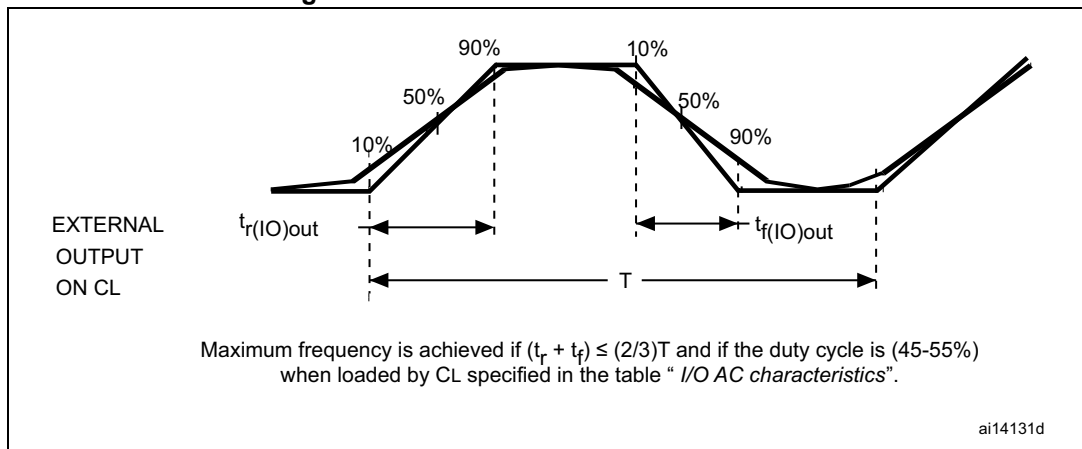
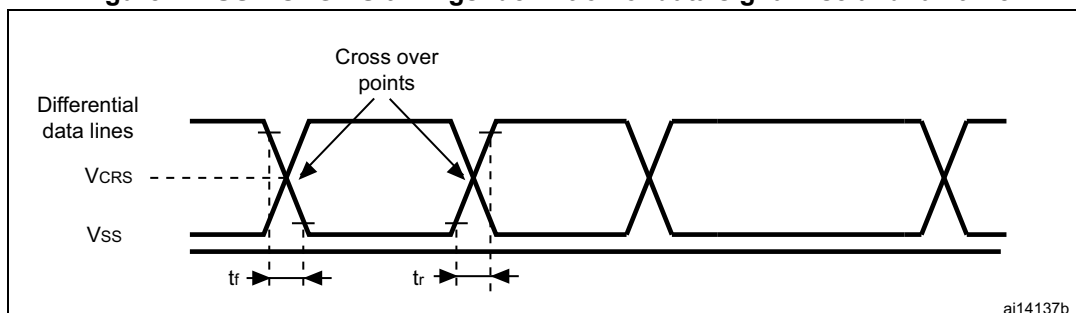


Figure 44. USB OTG FS timings: definition of data signal rise and fall time

Table 59. USB OTG FS electrical characteristics⁽¹⁾

Driver characteristics					
Symbol	Parameter	Conditions	Min	Max	Unit
t_r	Rise time ⁽²⁾	$C_L = 50 \text{ pF}$	4	20	ns
t_f	Fall time ⁽²⁾	$C_L = 50 \text{ pF}$	4	20	ns
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage	-	1.3	2.0	V

1. Guaranteed by design.

2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

USB HS characteristics

Unless otherwise specified, the parameters given in [Table 62](#) for ULPI are derived from tests performed under the ambient temperature, f_{HCLK} frequency summarized in [Table 61](#) and V_{DD} supply voltage conditions summarized in [Table 60](#), with the following configuration:

- Output speed is set to $OSPEEDR[1:0] = 10$
- Capacitive load $C = 30 \text{ pF}$
- Measurement points are done at CMOS levels: $0.5V_{DD}$.

Refer to [Section 5.3.16: I/O port characteristics](#) for more details on the input/output characteristics.

Table 60. USB HS DC electrical characteristics

Symbol	Parameter	Min. ⁽¹⁾	Max. ⁽¹⁾	Unit
Input level	V_{DD} USB OTG HS operating voltage	2.7	3.6	V

1. All the voltages are measured from the local ground potential.

Table 61. USB HS clock timing parameters⁽¹⁾

Parameter	Symbol	Min	Nominal	Max	Unit
f_{HCLK} value to guarantee proper operation of USB HS interface	-	30	-	-	MHz
Frequency (first transition)	8-bit $\pm 10\%$ F_{START_8BIT}	54	60	66	MHz

Table 66. Dynamic characteristics: Ethernet MAC signals for MII⁽¹⁾

Symbol	Parameter	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	9		-	ns
$t_{ih(RXD)}$	Receive data hold time	10		-	
$t_{su(DV)}$	Data valid setup time	9		-	
$t_{ih(DV)}$	Data valid hold time	8		-	
$t_{su(ER)}$	Error setup time	6		-	
$t_{ih(ER)}$	Error hold time	8		-	
$t_d(TXEN)$	Transmit enable valid delay time	0	10	14	
$t_d(TXD)$	Transmit data valid delay time	0	10	15	

1. Guaranteed by characterization.

5.3.20 CAN (controller area network) interface

Refer to [Section 5.3.16: I/O port characteristics](#) for more details on the input/output alternate function characteristics (CANTX and CANRX).

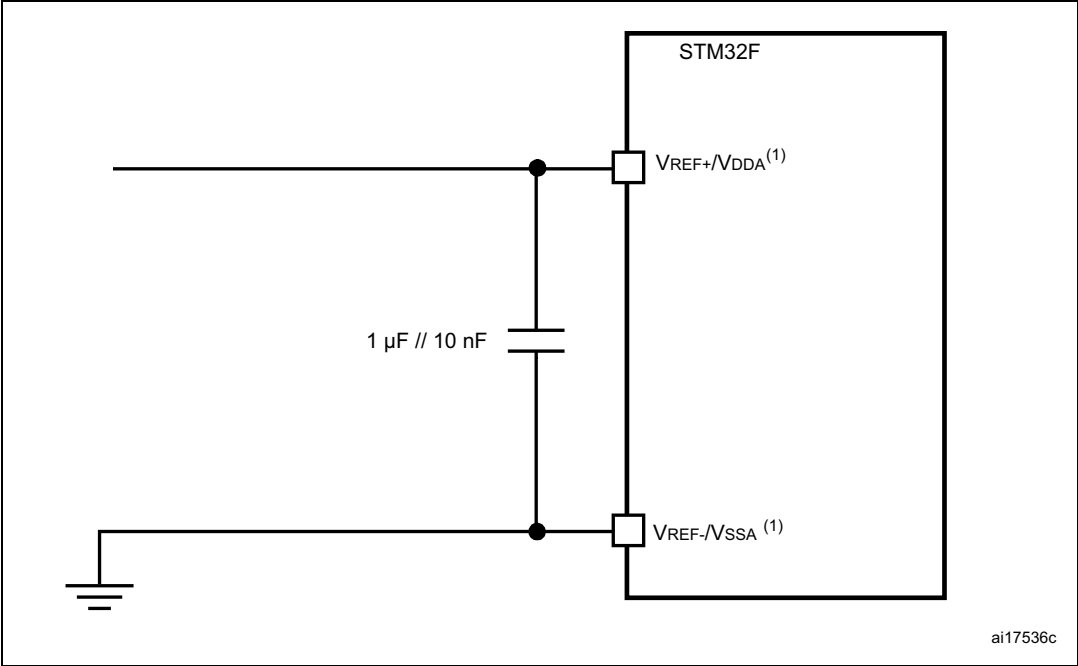
5.3.21 12-bit ADC characteristics

Unless otherwise specified, the parameters given in [Table 67](#) are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in [Table 14](#).

Table 67. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	1.8 ⁽¹⁾	-	3.6	V
V_{REF+}	Positive reference voltage	-	1.8 ⁽¹⁾⁽²⁾⁽³⁾	-	V_{DDA}	
V_{REF-}	Negative reference voltage	-	-	0	-	
f_{ADC}	ADC clock frequency	$V_{DDA} = 1.8^{(1)(3)}$ to 2.4 V	0.6	15	18	MHz
		$V_{DDA} = 2.4$ to 3.6 V ⁽³⁾	0.6	30	36	MHz
$f_{TRIG}^{(4)}$	External trigger frequency	$f_{ADC} = 30$ MHz, 12-bit resolution	-	-	1764	kHz
		-	-	-	17	1/ f_{ADC}
V_{AIN}	Conversion voltage range ⁽⁵⁾	-	0 (V_{SSA} or V_{REF-} tied to ground)	-	V_{REF+}	V
$R_{AIN}^{(4)}$	External input impedance	See Equation 1 for details	-	-	50	k Ω
$R_{ADC}^{(4)(6)}$	Sampling switch resistance	-	-	-	6	k Ω
$C_{ADC}^{(4)}$	Internal sample and hold capacitor	-	-	4	-	pF

Figure 52. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are both available on UFBGA176. V_{REF+} is also available on LQFP100, LQFP144, and LQFP176. When V_{REF+} and V_{REF-} are not available, they are internally connected to V_{DDA} and V_{SSA} .

5.3.22 Temperature sensor characteristics

Table 69. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$T_L^{(1)}$	V_{SENSE} linearity with temperature	-	± 1	± 2	$^{\circ}\text{C}$
Avg_Slope ⁽¹⁾	Average slope	-	2.5		mV/ $^{\circ}\text{C}$
$V_{25}^{(1)}$	Voltage at 25 $^{\circ}\text{C}$	-	0.76		V
$t_{START}^{(2)}$	Startup time	-	6	10	μs
$T_{S_temp}^{(2)}$	ADC sampling time when reading the temperature (1 $^{\circ}\text{C}$ accuracy)	10	-	-	μs

1. Guaranteed by characterization.

2. Guaranteed by design.

Table 70. Temperature sensor calibration values

Symbol	Parameter	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 $^{\circ}\text{C}$, $V_{DDA}=3.3\text{ V}$	0x1FFF 7A2C - 0x1FFF 7A2D
TS_CAL2	TS ADC raw data acquired at temperature of 110 $^{\circ}\text{C}$, $V_{DDA}=3.3\text{ V}$	0x1FFF 7A2E - 0x1FFF 7A2F

Table 74. DAC characteristics (continued)

Symbol	Parameter	Min	Typ	Max	Unit	Comments
$R_{LOAD}^{(2)}$	Resistive load with buffer ON	5	-	-	k Ω	
$R_O^{(2)}$	Impedance output with buffer OFF	-	-	15	k Ω	When the buffer is OFF, the Minimum resistive load between DAC_OUT and V_{SS} to have a 1% accuracy is 1.5 M Ω
$C_{LOAD}^{(2)}$	Capacitive load	-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
DAC_OUT min ⁽²⁾	Lower DAC_OUT voltage with buffer ON	0.2	-	-	V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at $V_{REF+} = 3.6$ V and (0x1C7) to (0xE38) at $V_{REF+} = 1.8$ V
DAC_OUT max ⁽²⁾	Higher DAC_OUT voltage with buffer ON	-	-	$V_{DDA} - 0.2$	V	
DAC_OUT min ⁽²⁾	Lower DAC_OUT voltage with buffer OFF	-	0.5	-	mV	It gives the maximum output excursion of the DAC.
DAC_OUT max ⁽²⁾	Higher DAC_OUT voltage with buffer OFF	-	-	$V_{REF+} - 1LSB$	V	
$I_{VREF+}^{(4)}$	DAC DC V_{REF} current consumption in quiescent mode (Standby mode)	-	170	240	μA	With no load, worst code (0x800) at $V_{REF+} = 3.6$ V in terms of DC consumption on the inputs
		-	50	75		With no load, worst code (0xF1C) at $V_{REF+} = 3.6$ V in terms of DC consumption on the inputs
$I_{DDA}^{(4)}$	DAC DC V_{DDA} current consumption in quiescent mode ⁽³⁾	-	280	380	μA	With no load, middle code (0x800) on the inputs
		-	475	625	μA	With no load, worst code (0xF1C) at $V_{REF+} = 3.6$ V in terms of DC consumption on the inputs
DNL ⁽⁴⁾	Differential non linearity Difference between two consecutive code-1LSB)	-	-	± 0.5	LSB	Given for the DAC in 10-bit configuration.
		-	-	± 2	LSB	Given for the DAC in 12-bit configuration.
INL ⁽⁴⁾	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)	-	-	± 1	LSB	Given for the DAC in 10-bit configuration.
		-	-	± 4	LSB	Given for the DAC in 12-bit configuration.

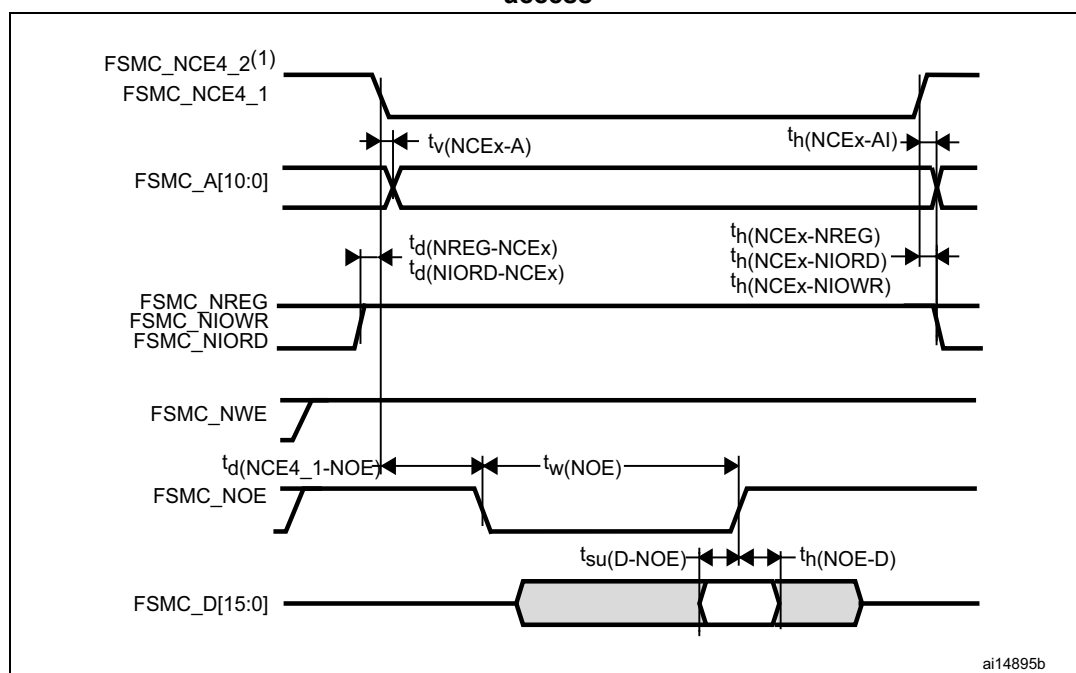
PC Card/CompactFlash controller waveforms and timings

Figure 62 through Figure 67 represent synchronous waveforms, and Table 83 and Table 84 provide the corresponding timings. The results shown in this table are obtained with the following FSMC configuration:

- COM.FSMC_SetupTime = 0x04;
- COM.FSMC_WaitSetupTime = 0x07;
- COM.FSMC_HoldSetupTime = 0x04;
- COM.FSMC_HiZSetupTime = 0x00;
- ATT.FSMC_SetupTime = 0x04;
- ATT.FSMC_WaitSetupTime = 0x07;
- ATT.FSMC_HoldSetupTime = 0x04;
- ATT.FSMC_HiZSetupTime = 0x00;
- IO.FSMC_SetupTime = 0x04;
- IO.FSMC_WaitSetupTime = 0x07;
- IO.FSMC_HoldSetupTime = 0x04;
- IO.FSMC_HiZSetupTime = 0x00;
- TCLRSetupTime = 0;
- TARSetupTime = 0.

In all timing tables, the T_{HCLK} is the HCLK clock period.

Figure 62. PC Card/CompactFlash controller waveforms for common memory read access



1. FSMC_NCE4_2 remains high (inactive during 8-bit access).

Table 86. Switching characteristics for NAND Flash write cycles⁽¹⁾

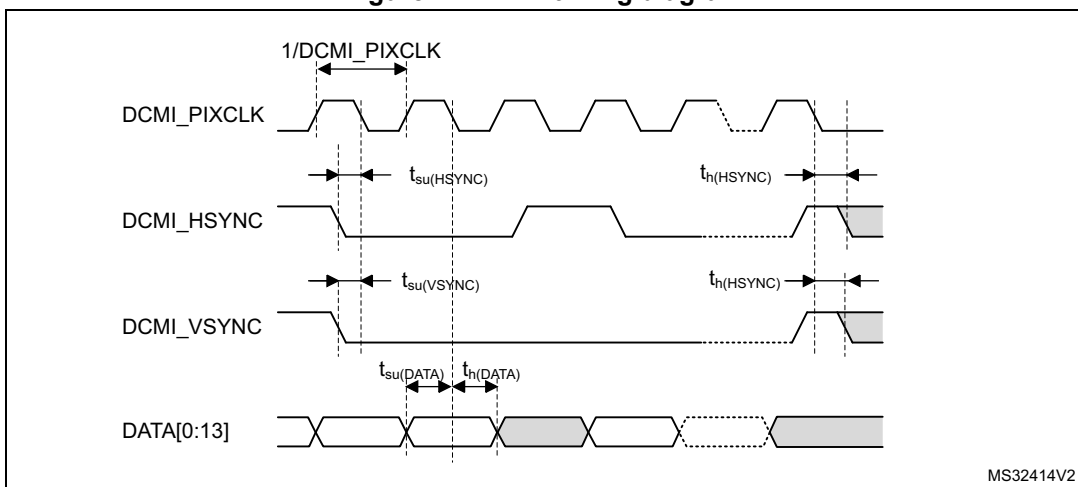
Symbol	Parameter	Min	Max	Unit
$t_{w(NWE)}$	FSMC_NWE low width	$4T_{HCLK}-1$	$4T_{HCLK}+3$	ns
$t_{v(NWE-D)}$	FSMC_NWE low to FSMC_D[15-0] valid	-	0	ns
$t_{h(NWE-D)}$	FSMC_NWE high to FSMC_D[15-0] invalid	$3T_{HCLK}-2$	-	ns
$t_{d(D-NWE)}$	FSMC_D[15-0] valid before FSMC_NWE high	$5T_{HCLK}-3$	-	ns
$t_{d(ALE-NWE)}$	FSMC_ALE valid before FSMC_NWE low	-	$3T_{HCLK}$	ns
$t_{h(NWE-ALE)}$	FSMC_NWE high to FSMC_ALE invalid	$3T_{HCLK}-2$	-	ns

1. $C_L = 30$ pF.

5.3.27 Camera interface (DCMI) timing specifications

Unless otherwise specified, the parameters given in [Table 87](#) for DCMI are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage summarized in [Table 13](#), with the following configuration:

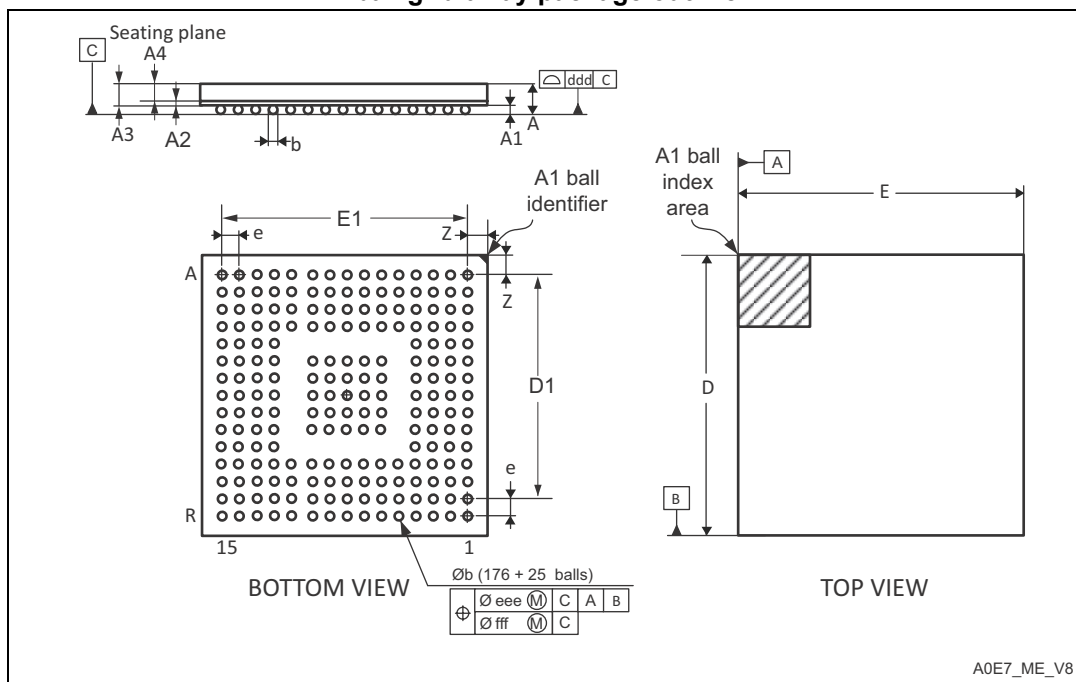
- PCK polarity: falling
- VSYNC and HSYNC polarity: high
- Data format: 14 bits

Figure 72. DCMI timing diagram**Table 87. DCMI characteristics⁽¹⁾**

Symbol	Parameter	Min	Max	Unit
	Frequency ratio DCMI_PIXCLK/ f_{HCLK}	-	0.4	
DCMI_PIXCLK	Pixel clock input	-	54	MHz
D_{pixel}	Pixel clock input duty cycle	30	70	%

6.5 UFBGA176+25 package information

Figure 87. UFBGA176+25 ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 95. UFBGA176+25 ball, 10 × 10 × 0.65 mm pitch, ultra thin fine pitch ball grid array mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.130	-	-	0.0051	-
A3	-	0.450	-	-	0.0177	-
A4	-	0.320	-	-	0.0126	-
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	9.850	10.000	10.150	0.3878	0.3937	0.3996
D1	-	9.100	-	-	0.3583	-
E	9.850	10.000	10.150	0.3878	0.3937	0.3996
E1	-	9.100	-	-	0.3583	-
e	-	0.650	-	-	0.0256	-
Z	-	0.450	-	-	0.0177	-
ddd	-	-	0.080	-	-	0.0031

Table 100. Document revision history (continued)

Date	Revision	Changes
22-Oct-2015	6	In the whole document, updated notes related to values guaranteed by design or by characterization. Updated Table 34: HSI oscillator characteristics. Changed f_{VCO_OUT} minimum value and VCO freq to 100 MHz in Table 36: Main PLL characteristics and Table 37: PLLI2S (audio PLL) characteristics. Updated Figure 39: SPI timing diagram - slave mode and CPHA = 0. Updated Figure 53: 12-bit buffered /non-buffered DAC. Removed note 1 related to better performance using a restricted V_{DD} range in Table 68: ADC accuracy at $f_{ADC} = 30$ MHz. Updated Figure 84: LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package outline. Updated Figure 87: UFBGA176+25 ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package outline and Table 95: UFBGA176+25 ball, 10 x 10 x 0.65 mm pitch, ultra thin fine pitch ball grid array mechanical data.
16-Mar-2016	7	Updated Figure 2: Compatible board design STM32F10xx/STM32F2/STM32F40xxx for LQFP100 package. Updated $V_{SSX}-V_{SS}$ in Table 11: Voltage characteristics to add V_{REF_A}. Added V_{REF_in} in Table 67: ADC characteristics. Updated Table 90: WLCSP90 - 4.223 x 3.969 mm, 0.400 mm pitch wafer level chip scale package mechanical data.
09-Sep-2016	8	Remove note 1 below Figure 5: STM32F40xxx block diagram. Updated definition of stresses above maximum ratings in Section 5.2: Absolute maximum ratings. Updated $t_{h(NSS)}$ in Figure 39: SPI timing diagram - slave mode and CPHA = 0 and Figure 40: SPI timing diagram - slave mode and CPHA = 1. Added note related to optional marking and inset/upset marks in all package marking sections. Updated Figure 87: UFBGA176+25 ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package outline and Table 95: UFBGA176+25 ball, 10 x 10 x 0.65 mm pitch, ultra thin fine pitch ball grid array mechanical data.