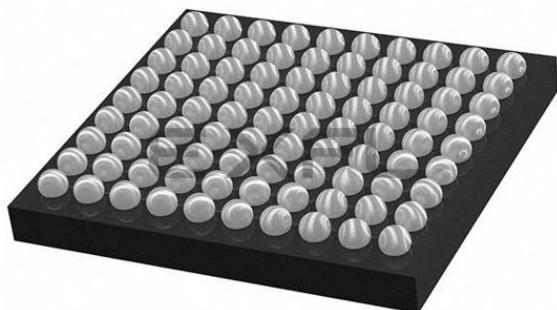




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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	168MHz
Connectivity	CANbus, EBI/EMI, I ² C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LCD, POR, PWM, WDT
Number of I/O	72
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 13x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	90-UFBGA, WLCSP
Supplier Device Package	90-WLCSP (4.22x3.97)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f405ogy6tr

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2.2.1 ARM® Cortex®-M4 core with FPU and embedded Flash and SRAM

The ARM Cortex-M4 processor with FPU is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM Cortex-M4 32-bit RISC processor with FPU features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU (floating point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

The STM32F405xx and STM32F407xx family is compatible with all ARM tools and software.

[Figure 5](#) shows the general block diagram of the STM32F40xxx family.

Note: Cortex-M4 with FPU is binary compatible with Cortex-M3.

2.2.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard ARM® Cortex®-M4 with FPU processors. It balances the inherent performance advantage of the ARM Cortex-M4 with FPU over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor full 210 DMIPS performance at this frequency, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 128-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 168 MHz.

2.2.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

2.2.4 Embedded Flash memory

The STM32F40xxx devices embed a Flash memory of 512 Kbytes or 1 Mbytes available for storing programs and data.

2.2.5 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a software signature during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

2.2.6 Embedded SRAM

All STM32F40xxx products embed:

- Up to 192 Kbytes of system SRAM including 64 Kbytes of CCM (core coupled memory) data RAM
RAM memory is accessed (read/write) at CPU clock speed with 0 wait states.
- 4 Kbytes of backup SRAM
This area is accessible only from the CPU. Its content is protected against possible unwanted write accesses, and is retained in Standby or VBAT mode.

2.2.7 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs, Ethernet, USB HS) and the slaves (Flash memory, RAM, FSMC, AHB and APB peripherals) and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

Eight DAC trigger inputs are used in the device. The DAC channels are triggered through the timer update outputs that are also connected to different DMA streams.

2.2.38 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using 2 pins only instead of 5 required by the JTAG (JTAG pins could be re-use as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

2.2.39 Embedded Trace Macrocell™

The ARM Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F40xxx through a small number of ETM pins to an external hardware trace port analyser (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell operates with third party debugger software tools.

Table 8. FSMC pin definition (continued)

Pins ⁽¹⁾	FSMC				LQFP100 ⁽²⁾	WLCSP90 ⁽²⁾
	CF	NOR/PSRAM/ SRAM	NOR/PSRAM Mux	NAND 16 bit		
PG2	-	A12	-	-	-	-
PG3	-	A13	-	-	-	-
PG4	-	A14	-	-	-	-
PG5	-	A15	-	-	-	-
PG6	-	-	-	INT2	-	-
PG7	-	-	-	INT3	-	-
PD0	D2	D2	DA2	D2	Yes	Yes
PD1	D3	D3	DA3	D3	Yes	Yes
PD3	-	CLK	CLK	-	Yes	-
PD4	NOE	NOE	NOE	NOE	Yes	Yes
PD5	NWE	NWE	NWE	NWE	Yes	Yes
PD6	NWAIT	NWAIT	NWAIT	NWAIT	Yes	Yes
PD7	-	NE1	NE1	NCE2	Yes	Yes
PG9	-	NE2	NE2	NCE3	-	-
PG10	NCE4_1	NE3	NE3	-	-	-
PG11	NCE4_2	-	-	-	-	-
PG12	-	NE4	NE4	-	-	-
PG13	-	A24	A24	-	-	-
PG14	-	A25	A25	-	-	-
PB7	-	NADV	NADV	-	Yes	Yes
PE0	-	NBL0	NBL0	-	Yes	-
PE1	-	NBL1	NBL1	-	Yes	-

1. Full FSMC features are available on LQFP144, LQFP176, and UFBGA176. The features available on smaller packages are given in the dedicated package column.

2. Ports F and G are not available in devices delivered in 100-pin packages.

Table 9. Alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/SPI2/I2S2/I2S2ext	SPI3/I2Sext/I2S3	USART1/2/3/I2S3ext	UART4/5/USART6	CAN1/2/TIM12/13/14	OTG_FS/OTG_HS	ETH	FSMC/SDIO/OTG_FS	DCMI		
Port D	PD0	-	-	-	-	-	-	-	-	-	CAN1_RX	-	-	FSMC_D2	-	-	EVENTOUT
	PD1	-	-	-	-	-	-	-	-	-	CAN1_TX	-	-	FSMC_D3	-	-	EVENTOUT
	PD2	-	-	TIM3_ETR	-	-	-	-	-	UART5_RX	-	-	-	SDIO_CMD	DCMI_D11	-	EVENTOUT
	PD3	-	-	-	-	-	-	-	USART2_CTS	-	-	-	-	FSMC_CLK	-	-	EVENTOUT
	PD4	-	-	-	-	-	-	-	USART2_RTS	-	-	-	-	FSMC_NOE	-	-	EVENTOUT
	PD5	-	-	-	-	-	-	-	USART2_TX	-	-	-	-	FSMC_NWE	-	-	EVENTOUT
	PD6	-	-	-	-	-	-	-	USART2_RX	-	-	-	-	FSMC_NWAIT	-	-	EVENTOUT
	PD7	-	-	-	-	-	-	-	USART2_CK	-	-	-	-	FSMC_NE1/FSMC_NCE2	-	-	EVENTOUT
	PD8	-	-	-	-	-	-	-	USART3_TX	-	-	-	-	FSMC_D13	-	-	EVENTOUT
	PD9	-	-	-	-	-	-	-	USART3_RX	-	-	-	-	FSMC_D14	-	-	EVENTOUT
	PD10	-	-	-	-	-	-	-	USART3_CK	-	-	-	-	FSMC_D15	-	-	EVENTOUT
	PD11	-	-	-	-	-	-	-	USART3_CTS	-	-	-	-	FSMC_A16	-	-	EVENTOUT
	PD12	-	-	TIM4_CH1	-	-	-	-	USART3_RTS	-	-	-	-	FSMC_A17	-	-	EVENTOUT
	PD13	-	-	TIM4_CH2	-	-	-	-	-	-	-	-	-	FSMC_A18	-	-	EVENTOUT
	PD14	-	-	TIM4_CH3	-	-	-	-	-	-	-	-	-	FSMC_D0	-	-	EVENTOUT
	PD15	-	-	TIM4_CH4	-	-	-	-	-	-	-	-	-	FSMC_D1	-	-	EVENTOUT

Figure 24. Typical current consumption versus temperature, Run mode, code with data processing running from Flash (ART accelerator ON) or RAM, and peripherals OFF

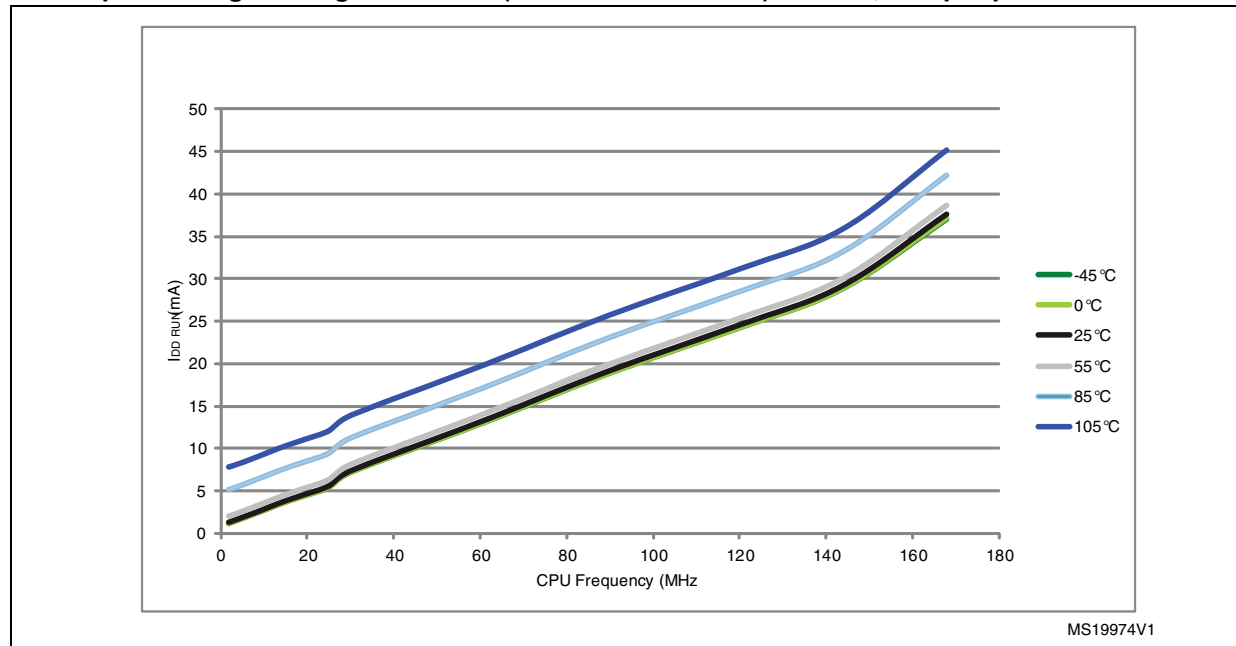


Figure 25. Typical current consumption versus temperature, Run mode, code with data processing running from Flash (ART accelerator ON) or RAM, and peripherals ON

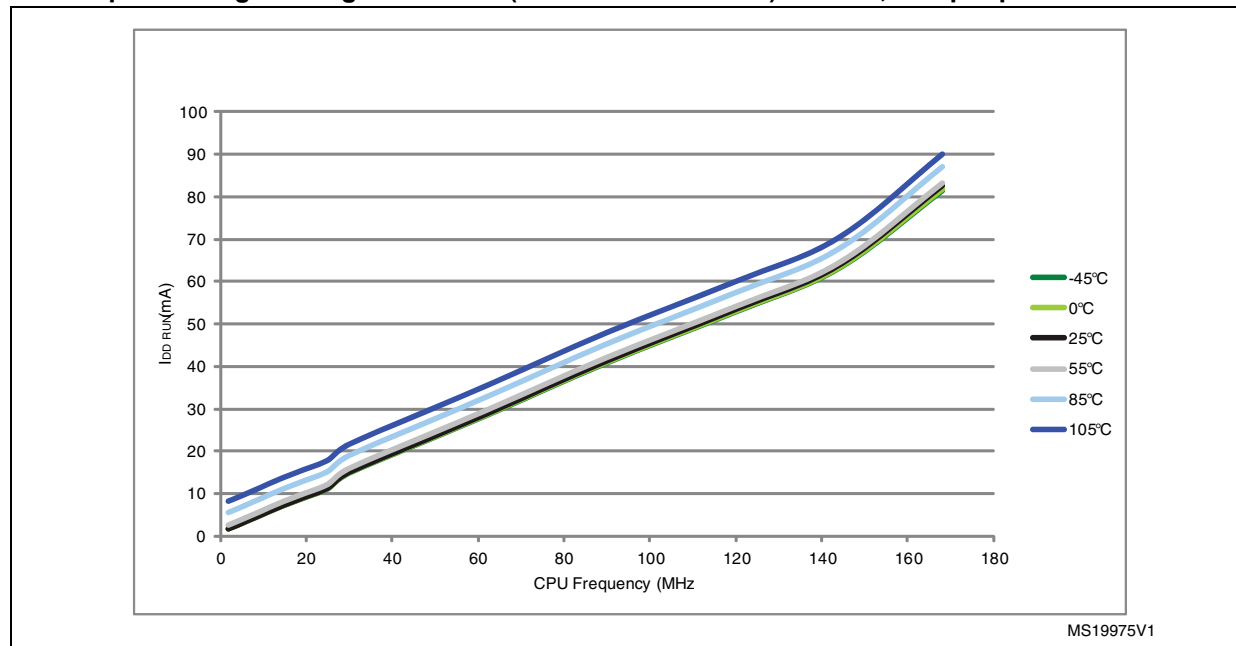
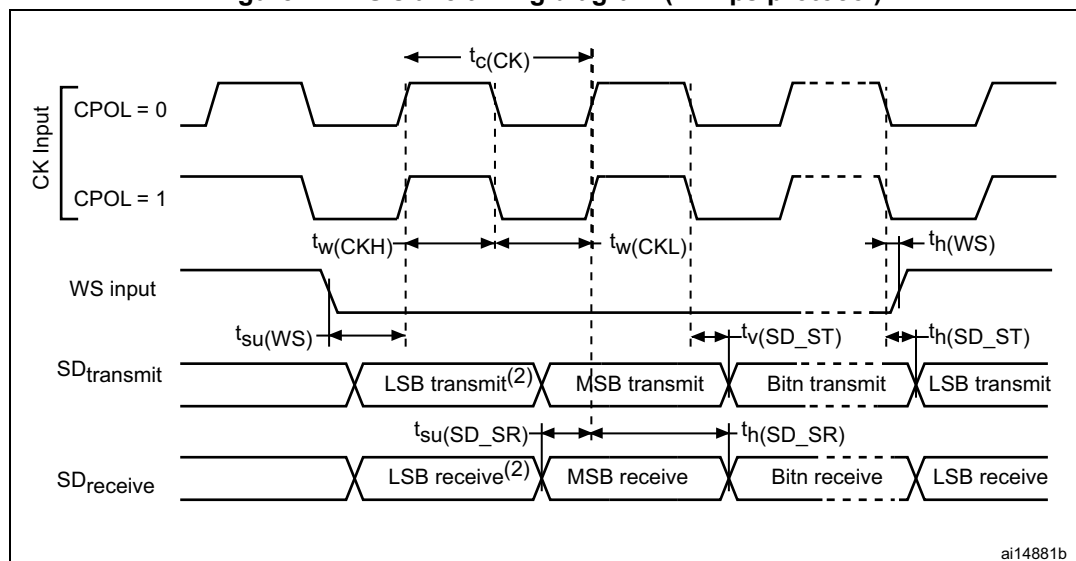
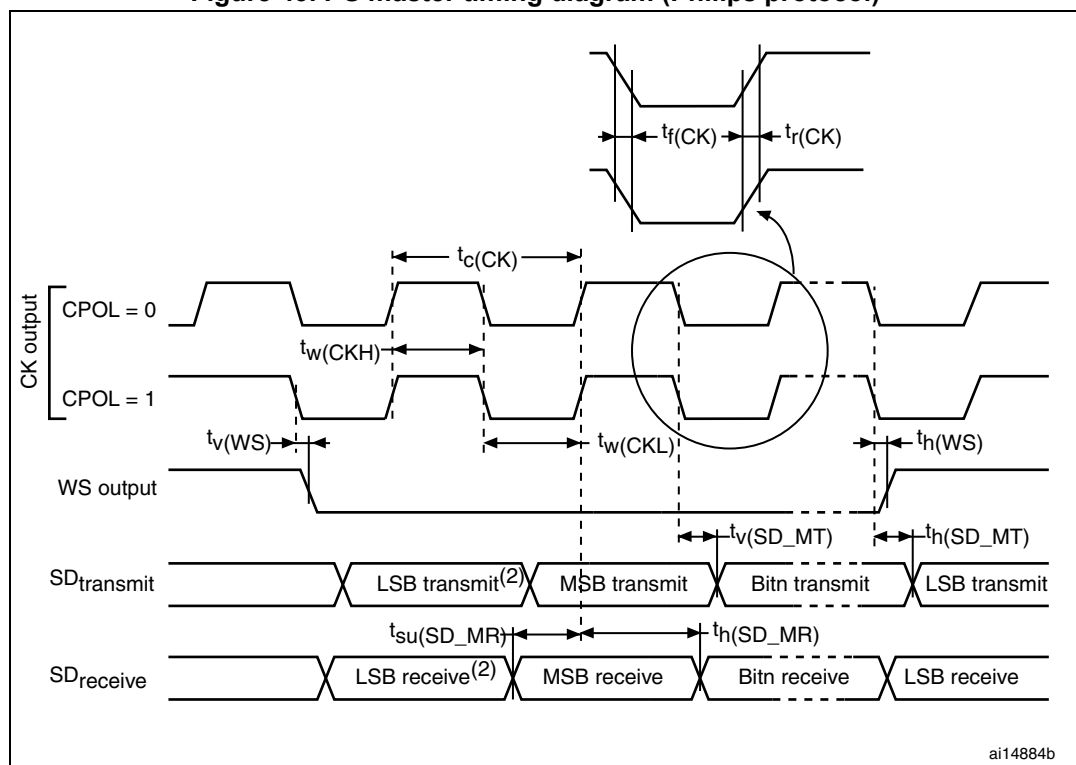


Figure 42. I²S slave timing diagram (Philips protocol)

1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 43. I²S master timing diagram (Philips protocol)⁽¹⁾

1. Guaranteed by characterization.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

USB OTG FS characteristics

This interface is present in both the USB OTG HS and USB OTG FS controllers.

Table 57. USB OTG FS startup time

Symbol	Parameter	Max	Unit
$t_{\text{STARTUP}}^{(1)}$	USB OTG FS transceiver startup time	1	μs

1. Guaranteed by design.

Table 58. USB OTG FS DC electrical characteristics

Symbol		Parameter	Conditions	Min. ⁽¹⁾	Typ.	Max. ⁽¹⁾	Unit
Input levels	V _{DD}	USB OTG FS operating voltage	-	3.0 ⁽²⁾	-	3.6	V
	V _{DI} ⁽³⁾	Differential input sensitivity	I(USB_FS_DP/DM, USB_HS_DP/DM)	0.2	-	-	V
	V _{CM} ⁽³⁾	Differential common mode range	Includes V _{DI} range	0.8	-	2.5	
	V _{SE} ⁽³⁾	Single ended receiver threshold	-	1.3	-	2.0	
Output levels	V _{OL}	Static output level low	R _L of 1.5 kΩ to 3.6 V ⁽⁴⁾	-	-	0.3	V
	V _{OH}	Static output level high	R _L of 15 kΩ to V _{SS} ⁽⁴⁾	2.8	-	3.6	
R _{PD}		PA11, PA12, PB14, PB15 (USB_FS_DP/DM, USB_HS_DP/DM)	V _{IN} = V _{DD}	17	21	24	kΩ
		PA9, PB13 (OTG_FS_VBUS, OTG_HS_VBUS)		0.65	1.1	2.0	
R _{PU}		PA12, PB15 (USB_FS_DP, USB_HS_DP)	V _{IN} = V _{SS}	1.5	1.8	2.1	
		PA9, PB13 (OTG_FS_VBUS, OTG_HS_VBUS)	V _{IN} = V _{SS}	0.25	0.37	0.55	

1. All the voltages are measured from the local ground potential.
2. The STM32F405xx and STM32F407xx USB OTG FS functionality is ensured down to 2.7 V but not the full USB OTG FS electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
3. Guaranteed by design.
4. R_{L} is the load connected on the USB OTG FS drivers

Table 61. USB HS clock timing parameters⁽¹⁾

Parameter		Symbol	Min	Nominal	Max	Unit
Frequency (steady state) ± 500 ppm		F_{STEADY}	59.97	60	60.03	MHz
Duty cycle (first transition)	8-bit $\pm 10\%$	$D_{\text{START_8BIT}}$	40	50	60	%
Duty cycle (steady state) ± 500 ppm		D_{STEADY}	49.975	50	50.025	%
Time to reach the steady state frequency and duty cycle after the first transition		T_{STEADY}	-	-	1.4	ms
Clock startup time after the de-assertion of SuspendM	Peripheral	$T_{\text{START_DEV}}$	-	-	5.6	ms
	Host	$T_{\text{START_HOST}}$	-	-	-	
PHY preparation time after the first transition of the input clock		T_{PREP}	-	-	-	μs

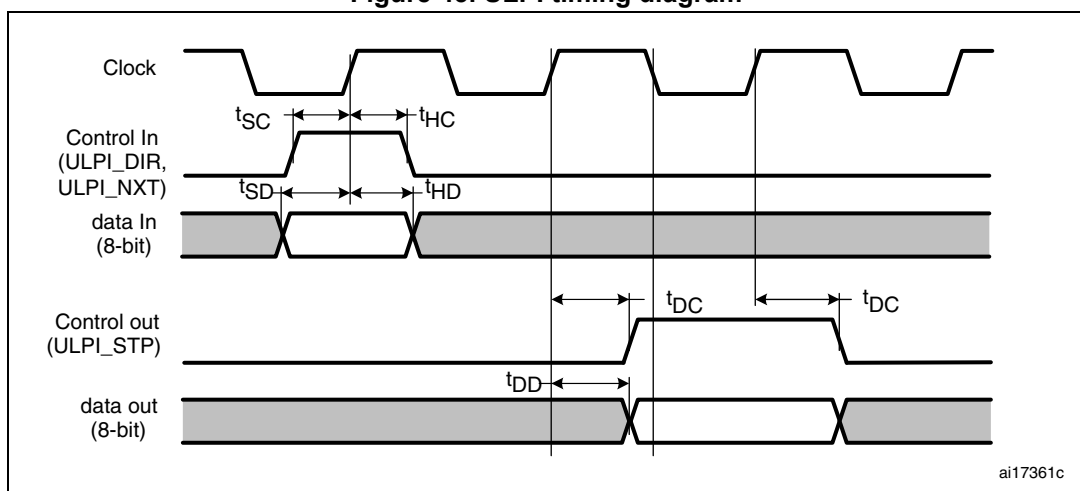
1. Guaranteed by design.

Table 62. ULPI timing

Parameter	Symbol	Value ⁽¹⁾		Unit
		Min.	Max.	
Control in (ULPI_DIR) setup time	t_{SC}	-	2.0	ns
Control in (ULPI_NXT) setup time		-	1.5	
Control in (ULPI_DIR, ULPI_NXT) hold time	t_{HC}	0	-	
Data in setup time	t_{SD}	-	2.0	
Data in hold time	t_{HD}	0	-	
Control out (ULPI_STP) setup time and hold time	t_{DC}	-	9.2	
Data out available from clock rising edge	t_{DD}	-	10.7	

1. $V_{\text{DD}} = 2.7 \text{ V}$ to 3.6 V and $T_{\text{A}} = -40$ to $85 \text{ }^{\circ}\text{C}$.

Figure 45. ULPI timing diagram



Ethernet characteristics

Unless otherwise specified, the parameters given in [Table 64](#), [Table 65](#) and [Table 66](#) for SMI, RMII and MII are derived from tests performed under the ambient temperature, f_{HCLK} frequency summarized in [Table 14](#) and VDD supply voltage conditions summarized in [Table 63](#), with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$.

Refer to [Section 5.3.16: I/O port characteristics](#) for more details on the input/output characteristics.

Table 63. Ethernet DC electrical characteristics

Symbol		Parameter	Min. ⁽¹⁾	Max. ⁽¹⁾	Unit
Input level	V _{DD}	Ethernet operating voltage	2.7	3.6	V

1. All the voltages are measured from the local ground potential.

[Table 64](#) gives the list of Ethernet MAC signals for the SMI (station management interface) and [Figure 46](#) shows the corresponding timing diagram.

Figure 46. Ethernet SMI timing diagram

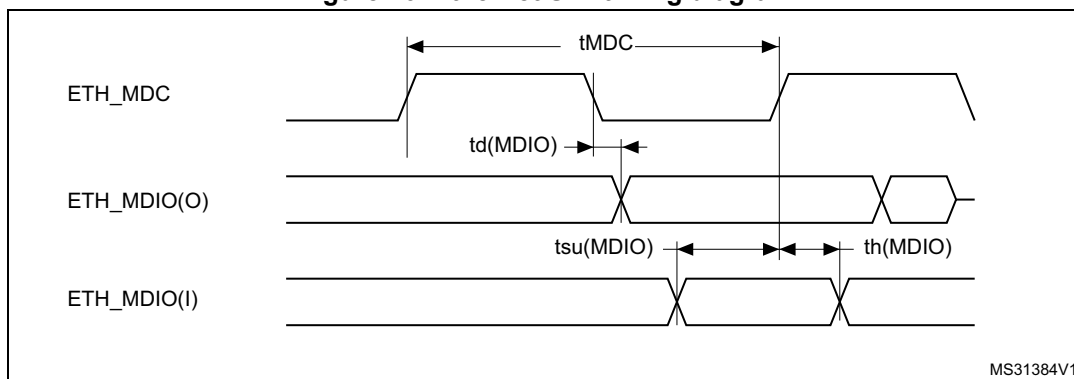


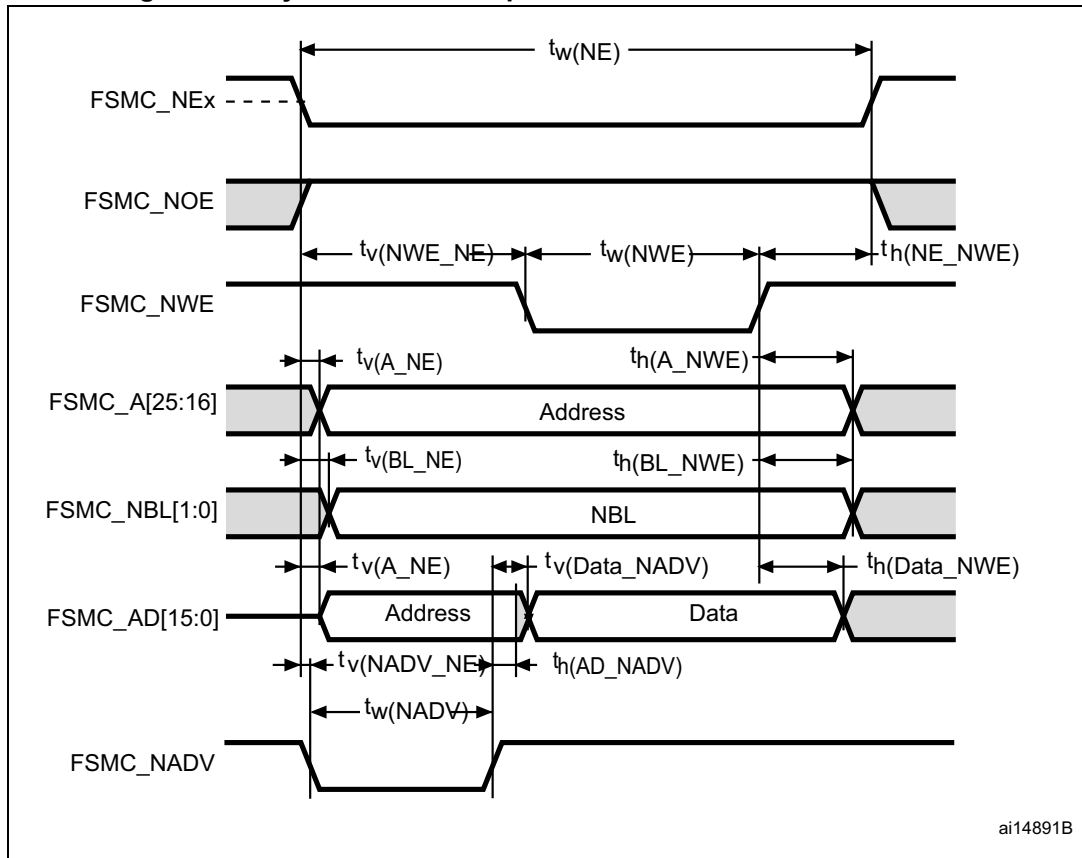
Table 64. Dynamic characteristics: Ethernet MAC signals for SMI⁽¹⁾

Symbol	Parameter	Min	Typ	Max	Unit
t_{MDC}	MDC cycle time(2.38 MHz)	411	420	425	ns
$T_d(MDIO)$	Write data valid time	6	10	13	
$t_{su}(MDIO)$	Read data setup time	12	-	-	
$t_h(MDIO)$	Read data hold time	0	-	-	

1. Guaranteed by characterization.

[Table 65](#) gives the list of Ethernet MAC signals for the RMII and [Figure 47](#) shows the corresponding timing diagram.

Figure 57. Asynchronous multiplexed PSRAM/NOR write waveforms



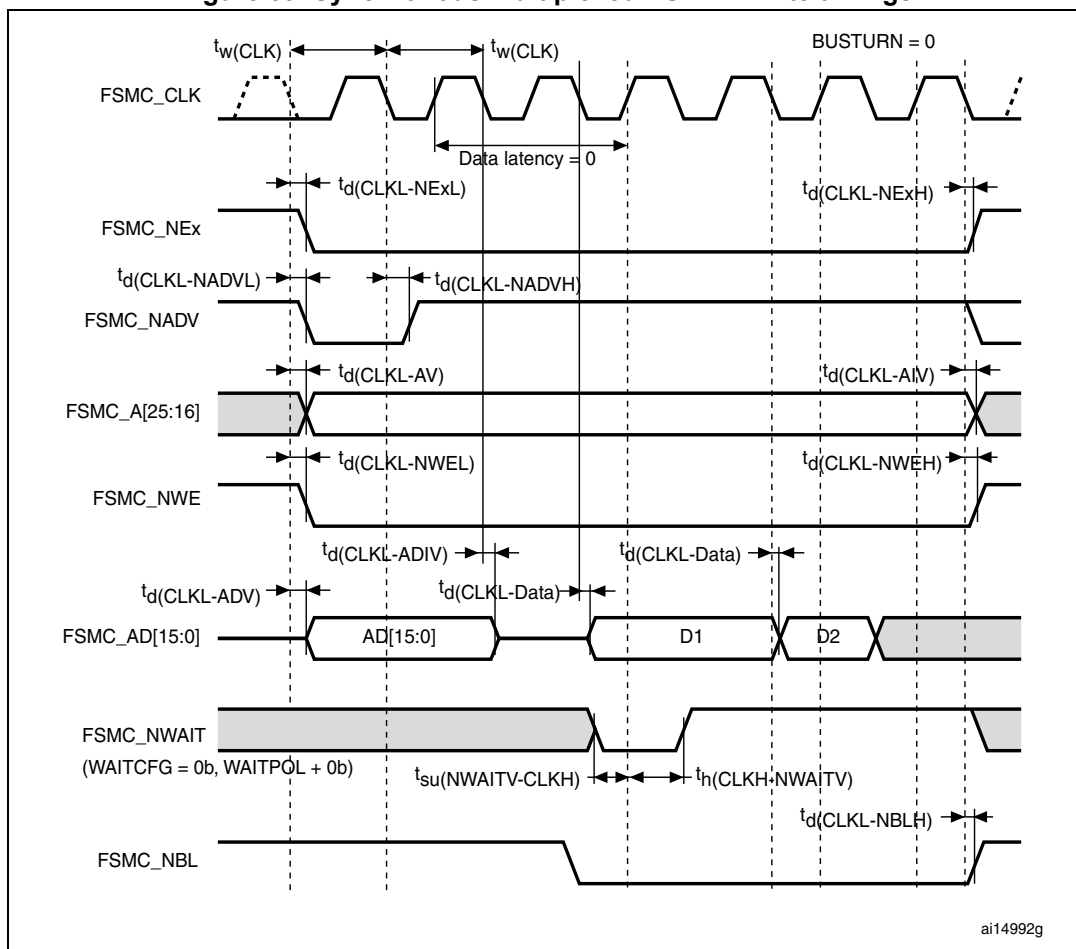
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Table 78. Asynchronous multiplexed PSRAM/NOR write timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NEx low time	$4T_{HCLK}-0.5$	$4T_{HCLK}+3$	ns
$t_{v(NWE_NE)}$	FSMC_NEx low to FSMC_NWE low	$T_{HCLK}-0.5$	$T_{HCLK}-0.5$	ns
$t_{w(NWE)}$	FSMC_NWE low time	$2T_{HCLK}-0.5$	$2T_{HCLK}+3$	ns
$t_{h(NE_NWE)}$	FSMC_NWE high to FSMC_NEx high hold time	T_{HCLK}	-	ns
$t_{v(A_NE)}$	FSMC_NEx low to FSMC_A valid	-	0	ns
$t_{v(NADV_NE)}$	FSMC_NEx low to FSMC_NADV low	1	2	ns
$t_{w(NADV)}$	FSMC_NADV low time	$T_{HCLK}-2$	$T_{HCLK}+1$	ns
$t_{h(AD_NADV)}$	FSMC_AD(address) valid hold time after FSMC_NADV high	$T_{HCLK}-2$	-	ns
$t_{h(A_NWE)}$	Address hold time after FSMC_NWE high	T_{HCLK}	-	ns
$t_{h(BL_NWE)}$	FSMC_BL hold time after FSMC_NWE high	$T_{HCLK}-2$	-	ns
$t_{v(BL_NE)}$	FSMC_NEx low to FSMC_BL valid	-	1.5	ns
$t_{v(Data_NADV)}$	FSMC_NADV high to Data valid	-	$T_{HCLK}-0.5$	ns
$t_{h(Data_NWE)}$	Data hold time after FSMC_NWE high	T_{HCLK}	-	ns

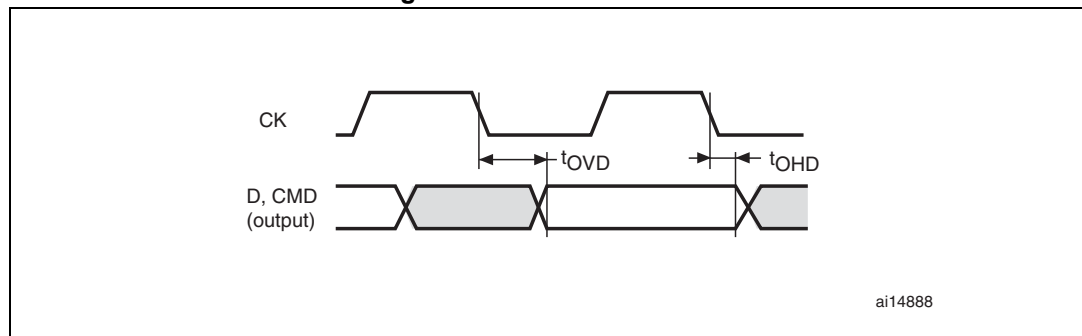
1. $C_L = 30$ pF.

Figure 59. Synchronous multiplexed PSRAM write timings

Table 80. Synchronous multiplexed PSRAM write timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_w(\text{CLK})$	FSMC_CLK period	$2T_{\text{HCLK}}$	-	ns
$t_d(\text{CLKL-NExL})$	FSMC_CLK low to FSMC_NEx low ($x=0..2$)	-	1	ns
$t_d(\text{CLKL-NExH})$	FSMC_CLK low to FSMC_NEx high ($x=0..2$)	1	-	ns
$t_d(\text{CLKL-NADVL})$	FSMC_CLK low to FSMC_NADV low	-	0	ns
$t_d(\text{CLKL-NADVH})$	FSMC_CLK low to FSMC_NADV high	0	-	ns
$t_d(\text{CLKL-AV})$	FSMC_CLK low to FSMC_Ax valid ($x=16..25$)	-	0	ns
$t_d(\text{CLKL-AIV})$	FSMC_CLK low to FSMC_Ax invalid ($x=16..25$)	8	-	ns
$t_d(\text{CLKL-NWEL})$	FSMC_CLK low to FSMC_NWE low	-	0.5	ns
$t_d(\text{CLKL-NWEH})$	FSMC_CLK low to FSMC_NWE high	0	-	ns
$t_d(\text{CLKL-ADIV})$	FSMC_CLK low to FSMC_AD[15:0] invalid	0	-	ns
$t_d(\text{CLKL-DATA})$	FSMC_A/D[15:0] valid data after FSMC_CLK low	-	3	ns

Figure 74. SD default mode

Table 88. Dynamic characteristics: SD / MMC characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f _{PP}	Clock frequency in data transfer mode		0		48	MHz
	SDIO_CK/f _{PCLK2} frequency ratio		-	-	8/3	-
t _{W(CKL)}	Clock low time	f _{PP} = 48 MHz	8.5	9	-	ns
t _{W(CKH)}	Clock high time	f _{PP} = 48 MHz	8.3	10	-	
CMD, D inputs (referenced to CK) in MMC and SD HS mode						
t _{ISU}	Input setup time HS	f _{PP} = 48 MHz	3	-	-	ns
t _{IH}	Input hold time HS	f _{PP} = 48 MHz	0	-	-	
CMD, D outputs (referenced to CK) in MMC and SD HS mode						
t _{OV}	Output valid time HS	f _{PP} = 48 MHz	-	4.5	6	ns
t _{OH}	Output hold time HS	f _{PP} = 48 MHz	1	-	-	
CMD, D inputs (referenced to CK) in SD default mode						
t _{ISUD}	Input setup time SD	f _{PP} = 24 MHz	1.5	-	-	ns
t _{IHD}	Input hold time SD	f _{PP} = 24 MHz	0.5	-	-	
CMD, D outputs (referenced to CK) in SD default mode						
t _{OVD}	Output valid default time SD	f _{PP} = 24 MHz	-	4.5	7	ns
t _{OHD}	Output hold default time SD	f _{PP} = 24 MHz	0.5	-	-	

1. Guaranteed by characterization.

5.3.29 RTC characteristics

Table 89. RTC characteristics

Symbol	Parameter	Conditions	Min	Max
-	f_{PCLK1} /RTCCLK frequency ratio	Any read/write operation from/to an RTC register	4	-

**Table 94. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package
mechanical data**

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.874
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	-	17.500	-	-	0.689	-
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	-	17.500	-	-	0.6890	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

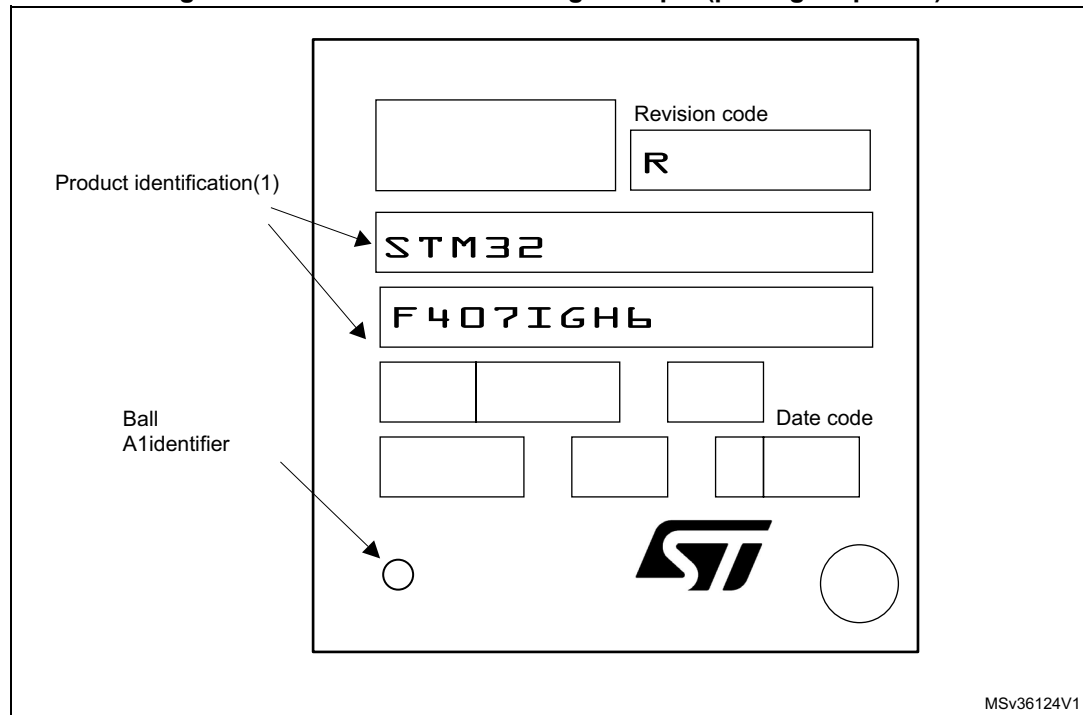
1. Values in inches are converted from mm and rounded to 4 decimal digits.

Device marking for UFBGA176+25

The following figure gives an example of topside marking and ball A 1 position identifier location.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 89. UFBGA176+25 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

6.7 Thermal characteristics

The maximum chip-junction temperature, $T_J \text{ max}$, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- $T_A \text{ max}$ is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- $P_D \text{ max}$ is the sum of $P_{INT} \text{ max}$ and $P_{I/O} \text{ max}$ ($P_D \text{ max} = P_{INT} \text{ max} + P_{I/O} \text{ max}$),
- $P_{INT} \text{ max}$ is the product of I_{DD} and V_{DD} , expressed in Watts. This is the maximum chip internal power.

$P_{I/O} \text{ max}$ represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma (V_{DD} - V_{OH}) \times I_{OH},$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 98. Package thermal characteristics

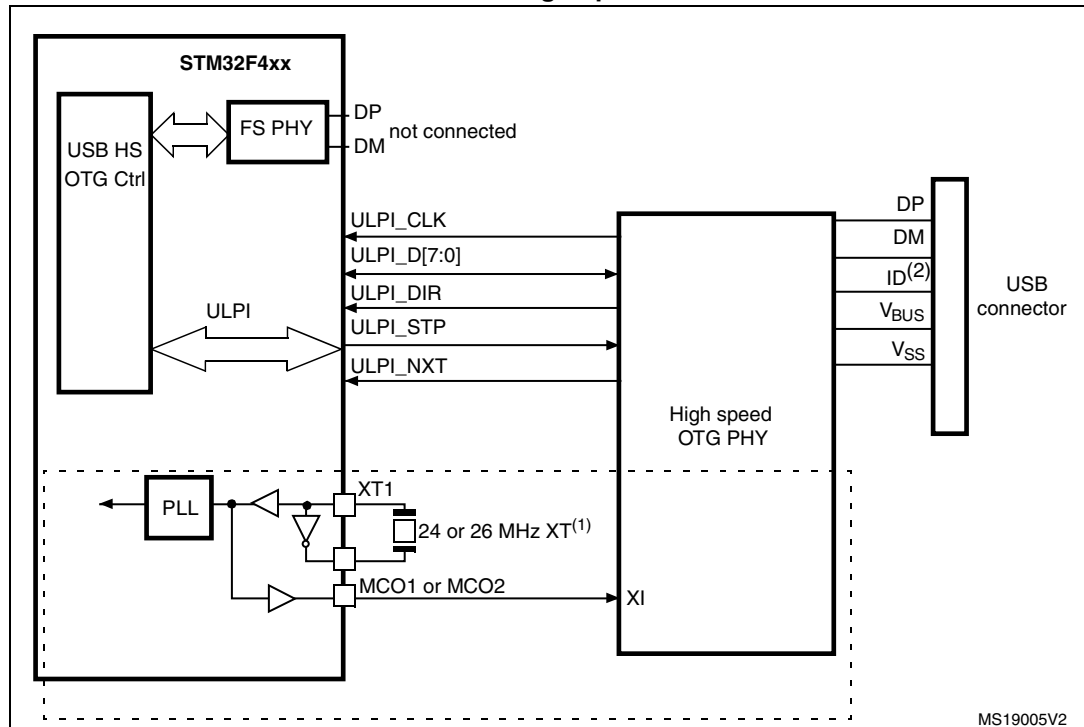
Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP64 - 10 × 10 mm / 0.5 mm pitch	46	°C/W
	Thermal resistance junction-ambient LQFP100 - 14 × 14 mm / 0.5 mm pitch	43	
	Thermal resistance junction-ambient LQFP144 - 20 × 20 mm / 0.5 mm pitch	40	
	Thermal resistance junction-ambient LQFP176 - 24 × 24 mm / 0.5 mm pitch	38	
	Thermal resistance junction-ambient UFBGA176 - 10 × 10 mm / 0.65 mm pitch	39	
	Thermal resistance junction-ambient WLCSP90 - 0.400 mm pitch	38.1	

Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

A.2 USB OTG high speed (HS) interface solutions

Figure 96. USB controller configured as peripheral, host, or dual-mode and used in high speed mode



1. It is possible to use MCO1 or MCO2 to save a crystal. It is however not mandatory to clock the STM32F40xxx with a 24 or 26 MHz crystal when using USB HS. The above figure only shows an example of a possible connection.
2. The ID pin is required in dual role only.

Table 100. Document revision history (continued)

Date	Revision	Changes
24-Jan-2012	2 (continued)	Updated Table 61: USB HS clock timing parameters Updated Table 67: ADC characteristics. Updated Table 68: ADC accuracy at fADC = 30 MHz. Updated Note 1 in Table 74: DAC characteristics. Section 5.3.26: FSMC characteristics: updated Table 75 to Table 86, changed C_L value to 30 pF, and modified FSMC configuration for asynchronous timings and waveforms. Updated Figure 59: Synchronous multiplexed PSRAM write timings. Updated Table 98: Package thermal characteristics. Appendix A.1: USB OTG full speed (FS) interface solutions: modified Figure 93: USB controller configured as peripheral-only and used in Full speed mode added Note 2, updated Figure 94: USB controller configured as host-only and used in full speed mode and added Note 2, changed Figure 95: USB controller configured in dual mode and used in full speed mode and added Note 3. Appendix A.2: USB OTG high speed (HS) interface solutions: removed figures USB OTG HS device-only connection in FS mode and USB OTG HS host-only connection in FS mode, and updated Figure 96: USB controller configured as peripheral, host, or dual-mode and used in high speed mode and added Note 2. Added Appendix A.3: Ethernet interface solutions.