# STMicroelectronics - STM32F405OGY6VTR Datasheet

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| **Details** | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 168MHz |
| Connectivity | CANbus, EBI/EMI, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT |
| Number of I/O | 72 |
| Program Memory Size | 1MB (1M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 192K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 13x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 90-UFBGA, WLCSP |
| Supplier Device Package | 90-WLCSP (4.22x3.97) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f405ogy6vtr |

# 2 Description

The STM32F405xx and STM32F407xx family is based on the high-performance ARM® Cortex®-M4 32-bit RISC core operating at a frequency of up to 168 MHz. The Cortex-M4 core features a Floating point unit (FPU) single precision which supports all ARM single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The STM32F405xx and STM32F407xx family incorporates high-speed embedded memories (Flash memory up to 1 Mbyte, up to 192 Kbytes of SRAM), up to 4 Kbytes of backup SRAM, and an extensive range of enhanced I/Os and peripherals connected to two APB buses, three AHB buses and a 32-bit multi-AHB bus matrix.

All devices offer three 12-bit ADCs, two DACs, a low-power RTC, twelve general-purpose 16-bit timers including two PWM timers for motor control, two general-purpose 32-bit timers. a true random number generator (RNG). They also feature standard and advanced communication interfaces.

- Up to three I$^2$Cs
- Three SPIs, two I$^2$Ss full duplex. To achieve audio class accuracy, the I2S peripherals can be clocked via a dedicated internal audio PLL or via an external clock to allow synchronization.
- Four USARTs plus two UARTs
- An USB OTG full-speed and a USB OTG high-speed with full-speed capability (with the ULPI),
- Two CANs
- An SDIO/MMC interface
- Ethernet and the camera interface available on STM32F407xx devices only.

New advanced peripherals include an SDIO, an enhanced flexible static memory control (FSMC) interface (for devices offered in packages of 100 pins and more), a camera interface for CMOS sensors. Refer to *Table 2: STM32F405xx and STM32F407xx: features and peripheral counts* for the list of peripherals available on each part number.

The STM32F405xx and STM32F407xx family operates in the –40 to +105 °C temperature range from a 1.8 to 3.6 V power supply. The supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range using an external power supply supervisor: refer to *Section : Internal reset OFF*. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F405xx and STM32F407xx family offers devices in various packages ranging from 64 pins to 176 pins. The set of included peripherals changes with the device chosen.

These features make the STM32F405xx and STM32F407xx microcontroller family suitable for a wide range of applications:

- Motor drive and application control
- Medical equipment
- Industrial applications: PLC, inverters, circuit breakers
- Printers, and scanners
- Alarm systems, video intercom, and HVAC
- Home audio appliances

clock entry is available when necessary (for example if an indirectly used external oscillator fails).

Several prescalers allow the configuration of the three AHB buses, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the three AHB buses is 168 MHz while the maximum frequency of the high-speed APB domains is 84 MHz. The maximum allowed frequency of the low-speed APB domain is 42 MHz.

The devices embed a dedicated PLL (PLLI2S) which allows to achieve audio class performance. In this case, the $I^2S$ master clock can generate all standard sampling frequencies from 8 kHz to 192 kHz.

## 2.2.13 Boot modes

At startup, boot pins are used to select one out of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART1 (PA9/PA10), USART3 (PC10/PC11 or PB10/PB11), CAN2 (PB5/PB13), USB OTG FS in Device mode (PA11/PA12) through DFU (device firmware upgrade).

## 2.2.14 Power supply schemes

- $V_{DD}$ = 1.8 to 3.6 V: external power supply for I/Os and the internal regulator (when enabled), provided externally through $V_{DD}$ pins.
- $V_{SSA}$, $V_{DDA}$ = 1.8 to 3.6 V: external analog power supplies for ADC, DAC, Reset blocks, RCs and PLL. $V_{DDA}$ and $V_{SSA}$ must be connected to $V_{DD}$ and $V_{SS}$, respectively.
- $V_{BAT}$ = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when $V_{DD}$ is not present.

Refer to *Figure 21: Power supply scheme* for more details.

*Note:* *$V_{DD}/V_{DDA}$ minimum value of 1.7 V is obtained when the device operates in reduced temperature range, and with the use of an external power supply supervisor (refer to Section : Internal reset OFF).*

*Refer to Table 2 in order to identify the packages supporting this option.*

## 2.2.15 Power supply supervisor

### Internal reset ON

On packages embedding the PDR_ON pin, the power supply supervisor is enabled by holding PDR_ON high. On all other packages, the power supply supervisor is always enabled.

The device has an integrated power-on reset (POR) / power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry. At power-on, POR/PDR is always active and ensures proper operation starting from 1.8 V. After the 1.8 V POR threshold level is reached, the option byte loading process starts, either to confirm or modify default BOR threshold levels, or to disable BOR permanently. Three BOR thresholds are available through option bytes. The device remains in reset mode when $V_{DD}$ is below a specified threshold, $V_{POR/PDR}$ or $V_{BOR}$, without the need for an external reset circuit.

Two external ceramic capacitors should be connected on $V_{CAP\_1}$ & $V_{CAP\_2}$ pin. Refer to *Figure 21: Power supply scheme* and *Figure 16: VCAP_1/VCAP_2 operating conditions*.

All packages have regulator ON feature.

### Regulator OFF

This feature is available only on packages featuring the BYPASS_REG pin. The regulator is disabled by holding BYPASS_REG high. The regulator OFF mode allows to supply externally a $V_{12}$ voltage source through $V_{CAP\_1}$ and $V_{CAP\_2}$ pins.

Since the internal voltage scaling is not manage internally, the external voltage value must be aligned with the targeted maximum frequency. Refer to *Table 14: General operating conditions*.

The two 2.2 µF ceramic capacitors should be replaced by two 100 nF decoupling capacitors.

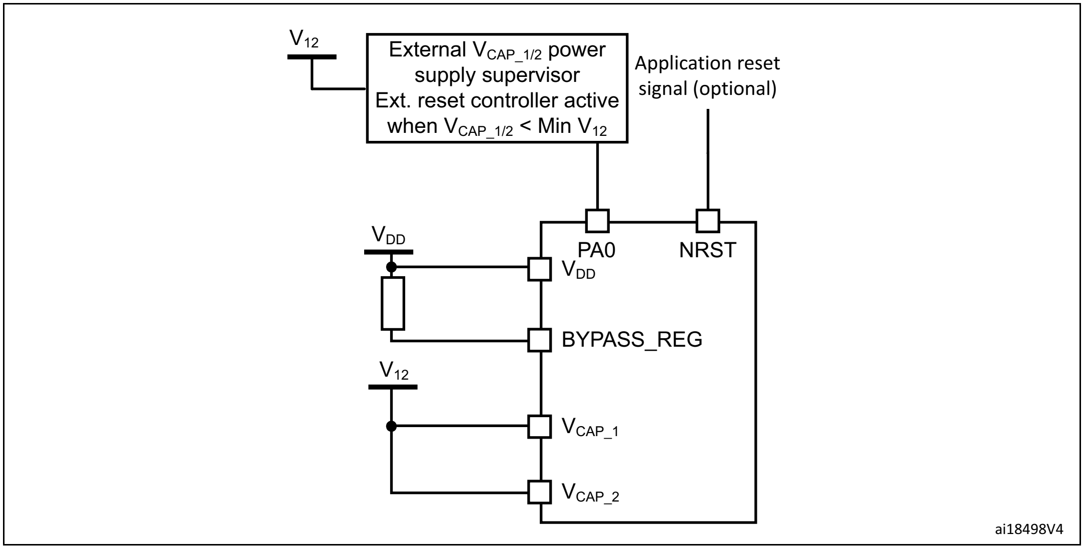
Refer to *Figure 21: Power supply scheme*

When the regulator is OFF, there is no more internal monitoring on $V_{12}$. An external power supply supervisor should be used to monitor the $V_{12}$ of the logic power domain. PA0 pin should be used for this purpose, and act as power-on reset on $V_{12}$ power domain.

In regulator OFF mode the following features are no more supported:

- PA0 cannot be used as a GPIO pin since it allows to reset a part of the $V_{12}$ logic power domain which is not reset by the NRST pin.
- As long as PA0 is kept low, the debug mode cannot be used under power-on reset. As a consequence, PA0 and NRST pins must be managed separately if the debug connection under reset or pre-reset is required.
- The standby mode is not available

**Figure 9. Regulator OFF**



Eight DAC trigger inputs are used in the device. The DAC channels are triggered through the timer update outputs that are also connected to different DMA streams.

### 2.2.38 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

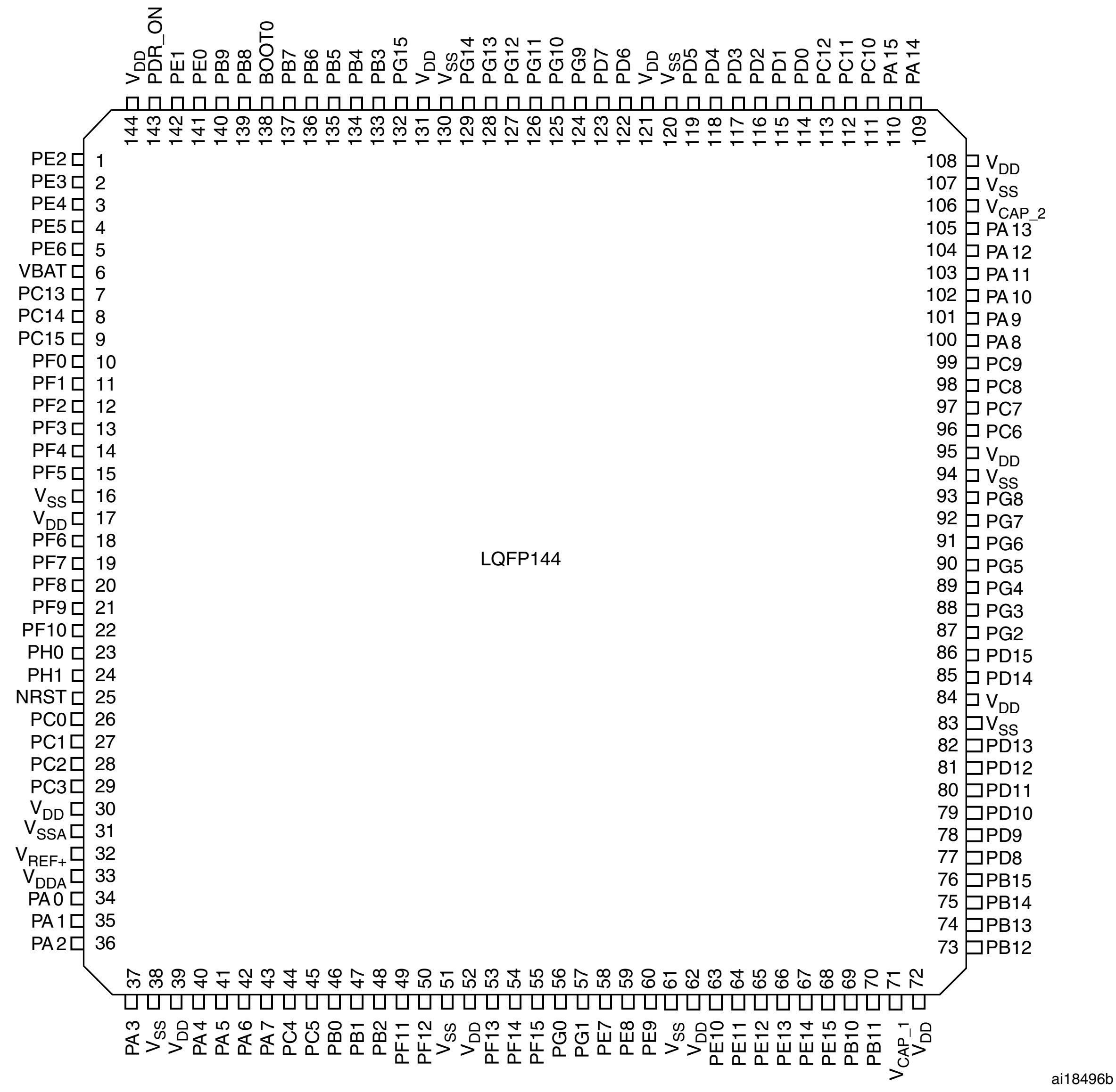
Debug is performed using 2 pins only instead of 5 required by the JTAG (JTAG pins could be re-use as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

### 2.2.39 Embedded Trace Macrocell™

The ARM Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F40xxx through a small number of ETM pins to an external hardware trace port analyser (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell operates with third party debugger software tools.

### Figure 14. STM32F40xxx LQFP144 pinout



1. The above figure shows the package top view.

Table 7. STM32F40xxx pin and ball definitions (continued)

| Pin number | | | | | | Pin name (function after reset)[1] | Pin type | I / O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP64 | WLCSP90 | LQFP100 | LQFP144 | UFBGA176 | LQFP176 | | | | | | |
| - | - | - | 11 | H3 | 17 | PF1 | I/O | FT | - | FSMC_A1 / I2C2_SCL / EVENTOUT | - |
| - | - | - | 12 | H2 | 18 | PF2 | I/O | FT | - | FSMC_A2 / I2C2_SMBA / EVENTOUT | - |
| - | - | - | 13 | J2 | 19 | PF3 | I/O | FT | (4) | FSMC_A3/EVENTOUT | ADC3_IN9 |
| - | - | - | 14 | J3 | 20 | PF4 | I/O | FT | (4) | FSMC_A4/EVENTOUT | ADC3_IN14 |
| - | - | - | 15 | K3 | 21 | PF5 | I/O | FT | (4) | FSMC_A5/EVENTOUT | ADC3_IN15 |
| - | C9 | 10 | 16 | G2 | 22 | $V_{SS}$ | S | - | - | - | - |
| - | B8 | 11 | 17 | G3 | 23 | $V_{DD}$ | S | - | - | - | - |
| - | - | - | 18 | K2 | 24 | PF6 | I/O | FT | (4) | TIM10_CH1 / FSMC_NIORD/ EVENTOUT | ADC3_IN4 |
| - | - | - | 19 | K1 | 25 | PF7 | I/O | FT | (4) | TIM11_CH1/FSMC_NREG/ EVENTOUT | ADC3_IN5 |
| - | - | - | 20 | L3 | 26 | PF8 | I/O | FT | (4) | TIM13_CH1 / FSMC_NIOWR/ EVENTOUT | ADC3_IN6 |
| - | - | - | 21 | L2 | 27 | PF9 | I/O | FT | (4) | TIM14_CH1 / FSMC_CD/ EVENTOUT | ADC3_IN7 |
| - | - | - | 22 | L1 | 28 | PF10 | I/O | FT | (4) | FSMC_INTR/ EVENTOUT | ADC3_IN8 |
| 5 | F10 | 12 | 23 | G1 | 29 | PH0/OSC_IN (PH0) | I/O | FT | - | EVENTOUT | OSC_IN(4) |
| 6 | F9 | 13 | 24 | H1 | 30 | PH1/OSC_OUT (PH1) | I/O | FT | - | EVENTOUT | OSC_OUT(4) |
| 7 | G10 | 14 | 25 | J1 | 31 | NRST | I/O | RST | - | - | - |
| 8 | E10 | 15 | 26 | M2 | 32 | PC0 | I/O | FT | (4) | OTG_HS_ULPI_STP/ EVENTOUT | ADC123_IN10 |
| 9 | - | 16 | 27 | M3 | 33 | PC1 | I/O | FT | (4) | ETH_MDC/ EVENTOUT | ADC123_IN11 |
| 10 | D10 | 17 | 28 | M4 | 34 | PC2 | I/O | FT | (4) | SPI2_MISO / OTG_HS_ULPI_DIR / ETH_MII_TXD2 /I2S2ext_SD/ EVENTOUT | ADC123_IN12 |

## Table 9. Alternate function mapping (continued)

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2 | TIM3/4/5 | TIM8/9/10/11 | I2C1/2/3 | SPI1/SPI2/I2S2/I2S2ext | SPI3/I2Sext/I2S3 | USART1/2/3/I2S3ext | UART4/5/USART6 | CAN1/2 TIM12/13/14 | OTG_FS/OTG_HS | ETH | FSMC/SDIO/OTG_FS | DCMI | | |
| Port B | PB0 | - | TIM1_CH2N | TIM3_CH3 | TIM8_CH2N | - | - | - | - | - | - | OTG_HS_ULPI_D1 | ETH _MII_RXD2 | - | - | - | EVENTOUT |
| | PB1 | - | TIM1_CH3N | TIM3_CH4 | TIM8_CH3N | | - | - | - | - | - | OTG_HS_ULPI_D2 | ETH _MII_RXD3 | - | - | - | EVENTOUT |
| | PB2 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PB3 | JTDO/TRACESWO | TIM2_CH2 | - | - | - | SPI1_SCK | SPI3_SCK<br>I2S3_CK | - | - | - | - | - | - | - | - | EVENTOUT |
| | PB4 | NJTRST | - | TIM3_CH1 | | - | SPI1_MISO | SPI3_MISO | I2S3ext_SD | - | - | - | - | - | - | - | EVENTOUT |
| | PB5 | - | - | TIM3_CH2 | | I2C1_SMBA | SPI1_MOSI | SPI3_MOSI<br>I2S3_SD | | - | CAN2_RX | OTG_HS_ULPI_D7 | ETH _PPS_OUT | - | DCMI_D10 | - | EVENTOUT |
| | PB6 | - | - | TIM4_CH1 | | I2C1_SCL | - | - | USART1_TX | - | CAN2_TX | - | - | - | DCMI_D5 | - | EVENTOUT |
| | PB7 | - | - | TIM4_CH2 | | I2C1_SDA | - | - | USART1_RX | - | - | - | - | FSMC_NL | DCMI_VSYNC | - | EVENTOUT |
| | PB8 | - | - | TIM4_CH3 | TIM10_CH1 | I2C1_SCL | - | - | - | - | CAN1_RX | - | ETH _MII_TXD3 | SDIO_D4 | DCMI_D6 | - | EVENTOUT |
| | PB9 | - | - | TIM4_CH4 | TIM11_CH1 | I2C1_SDA | SPI2_NSS<br>I2S2_WS | - | - | - | CAN1_TX | - | - | SDIO_D5 | DCMI_D7 | - | EVENTOUT |
| | PB10 | - | TIM2_CH3 | - | - | I2C2_SCL | SPI2_SCK<br>I2S2_CK | - | USART3_TX | - | - | OTG_HS_ULPI_D3 | ETH_ MII_RX_ER | - | - | - | EVENTOUT |
| | PB11 | - | TIM2_CH4 | - | - | I2C2_SDA | - | - | USART3_RX | - | - | OTG_HS_ULPI_D4 | ETH _MII_TX_EN<br>ETH _RMII_TX_EN | - | - | - | EVENTOUT |
| | PB12 | - | TIM1_BKIN | - | - | I2C2_SMBA | SPI2_NSS<br>I2S2_WS | - | USART3_CK | - | CAN2_RX | OTG_HS_ULPI_D5 | ETH _MII_TXD0<br>ETH _RMII_TXD0 | OTG_HS_ID | - | - | EVENTOUT |
| | PB13 | - | TIM1_CH1N | - | - | - | SPI2_SCK<br>I2S2_CK | - | USART3_CTS | - | CAN2_TX | OTG_HS_ULPI_D6 | ETH _MII_TXD1<br>ETH _RMII_TXD1 | - | - | - | EVENTOUT |
| | PB14 | - | TIM1_CH2N | - | TIM8_CH2N | - | SPI2_MISO | I2S2ext_SD | USART3_RTS | - | TIM12_CH1 | - | - | OTG_HS_DM | - | - | EVENTOUT |
| | PB15 | RTC_REFIN | TIM1_CH3N | - | TIM8_CH3N | - | SPI2_MOSI<br>I2S2_SD | - | - | - | TIM12_CH2 | - | - | OTG_HS_DP | - | - | EVENTOUT |

### Table 23. Typical and maximum current consumptions in Stop mode

| Symbol | Parameter | Conditions | Typ | Max | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25 °C | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | |
| $I_{DD\_STOP}$ | Supply current in Stop mode with main regulator in Run mode | Flash in Stop mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog) | 0.45 | 1.5 | 11.00 | 20.00 | mA |
| | | Flash in Deep power-down mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog) | 0.40 | 1.5 | 11.00 | 20.00 | |
| | Supply current in Stop mode with main regulator in Low-power mode | Flash in Stop mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog) | 0.31 | 1.1 | 8.00 | 15.00 | |
| | | Flash in Deep power-down mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog) | 0.28 | 1.1 | 8.00 | 15.00 | |

### Table 24. Typical and maximum current consumptions in Standby mode

| Symbol | Parameter | Conditions | Typ | | | Max[1] | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25 °C | | | $T_A$ = 85 °C | $T_A$ = 105 °C | |
| | | | $V_{DD}$ = 1.8 V | $V_{DD}$= 2.4 V | $V_{DD}$ = 3.3 V | $V_{DD}$ = 3.6 V | | |
| $I_{DD\_STBY}$ | Supply current in Standby mode | Backup SRAM ON, low-speed oscillator and RTC ON | 3.0 | 3.4 | 4.0 | 20 | 36 | µA |
| | | Backup SRAM OFF, low-speed oscillator and RTC ON | 2.4 | 2.7 | 3.3 | 16 | 32 | |
| | | Backup SRAM ON, RTC OFF | 2.4 | 2.6 | 3.0 | 12.5 | 24.8 | |
| | | Backup SRAM OFF, RTC OFF | 1.7 | 1.9 | 2.2 | 9.8 | 19.2 | |

1. Guaranteed by characterization.

A device reset allows normal operations to be resumed.

The test results are given in *Table 43*. They are based on the EMS levels and classes defined in application note AN1709.

**Table 43. EMS characteristics**

| Symbol | Parameter | Conditions | Level/ Class |
|---|---|---|---|
| $V_{FESD}$ | Voltage limits to be applied on any I/O pin to induce a functional disturbance | $V_{DD}$ = 3.3 V, LQFP176, $T_A$ = +25 °C, $f_{HCLK}$ = 168 MHz, conforms to IEC 61000-4-2 | 2B |
| $V_{EFTB}$ | Fast transient voltage burst limits to be applied through 100 pF on $V_{DD}$ and $V_{SS}$ pins to induce a functional disturbance | $V_{DD}$ = 3.3 V, LQFP176, $T_A$ = +25 °C, $f_{HCLK}$ = 168 MHz, conforms to IEC 61000-4-2 | 4A |

### Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

### Static latchup

Two complementary static tests are required on six parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latchup standard.

**Table 46. Electrical sensitivities**

| Symbol | Parameter | Conditions | Class |
|---|---|---|---|
| LU | Static latch-up class | $T_A$ = +105 °C conforming to JESD78A | II level A |

## 5.3.15 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below $V_{SS}$ or above $V_{DD}$ (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

### Functional susceptibilty to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of 5 µA/+0 µA range), or other functional failure (for example reset, oscillator frequency deviation).

Negative induced leakage current is caused by negative injection and positive induced leakage current by positive injection.

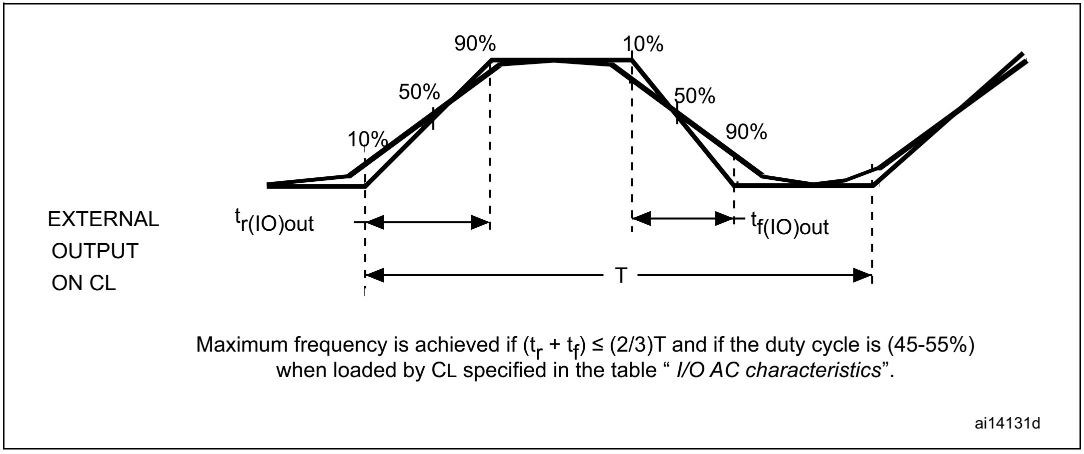
The test results are given in *Table 47*.

### Table 50. I/O AC characteristics(1)(2) (continued)

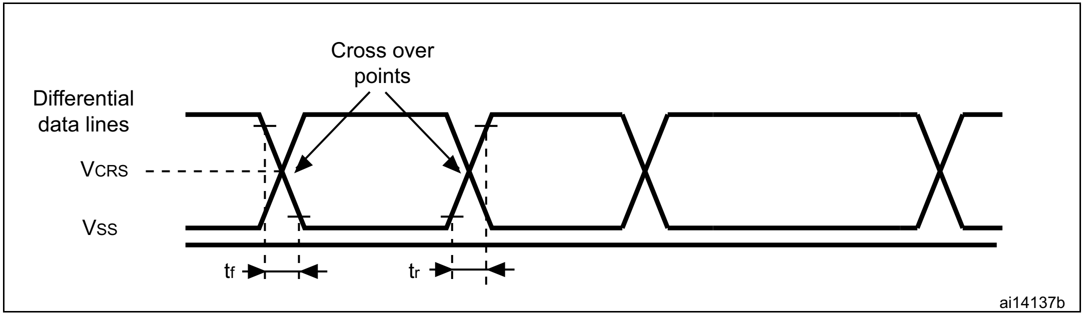
| OSPEEDRy [1:0] bit value(1) | Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| 11 | $F_{max(IO)out}$ | Maximum frequency(3) | $C_L$ = 30 pF, $V_{DD} > 2.70$ V | - | - | 100(4) | MHz |
| | | | $C_L$ = 30 pF, $V_{DD} > 1.8$ V | - | - | 50(4) | |
| | | | $C_L$ = 10 pF, $V_{DD} > 2.70$ V | - | - | 180(4) | |
| | | | $C_L$ = 10 pF, $V_{DD} > 1.8$ V | - | - | 100(4) | |
| | $t_{f(IO)out}$/ $t_{r(IO)out}$ | Output high to low level fall time and output low to high level rise time | $C_L$ = 30 pF, $V_{DD} > 2.70$ V | - | - | 4 | ns |
| | | | $C_L$ = 30 pF, $V_{DD} > 1.8$ V | - | - | 6 | |
| | | | $C_L$ = 10 pF, $V_{DD} > 2.70$ V | - | - | 2.5 | |
| | | | $C_L$ = 10 pF, $V_{DD} > 1.8$ V | - | - | 4 | |
| - | $t_{EXTIpw}$ | Pulse width of external signals detected by the EXTI controller | | 10 | - | - | ns |

1. Guaranteed by characterization.
2. The I/O speed is configured using the OSPEEDRy[1:0] bits. Refer to the STM32F4xx reference manual for a description of the GPIOx_SPEEDR GPIO port output speed register.
3. The maximum frequency is defined in *Figure 37*.
4. For maximum frequencies above 50 MHz, the compensation cell should be used.

### Figure 37. I/O AC characteristics definition



### Figure 44. USB OTG FS timings: definition of data signal rise and fall time



### Table 59. USB OTG FS electrical characteristics[1]

| Driver characteristics | | | | | |
|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Unit** |
| $t_r$ | Rise time[2] | $C_L$ = 50 pF | 4 | 20 | ns |
| $t_f$ | Fall time[2] | $C_L$ = 50 pF | 4 | 20 | ns |
| $t_{rfm}$ | Rise/ fall time matching | $t_r/t_f$ | 90 | 110 | % |
| $V_{CRS}$ | Output signal crossover voltage | - | 1.3 | 2.0 | V |

1. Guaranteed by design.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

## USB HS characteristics

Unless otherwise specified, the parameters given in *Table 62* for ULPI are derived from tests performed under the ambient temperature, $f_{HCLK}$ frequency summarized in *Table 61* and $V_{DD}$ supply voltage conditions summarized in *Table 60*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$.

Refer to Section *Section 5.3.16: I/O port characteristics* for more details on the input/output characteristics.

### Table 60. USB HS DC electrical characteristics

| **Symbol** | | **Parameter** | **Min.[1]** | **Max.[1]** | **Unit** |
|---|---|---|---|---|---|
| Input level | $V_{DD}$ | USB OTG HS operating voltage | 2.7 | 3.6 | V |

1. All the voltages are measured from the local ground potential.

### Table 61. USB HS clock timing parameters[1]

| **Parameter** | | **Symbol** | **Min** | **Nominal** | **Max** | **Unit** |
|---|---|---|---|---|---|---|
| $f_{HCLK}$ value to guarantee proper operation of USB HS interface | | - | 30 | - | - | MHz |
| Frequency (first transition) | 8-bit ±10% | $F_{START\_8BIT}$ | 54 | 60 | 66 | MHz |

### Table 61. USB HS clock timing parameters[1]

| Parameter | | Symbol | Min | Nominal | Max | Unit |
|---|---|---|---|---|---|---|
| Frequency (steady state) ±500 ppm | | $F_{STEADY}$ | 59.97 | 60 | 60.03 | MHz |
| Duty cycle (first transition) | 8-bit ±10% | $D_{START\_8BIT}$ | 40 | 50 | 60 | % |
| Duty cycle (steady state) ±500 ppm | | $D_{STEADY}$ | 49.975 | 50 | 50.025 | % |
| Time to reach the steady state frequency and duty cycle after the first transition | | $T_{STEADY}$ | - | - | 1.4 | ms |
| Clock startup time after the de-assertion of SuspendM | Peripheral | $T_{START\_DEV}$ | - | - | 5.6 | ms |
| | Host | $T_{START\_HOST}$ | - | - | - | |
| PHY preparation time after the first transition of the input clock | | $T_{PREP}$ | - | - | - | µs |

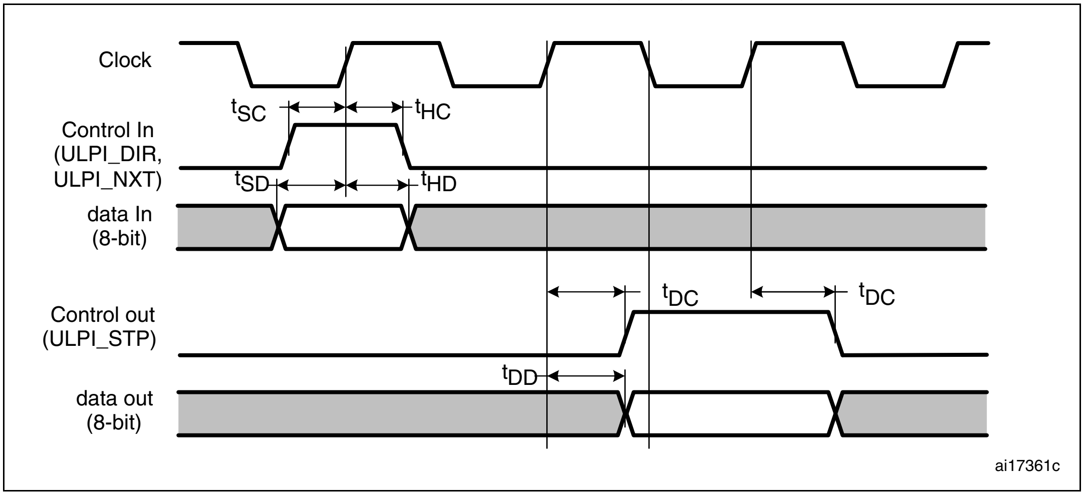
1. Guaranteed by design.

### Table 62. ULPI timing

| Parameter | Symbol | Value[1] | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| Control in (ULPI_DIR) setup time | $t_{SC}$ | - | 2.0 | ns |
| Control in (ULPI_NXT) setup time | | - | 1.5 | |
| Control in (ULPI_DIR, ULPI_NXT) hold time | $t_{HC}$ | 0 | - | |
| Data in setup time | $t_{SD}$ | - | 2.0 | |
| Data in hold time | $t_{HD}$ | 0 | - | |
| Control out (ULPI_STP) setup time and hold time | $t_{DC}$ | - | 9.2 | |
| Data out available from clock rising edge | $t_{DD}$ | - | 10.7 | |

1. $V_{DD}$ = 2.7 V to 3.6 V and $T_A$ = –40 to 85 °C.

### Figure 45. ULPI timing diagram



### Ethernet characteristics

Unless otherwise specified, the parameters given in *Table 64*, *Table 65* and *Table 66* for SMI, RMII and MII are derived from tests performed under the ambient temperature, $f_{HCLK}$ frequency summarized in *Table 14* and VDD supply voltage conditions summarized in *Table 63*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$.

Refer to *Section 5.3.16: I/O port characteristics* for more details on the input/output characteristics.

**Table 63. Ethernet DC electrical characteristics**

| Symbol | | Parameter | Min.(1) | Max.(1) | Unit |
|---|---|---|---|---|---|
| Input level | $V_{DD}$ | Ethernet operating voltage | 2.7 | 3.6 | V |

1. All the voltages are measured from the local ground potential.

*Table 64* gives the list of Ethernet MAC signals for the SMI (station management interface) and *Figure 46* shows the corresponding timing diagram.

**Figure 46. Ethernet SMI timing diagram**

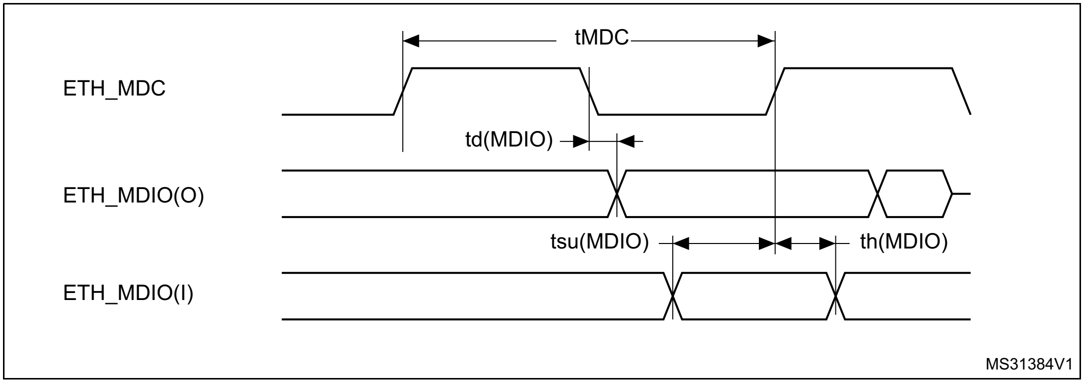


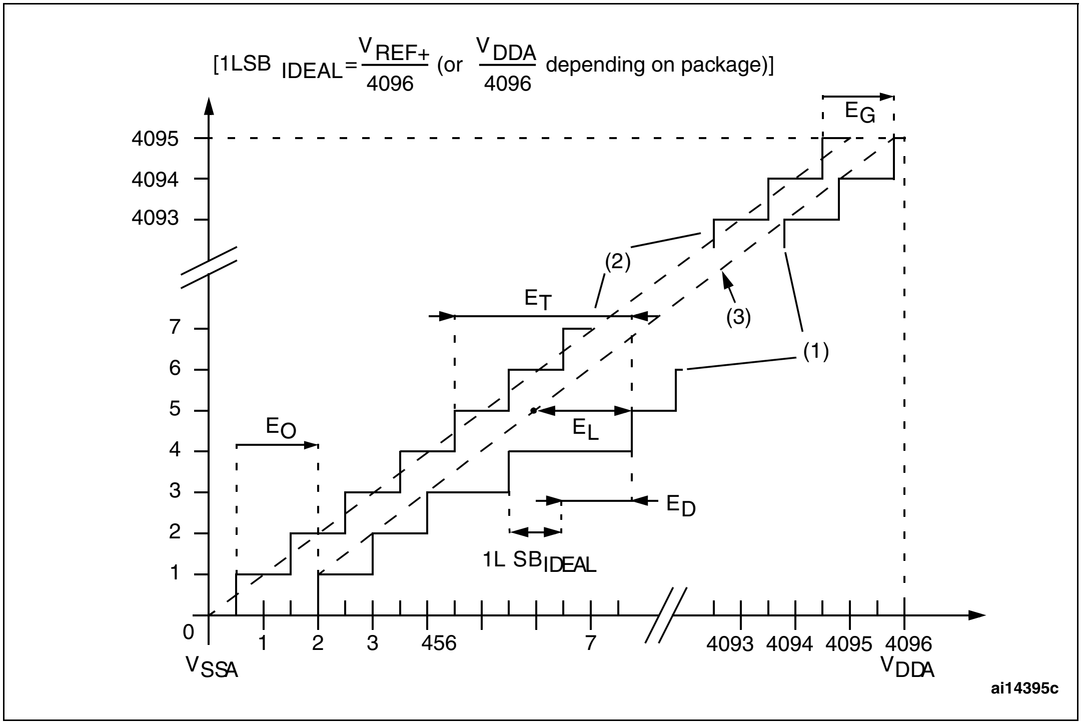
**Table 64. Dynamic characteristics: Eternity MAC signals for SMI(1)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{MDC}$ | MDC cycle time(2.38 MHz) | 411 | 420 | 425 | ns |
| $T_{d(MDIO)}$ | Write data valid time | 6 | 10 | 13 | |
| $t_{su(MDIO)}$ | Read data setup time | 12 | - | - | |
| $t_{h(MDIO)}$ | Read data hold time | 0 | - | - | |

1. Guaranteed by characterization.

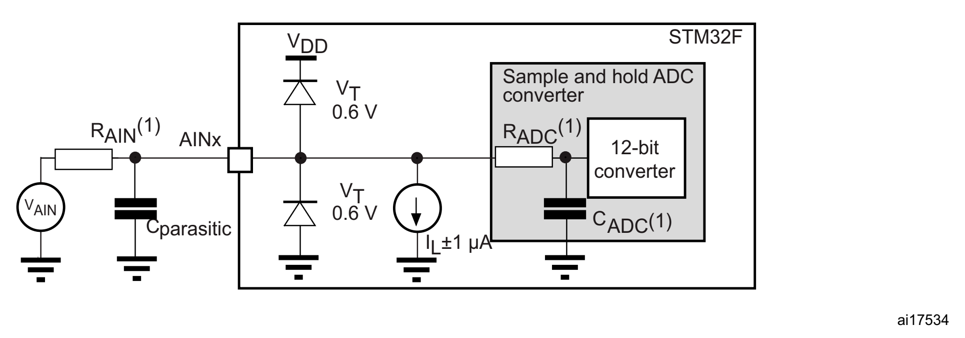
*Table 65* gives the list of Ethernet MAC signals for the RMII and *Figure 47* shows the corresponding timing diagram.

Figure 49. ADC accuracy characteristics



1. See also *Table 68*.
2. Example of an actual transfer curve.
3. Ideal transfer curve.
4. End point correlation line.
5. $E_T$ = Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves.
   EO = Offset Error: deviation between the first actual transition and the first ideal one.
   EG = Gain Error: deviation between the last ideal transition and the last actual one.
   ED = Differential Linearity Error: maximum deviation between actual steps and the ideal one.
   EL = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

Figure 50. Typical connection diagram using the ADC



1. Refer to *Table 67* for the values of $R_{AIN}$, $R_{ADC}$ and $C_{ADC}$.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 5 pF). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, $f_{ADC}$ should be reduced.

**Table 74. DAC characteristics (continued)**

| Symbol | Parameter | Min | Typ | Max | Unit | Comments |
|---|---|---|---|---|---|---|
| Offset(4) | Offset error (difference between measured value at Code (0x800) and the ideal value = $V_{REF+}/2$) | - | - | ±10 | mV | Given for the DAC in 12-bit configuration |
| | | - | - | ±3 | LSB | Given for the DAC in 10-bit at $V_{REF+}$ = 3.6 V |
| | | - | - | ±12 | LSB | Given for the DAC in 12-bit at $V_{REF+}$ = 3.6 V |
| Gain error(4) | Gain error | - | - | ±0.5 | % | Given for the DAC in 12-bit configuration |
| $t_{SETTLING}$(4) | Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±4LSB | - | 3 | 6 | µs | $C_{LOAD} \leq 50$ pF,<br>$R_{LOAD} \geq 5$ kΩ |
| THD(4) | Total Harmonic Distortion Buffer ON | - | - | - | dB | $C_{LOAD} \leq 50$ pF,<br>$R_{LOAD} \geq 5$ kΩ |
| Update rate(2) | Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB) | - | - | 1 | MS/s | $C_{LOAD} \leq 50$ pF,<br>$R_{LOAD} \geq 5$ kΩ |
| $t_{WAKEUP}$(4) | Wakeup time from off state (Setting the ENx bit in the DAC Control register) | - | 6.5 | 10 | µs | $C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ input code between lowest and highest possible ones. |
| PSRR+ (2) | Power supply rejection ratio (to $V_{DDA}$) (static DC measurement) | - | –67 | –40 | dB | No $R_{LOAD}$, $C_{LOAD}$ = 50 pF |

1. $V_{DD}/V_{DDA}$ minimum value of 1.7 V is obtained when the device operates in reduced temperature range, and with the use of an external power supply supervisor (refer to *Section : Internal reset OFF*).
2. Guaranteed by design.
3. The quiescent mode corresponds to a state where the DAC maintains a stable output level to ensure that no dynamic consumption occurs.
4. Guaranteed by characterization.

Figure 74. SD default mode

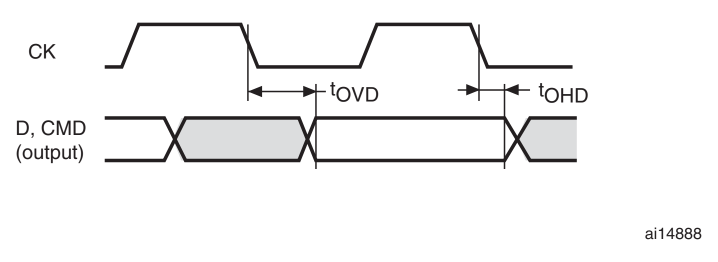


Table 88. Dynamic characteristics: SD / MMC characteristics[1]

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{PP}$ | Clock frequency in data transfer mode | | 0 | | 48 | MHz |
| | SDIO_CK/$f_{PCLK2}$ frequency ratio | | - | - | 8/3 | - |
| $t_{W(CKL)}$ | Clock low time | $f_{PP}$ = 48 MHz | 8.5 | 9 | - | ns |
| $t_{W(CKH)}$ | Clock high time | $f_{PP}$ = 48 MHz | 8.3 | 10 | - | |
| CMD, D inputs (referenced to CK) in MMC and SD HS mode | | | | | | |
| $t_{ISU}$ | Input setup time HS | $f_{PP}$ = 48 MHz | 3 | - | - | ns |
| $t_{IH}$ | Input hold time HS | $f_{PP}$ = 48 MHz | 0 | - | - | |
| CMD, D outputs (referenced to CK) in MMC and SD HS mode | | | | | | |
| $t_{OV}$ | Output valid time HS | $f_{PP}$ = 48 MHz | - | 4.5 | 6 | ns |
| $t_{OH}$ | Output hold time HS | $f_{PP}$ = 48 MHz | 1 | - | - | |
| CMD, D inputs (referenced to CK) in SD default mode | | | | | | |
| $t_{ISUD}$ | Input setup time SD | $f_{PP}$ = 24 MHz | 1.5 | - | - | ns |
| $t_{IHD}$ | Input hold time SD | $f_{PP}$ = 24 MHz | 0.5 | - | - | |
| CMD, D outputs (referenced to CK) in SD default mode | | | | | | |
| $t_{OVD}$ | Output valid default time SD | $f_{PP}$ = 24 MHz | - | 4.5 | 7 | ns |
| $t_{OHD}$ | Output hold default time SD | $f_{PP}$ = 24 MHz | 0.5 | - | - | |

1. Guaranteed by characterization.

### 5.3.29 RTC characteristics

Table 89. RTC characteristics

| Symbol | Parameter | Conditions | Min | Max |
|---|---|---|---|---|
| - | $f_{PCLK1}$/RTCCLK frequency ratio | Any read/write operation from/to an RTC register | 4 | - |

# 7 Part numbering

**Table 99. Ordering information scheme**

Example: STM32 F 405 R E T 6 xxx

**Device family**

STM32 = ARM-based 32-bit microcontroller

**Product type**

F = general-purpose

**Device subfamily**

405 = STM32F40xxx, connectivity
407= STM32F40xxx, connectivity, camera interface, Ethernet

**Pin count**

R = 64 pins
O = 90 pins
V = 100 pins
Z = 144 pins
I = 176 pins

**Flash memory size**

E = 512 Kbytes of Flash memory
G = 1024 Kbytes of Flash memory

**Package**

T = LQFP
H = UFBGA
Y = WLCSP

**Temperature range**

6 = Industrial temperature range, –40 to 85 °C.
7 = Industrial temperature range, –40 to 105 °C.

**Options**

xxx = programmed parts
TR = tape and reel

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.