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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

| Product Status | Active |
|----------------------------|---|
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 168MHz |
| Connectivity | CANbus, I ² C, IrDA, LINbus, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, I ² S, LCD, POR, PWM, WDT |
| Number of I/O | 51 |
| Program Memory Size | 1MB (1M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 192К х 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 16x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f405rgt6 |

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

- 8- to 14-bit parallel camera interface up to 54 Mbytes/s
- 96-bit unique ID
- RTC: subsecond accuracy, hardware calendar
- True random number generator
- CRC calculation unit

Table 1. Device summary

| Reference | Part number |
|-------------|---|
| STM32F405xx | STM32F405RG, STM32F405VG, STM32F405ZG, STM32F405OG, STM32F405OE |
| STM32F407xx | STM32F407VG, STM32F407IG, STM32F407ZG, STM32F407VE, STM32F407ZE, STM32F407IE |



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Figure 6. Multi-AHB matrix

2.2.8 DMA controller (DMA)

The devices feature two general-purpose dual-port DMAs (DMA1 and DMA2) with 8 streams each. They are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They feature dedicated FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB).

The two DMA controllers support circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

Each stream is connected to dedicated hardware DMA requests, with support for software trigger on each stream. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals:

- SPI and I²S
- I²C
- USART
- General-purpose, basic and advanced-control timers TIMx
- DAC
- SDIO
- Camera interface (DCMI)
- ADC.

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Figure 8. PDR_ON and NRST control with internal reset OFF



2.2.16 Voltage regulator

The regulator has four operating modes:

- Regulator ON
 - Main regulator mode (MR)
 - Low-power regulator (LPR)
 - Power-down
- Regulator OFF

Regulator ON

On packages embedding the BYPASS_REG pin, the regulator is enabled by holding BYPASS_REG low. On all other packages, the regulator is always enabled.

There are three power modes configured by software when regulator is ON:

- MR is used in the nominal regulation mode (With different voltage scaling in Run) In Main regulator mode (MR mode), different voltage scaling are provided to reach the best compromise between maximum frequency and dynamic power consumption. Refer to *Table 14: General operating conditions*.
- LPR is used in the Stop modes
 The LP regulator mode is configured by software when entering Stop mode.
- Power-down is used in Standby mode.
 - The Power-down mode is activated only when entering in Standby mode. The regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption. The contents of the registers and SRAM are lost)



| | | | | M# 00000 | | |
|---------------------|-------|--------------------|-------------------------------|----------|------------------------|------------|
| Pins ⁽¹⁾ | CF | NOR/PSRAM/ SRAM | AM/ NOR/PSRAM Mux NAND 16 bit | | LQFP100 ⁽²⁾ | (2) (2) |
| PF1 | A1 | A1 | - | - | - | - |
| PF2 | A2 | A2 | - | - | - | - |
| PF3 | A3 | A3 | - | - | - | - |
| PF4 | A4 | A4 | - | - | - | - |
| PF5 | A5 | A5 | - | - | - | - |
| PF6 | NIORD | - | - | - | - | - |
| PF7 | NREG | - | - | - | - | - |
| PF8 | NIOWR | - | - | - | - | - |
| PF9 | CD | - | - | - | - | - |
| PF10 | INTR | - | - | - | - | - |
| PF12 | A6 | A6 | - | - | - | - |
| PF13 | A7 | A7 | - | - | - | - |
| PF14 | A8 | A8 | - | - | - | - |
| PF15 | A9 | A9 | - | - | - | - |
| PG0 | A10 | A10 | | | - | - |
| PG1 | | A11 | - | - | - | - |
| PE7 | D4 | D4 | DA4 | D4 | Yes | Yes |
| PE8 | D5 | D5 | DA5 | D5 | Yes | Yes |
| PE9 | D6 | D6 | DA6 | D6 | Yes | Yes |
| PE10 | D7 | D7 | DA7 | D7 | Yes | Yes |
| PE11 | D8 | D8 | DA8 | D8 | Yes | Yes |
| PE12 | D9 | D9 | DA9 | D9 | Yes | Yes |
| PE13 | D10 | D10 | DA10 | D10 | Yes | Yes |
| PE14 | D11 | D11 | DA11 | D11 | Yes | Yes |
| PE15 | D12 | D12 | DA12 | D12 | Yes | Yes |
| PD8 | D13 | D13 | DA13 | D13 | Yes | Yes |
| PD9 | D14 | D14 | DA14 | D14 | Yes | Yes |
| PD10 | D15 | D15 | DA15 | D15 | Yes | Yes |
| PD11 | - | A16 | A16 | CLE | Yes | Yes |
| PD12 | - | A17 | A17 | ALE | Yes | Yes |
| PD13 | - | A18 | A18 | - | Yes | - |
| PD14 | D0 | D0 | DA0 | D0 | Yes | Yes |
| PD15 | D1 | D1 | DA1 | D1 | Yes | Yes |



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| | Table 9. Alternate function mapping (continued) | | | | | | | | | | | | | | | | |
|--------|---|-----------------------|-----------|------------------|-----------|--------------------------------|----------------------|------------------------|--------------------|---------------------------|-------------------|--------------------|--------------------------------------|-----------|----------------|------|----------|
| | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | | |
| Port | SYS | TIM1/2 | TIM3/4/5 | TIM8/9/10 /11 | I2C1/2/3 | SPI1/SPI2/ I2S2/I2S2e xt | SPI3/I2Sext /I2S3 | USART1/2/3/ I2S3ext | UART4/5/ USART6 | CAN1/2 TIM12/13/ 14 | OTG_FS/ OTG_HS | ЕТН | FSMC/SDIO /OTG_FS | DCMI | AF14 | AF15 | |
| | PB0 | - | TIM1_CH2N | TIM3_CH3 | TIM8_CH2N | - | - | - | - | - | - | OTG_HS_ULPI_ D1 | ETH_MII_RXD2 | - | - | - | EVENTOUT |
| | PB1 | - | TIM1_CH3N | TIM3_CH4 | TIM8_CH3N | | - | - | - | - | - | OTG_HS_ULPI_ D2 | ETH _MII_RXD3 | - | - | - | EVENTOUT |
| | PB2 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PB3 | JTDO/ TRACES WO | TIM2_CH2 | - | - | - | SPI1_SCK | SPI3_SCK I2S3_CK | - | - | - | - | - | - | - | - | EVENTOUT |
| | PB4 | NJTRST | - | TIM3_CH1 | | - | SPI1_MISO | SPI3_MISO | I2S3ext_SD | - | - | - | - | - | - | - | EVENTOUT |
| | PB5 | - | - | TIM3_CH2 | | I2C1_SMB A | SPI1_MOSI | SPI3_MOSI I2S3_SD | | - | CAN2_RX | OTG_HS_ULPI_ D7 | ETH_PPS_OUT | - | DCMI_D10 | - | EVENTOUT |
| | PB6 | - | - | TIM4_CH1 | | I2C1_SCL | - | - | USART1_TX | - | CAN2_TX | - | - | - | DCMI_D5 | - | EVENTOUT |
| | PB7 | - | - | TIM4_CH2 | | I2C1_SDA | - | - | USART1_RX | - | - | - | - | FSMC_NL | DCMI_VSYN C | - | EVENTOUT |
| Port B | PB8 | - | - | TIM4_CH3 | TIM10_CH1 | I2C1_SCL | - | - | - | - | CAN1_RX | - | ETH _MII_TXD3 | SDIO_D4 | DCMI_D6 | - | EVENTOUT |
| | PB9 | - | - | TIM4_CH4 | TIM11_CH1 | I2C1_SDA | SPI2_NSS I2S2_WS | - | - | - | CAN1_TX | - | - | SDIO_D5 | DCMI_D7 | - | EVENTOUT |
| | PB10 | - | TIM2_CH3 | - | - | I2C2_SCL | SPI2_SCK I2S2_CK | - | USART3_TX | - | - | OTG_HS_ULPI_ D3 | ETH_MII_RX_ER | - | - | - | EVENTOUT |
| | PB11 | - | TIM2_CH4 | - | - | I2C2_SDA | - | - | USART3_RX | - | - | OTG_HS_ULPI_ D4 | ETH _MII_TX_EN ETH _RMII_TX_EN | - | - | - | EVENTOUT |
| | PB12 | - | TIM1_BKIN | - | - | I2C2_ SMBA | SPI2_NSS I2S2_WS | - | USART3_CK | - | CAN2_RX | OTG_HS_ULPI_ D5 | ETH _MII_TXD0 ETH _RMII_TXD0 | OTG_HS_ID | - | - | EVENTOUT |
| | PB13 | - | TIM1_CH1N | - | - | - | SPI2_SCK I2S2_CK | - | USART3_CTS | - | CAN2_TX | OTG_HS_ULPI_ D6 | ETH _MII_TXD1 ETH _RMII_TXD1 | - | - | - | EVENTOUT |
| | PB14 | - | TIM1_CH2N | - | TIM8_CH2N | - | SPI2_MISO | I2S2ext_SD | USART3_RTS | - | TIM12_CH1 | - | - | OTG_HS_DM | - | - | EVENTOUT |
| | PB15 | RTC_ | TIM1_CH3N | - | TIM8_CH3N | - | SPI2_MOSI | - | - | - | TIM12_CH2 | - | - | OTG_HS_DP | - | - | EVENTOUT |

Pinouts and pin description

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Figure 25. Typical current consumption versus temperature, Run mode, code with data processing running from Flash (ART accelerator ON) or RAM, and peripherals ON





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| | | | Тур | Max | | | | |
|----------------------|---|--|---------------------------|---------------------------|---------------------------|----------------------------|------|--|
| Symbol | Parameter | Conditions | T _A = 25 °C | T _A = 25 °C | T _A = 85 °C | T _A = 105 °C | Unit | |
| I _{DD_STOP} | Supply current in | Flash in Stop mode, low-speed and high- speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog) | 0.45 | 1.5 | 11.00 | 20.00 | | |
| | with main regulator in Run mode | Flash in Deep power-down mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog) | 0.40 | 1.5 | 11.00 | 20.00 | - mA | |
| | Supply current in Stop mode with main regulator in Low-power mode | Flash in Stop mode, low-speed and high- speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog) | 0.31 | 1.1 | 8.00 | 15.00 | | |
| | | Flash in Deep power-down mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog) | 0.28 | 1.1 | 8.00 | 15.00 | | |

| Table 23. 1 | Typical and | maximum | current | consum | ptions | in Sto | p mode |
|-------------|-------------|---------|---------|--------|--------|--------|--------|
| | | | | | | | |

Table 24. Typical and maximum current consumptions in Standby mode

| | | Conditions | | Тур | | Ма | | | |
|----------------------|--------------------------------------|--|----------------------------|----------------------------|----------------------------|---------------------------|----------------------------|------|--|
| Symbol | Parameter | | 1 | (_A = 25 ° | C | T _A = 85 °C | T _A = 105 °C | Unit | |
| | | | V _{DD} = 1.8 V | V _{DD} = 2.4 V | V _{DD} = 3.3 V | V _{DD} = | = 3.6 V | | |
| I _{DD_STBY} | Supply current in Standby mode | Backup SRAM ON, low- speed oscillator and RTC ON | 3.0 | 3.4 | 4.0 | 20 | 36 | | |
| | | Backup SRAM OFF, low- speed oscillator and RTC ON | 2.4 | 2.7 | 3.3 | 16 | 32 | | |
| | | Backup SRAM ON, RTC OFF | 2.4 | 2.6 | 3.0 | 12.5 | 24.8 | - μΑ | |
| | | Backup SRAM OFF, RTC OFF | 1.7 | 1.9 | 2.2 | 9.8 | 19.2 | | |

1. Guaranteed by characterization.





A device reset allows normal operations to be resumed.

The test results are given in *Table 43*. They are based on the EMS levels and classes defined in application note AN1709.

| Symbol | Parameter | Conditions | Level/ Class |
|-------------------|---|---|-----------------|
| V _{FESD} | Voltage limits to be applied on any I/O pin to induce a functional disturbance | V _{DD} = 3.3 V, LQFP176, T _A = +25 °C, f _{HCLK} = 168 MHz, conforms to IEC 61000-4-2 | 2B |
| V _{EFTB} | Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance | V _{DD} = 3.3 V, LQFP176, T _A = +25 °C, f _{HCLK} = 168 MHz, conforms to IEC 61000-4-2 | 4A |

Table 43. EMS characteristics

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).



Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application, executing EEMBC[?] code, is running. This emission test is compliant with SAE IEC61967-2 standard which specifies the test board and the pin loading.

| Symbol | Parameter | Parameter Conditions fi | | Max vs. [f _{HSE} /f _{CPU}] 25/168 MHz | Unit |
|--------|------------|---|-----------------|--|------|
| | | | | 22 | |
| | | $V_{PP} = 3.3 \text{ V}$ T = 25 °C OFP176 | 0.1 to 30 MHZ | 32 | |
| | | v DD = 0.0 v, rA = 20 v, | 30 to 130 MHz | 25 | dBµV |
| | | | 130 MHz to 1GHz | 29 | |
| S | Poak loval | | SAE EMI Level | 4 | - |
| SEWI | | V _{DD} = 3.3 V, T _A = 25 °C, LQFP176 | 0.1 to 30 MHz | 19 | |
| | | package, conforming to SAE J1752/3 | 30 to 130 MHz | 16 | dBµV |
| | | ART accelerator and PLL spread | 130 MHz to 1GHz | 18 | |
| | | spectrum enabled | SAE EMI level | 3.5 | - |

| Table 44. | EMI | characteristics |
|-----------|-----|-----------------|
|-----------|-----|-----------------|

5.3.14 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts \times (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

| Symbol | Ratings | Conditions | Class | Maximum value ⁽¹⁾ | Unit |
|-----------------------|--|---|-------|---------------------------------|------|
| V _{ESD(HBM)} | Electrostatic discharge voltage (human body model) | $T_A = +25 \ ^{\circ}C$ conforming to JESD22-A114 | 2 | 2000 ⁽²⁾ | V |
| V _{ESD(CDM)} | Electrostatic discharge voltage (charge device model) | $T_A = +25$ °C conforming to ANSI/ESD STM5.3.1 | II | 500 | |

Table 45. ESD absolute maximum ratings

1. Guaranteed by characterization.

2. On V_{BAT} pin, $V_{ESD(HBM)}$ is limited to 1000 V.



Static latchup

Two complementary static tests are required on six parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latchup standard.

| Table | 46 | Electrical | sensitivities |
|-------|-----|------------|----------------|
| Table | τυ. | LICCUICAI | 30113111411103 |

| Symbol | Parameter | Conditions | Class |
|--------|-----------------------|---|------------|
| LU | Static latch-up class | $T_A = +105 \text{ °C conforming to JESD78A}$ | II level A |

5.3.15 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibilty to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of 5 μ A/+0 μ A range), or other functional failure (for example reset, oscillator frequency deviation).

Negative induced leakage current is caused by negative injection and positive induced leakage current by positive injection.

The test results are given in Table 47.



| | | Functional s | usceptibility | |
|---------------------------------|---|--------------------|--------------------|------|
| Symbol | Description | Negative injection | Positive injection | Unit |
| | Injected current on BOOT0 pin | - 0 | NA | |
| | Injected current on NRST pin | - 0 | NA | |
| I _{INJ} ⁽¹⁾ | Injected current on PE2, PE3, PE4, PE5, PE6, PI8, PC13, PC14, PC15, PI9, PI10, PI11, PF0, PF1, PF2, PF3, PF4, PF5, PF10, PH0/OSC_IN, PH1/OSC_OUT, PC0, PC1, PC2, PC3, PB6, PB7, PB8, PB9, PE0, PE1, PI4, PI5, PI6, PI7, PDR_ON, BYPASS_REG | - 0 | NA | mA |
| | Injected current on all FT pins | - 5 | NA | |
| | Injected current on any other pin | - 5 | +5 | |

Table 47. I/O current injection susceptibility

1. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

5.3.16 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 48* are derived from tests performed under the conditions summarized in *Table 14*. All I/Os are CMOS and TTL compliant.

| Symbol | Parameter | Conditions | Min | Тур | Мах | Unit |
|-----------------|--------------------------------|---|---|-----|---|------|
| V _{IL} | FT, TTa and NRST I/O input low | | - | - | 0.3V _{DD} -0.04 ⁽¹⁾ | |
| | level voltage | 1.7 v ≤v _{DD} ≤3.0 v | - | - | 0.3V _{DD} ⁽²⁾ | |
| | BOOT0 I/O input low level | 1.75 V ≤V _{DD} ≤3.6 V -40 °C≤T _A ≤105 °C | - | - | | |
| | voltage | 1.7 V ≤V _{DD} ≤3.6 V 0 °C≤T _A ≤105 °C | - | - | 0.1V _{DD} -+0.1 | V |
| | FT, TTa and NRST I/O input low | 1710 361 | 0.45V _{DD} +0.3 ⁽¹⁾ | - | - | v |
| | level voltage | 1.7 V ≤V _{DD} ≤3.0 V | 0.7V _{DD} ⁽²⁾ | - | - | |
| V _{IH} | BOOT0 I/O input low level | 1.75 V ≤V _{DD} ≤3.6 V -40 °C≤T _A ≤105 °C | $0.17 V_{-} + 0.7^{(1)}$ | - | - | |
| | voltage | 1.7 V ≤V _{DD} ≤3.6 V 0 °C≤T _A ≤105 °C | 0.17 VDD+0.7 V | - | - | |

| Table 48. | I/O | static | characteristics |
|-----------|-----|--------|-----------------|
|-----------|-----|--------|-----------------|



| OSPEEDRy [1:0] bit value ⁽¹⁾ | Symbol | Parameter | Conditions | Min | Тур | Max | Unit | |
|---|-------------------------|---|---|-----|-----|--------------------|------|--|
| | | t Maximum frequency ⁽³⁾ | C_L = 30 pF, V_{DD} > 2.70 V | - | - | 100 ⁽⁴⁾ | | |
| | с | | C _L = 30 pF, V _{DD >} 1.8 V | - | - | 50 ⁽⁴⁾ | MHz | |
| | r max(IO)out | | C _L = 10 pF, V _{DD >} 2.70 V | - | - | 180 ⁽⁴⁾ | | |
| | | | C _L = 10 pF, V _{DD >} 1.8 V | - | - | 100 ⁽⁴⁾ | | |
| 11 | t _{f(IQ)out} / | Output high to low level fall time and output low to high level rise time | C _L = 30 pF, V _{DD >} 2.70 V | - | - | 4 | | |
| | | | C _L = 30 pF, V _{DD >} 1.8 V | - | - | 6 | ns | |
| | t _{r(IO)out} | | C _L = 10 pF, V _{DD >} 2.70 V | - | - | 2.5 | | |
| | | | C _L = 10 pF, V _{DD >} 1.8 V | - | - | 4 | | |
| - | t _{EXTIpw} | Pulse width of external signals detected by the EXTI controller | | 10 | - | - | ns | |

Table 50. I/O AC characteristics⁽¹⁾⁽²⁾ (continued)

1. Guaranteed by characterization.

 The I/O speed is configured using the OSPEEDRy[1:0] bits. Refer to the STM32F4xx reference manual for a description of the GPIOx_SPEEDR GPIO port output speed register.

3. The maximum frequency is defined in *Figure* 37.

4. For maximum frequencies above 50 MHz, the compensation cell should be used.



Figure 37. I/O AC characteristics definition



Electrical characteristics

| Symbol | Parameter | Min | Тур | Мах | Unit | Comments |
|----------------------------------|--|-----|-----|--------------------------|------|--|
| R _{LOAD} ⁽²⁾ | Resistive load with buffer ON | 5 | - | - | kΩ | |
| R _O ⁽²⁾ | Impedance output with buffer OFF | - | - | 15 | kΩ | When the buffer is OFF, the Minimum resistive load between DAC_OUT and V_{SS} to have a 1% accuracy is 1.5 $M\Omega$ |
| C _{LOAD} ⁽²⁾ | Capacitive load | - | - | 50 | pF | Maximum capacitive load at DAC_OUT pin (when the buffer is ON). |
| DAC_OUT min ⁽²⁾ | Lower DAC_OUT voltage with buffer ON | 0.2 | - | - | V | It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code |
| DAC_OUT max ⁽²⁾ | Higher DAC_OUT voltage with buffer ON | - | - | V _{DDA} – 0.2 | V | 3.6 V and (0x1C7) to (0xE38) at V_{REF+} = 1.8 V |
| DAC_OUT min ⁽²⁾ | Lower DAC_OUT voltage with buffer OFF | - | 0.5 | - | mV | It gives the maximum output |
| DAC_OUT max ⁽²⁾ | Higher DAC_OUT voltage with buffer OFF | - | - | V _{REF+} – 1LSB | V | excursion of the DAC. |
| (4) | DAC DC V _{REF} current | - | 170 | 240 | uΔ | With no load, worst code (0x800) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs |
| 'VREF+ | mode (Standby mode) | - | 50 | 75 | μΛ | With no load, worst code (0xF1C) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs |
| | DAC DC VDDA current | - | 280 | 380 | μA | With no load, middle code (0x800) on the inputs |
| I _{DDA} ⁽⁴⁾ | consumption in quiescent mode ⁽³⁾ | - | 475 | 625 | μΑ | With no load, worst code (0xF1C) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs |
| DNI ⁽⁴⁾ | Differential non linearity Difference between two | - | - | ±0.5 | LSB | Given for the DAC in 10-bit configuration. |
| | consecutive code-1LSB) | - | - | ±2 | LSB | Given for the DAC in 12-bit configuration. |
| | Integral non linearity (difference between | - | - | ±1 | LSB | Given for the DAC in 10-bit configuration. |
| INL ⁽⁴⁾ | and the value at Code i on a line drawn between Code 0 and last Code 1023) | - | - | ±4 | LSB | Given for the DAC in 12-bit configuration. |

 Table 74. DAC characteristics (continued)





Figure 55. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms

1. Mode 2/B, C and D only. In Mode 1, FSMC_NADV is not used.

| Table 76. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings ⁽¹⁾⁽² |
|--|
|--|

| Symbol | Parameter | Min | Мах | Unit |
|--------------------------|---|------------------------|------------------------|------|
| t _{w(NE)} | FSMC_NE low time | 3T _{HCLK} | 3T _{HCLK} + 4 | ns |
| t _{v(NWE_NE)} | FSMC_NEx low to FSMC_NWE low | T _{HCLK} –0.5 | T _{HCLK} +0.5 | ns |
| t _{w(NWE)} | FSMC_NWE low time | T _{HCLK} –1 | T _{HCLK} +2 | ns |
| t _{h(NE_NWE)} | FSMC_NWE high to FSMC_NE high hold time | T _{HCLK} –1 | - | ns |
| t _{v(A_NE)} | FSMC_NEx low to FSMC_A valid | - | 0 | ns |
| t _{h(A_NWE)} | Address hold time after FSMC_NWE high | T _{HCLK} – 2 | - | ns |
| $t_{v(BL_NE)}$ | FSMC_NEx low to FSMC_BL valid | - | 1.5 | ns |
| t _{h(BL_NWE)} | FSMC_BL hold time after FSMC_NWE high | T _{HCLK} – 1 | - | ns |
| t _{v(Data_NE)} | Data to FSMC_NEx low to Data valid | - | T _{HCLK} +3 | ns |
| t _{h(Data_NWE)} | Data hold time after FSMC_NWE high | T _{HCLK} –1 | - | ns |
| t _{v(NADV_NE)} | FSMC_NEx low to FSMC_NADV low | - | 2 | ns |
| t _{w(NADV)} | FSMC_NADV low time | - | T _{HCLK} +0.5 | ns |

1. C_L = 30 pF.

2. Guaranteed by characterization.



| Symbol | Parameter | Min | Max | Unit |
|-------------------------|---|-----------------------|------------------------|------|
| t _{w(NWE)} | FSMC_NWE low width | 4T _{HCLK} –1 | 4T _{HCLK} + 3 | ns |
| t _{v(NWE-D)} | FSMC_NWE low to FSMC_D[15-0] valid | - | 0 | ns |
| t _{h(NWE-D)} | FSMC_NWE high to FSMC_D[15-0] invalid | 3T _{HCLK} –2 | - | ns |
| t _{d(D-NWE)} | FSMC_D[15-0] valid before FSMC_NWE high | 5T _{HCLK} –3 | - | ns |
| t _{d(ALE-NWE)} | FSMC_ALE valid before FSMC_NWE low | - | 3T _{HCLK} | ns |
| t _{h(NWE-ALE)} | FSMC_NWE high to FSMC_ALE invalid | 3T _{HCLK} –2 | _ | ns |

 Table 86. Switching characteristics for NAND Flash write cycles⁽¹⁾

1. C_L = 30 pF.

5.3.27 Camera interface (DCMI) timing specifications

Unless otherwise specified, the parameters given in *Table 87* for DCMI are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage summarized in *Table 13*, with the following configuration:

- PCK polarity: falling
- VSYNC and HSYNC polarity: high
- Data format: 14 bits







| Symbol | Parameter | Min | Max | Unit |
|--------------------|---|-----|-----|------|
| | Frequency ratio DCMI_PIXCLK/f _{HCLK} | - | 0.4 | |
| DCMI_PIXCLK | Pixel clock input | - | 54 | MHz |
| D _{pixel} | Pixel clock input duty cycle | 30 | 70 | % |



Device marking for LQFP64

The following figure gives an example of topside marking and pin 1 position identifier location.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.



Figure 80. LPQF64 marking example (package top view)

 Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.



| niconanical data (continued) | | | | | | | | | | |
|------------------------------|-------------|-------|--------|-----------------------|--------|--------|--|--|--|--|
| Symbol | millimeters | | | inches ⁽¹⁾ | | | | | | |
| | Min | Тур | Мах | Min | Тур | Max | | | | |
| ZD | - | 1.250 | - | - | 0.0492 | - | | | | |
| E | 23.900 | - | 24.100 | 0.9409 | - | 0.9488 | | | | |
| HE | 25.900 | - | 26.100 | 1.0197 | - | 1.0276 | | | | |
| ZE | - | 1.250 | - | - | 0.0492 | - | | | | |
| е | - | 0.500 | - | - | 0.0197 | - | | | | |
| L ⁽²⁾ | 0.450 | - | 0.750 | 0.0177 | - | 0.0295 | | | | |
| L1 | - | 1.000 | - | - | 0.0394 | - | | | | |
| k | 0° | - | 7° | 0° | - | 7° | | | | |
| ссс | - | - | 0.080 | - | - | 0.0031 | | | | |

Table 97. LQFP176 - 176-pin, 24 x 24 mm low profile quad flat packagemechanical data (continued)

1. Values in inches are converted from mm and rounded to 4 decimal digits.

2. L dimension is measured at gauge plane at 0.25 mm above the seating plane.

