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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

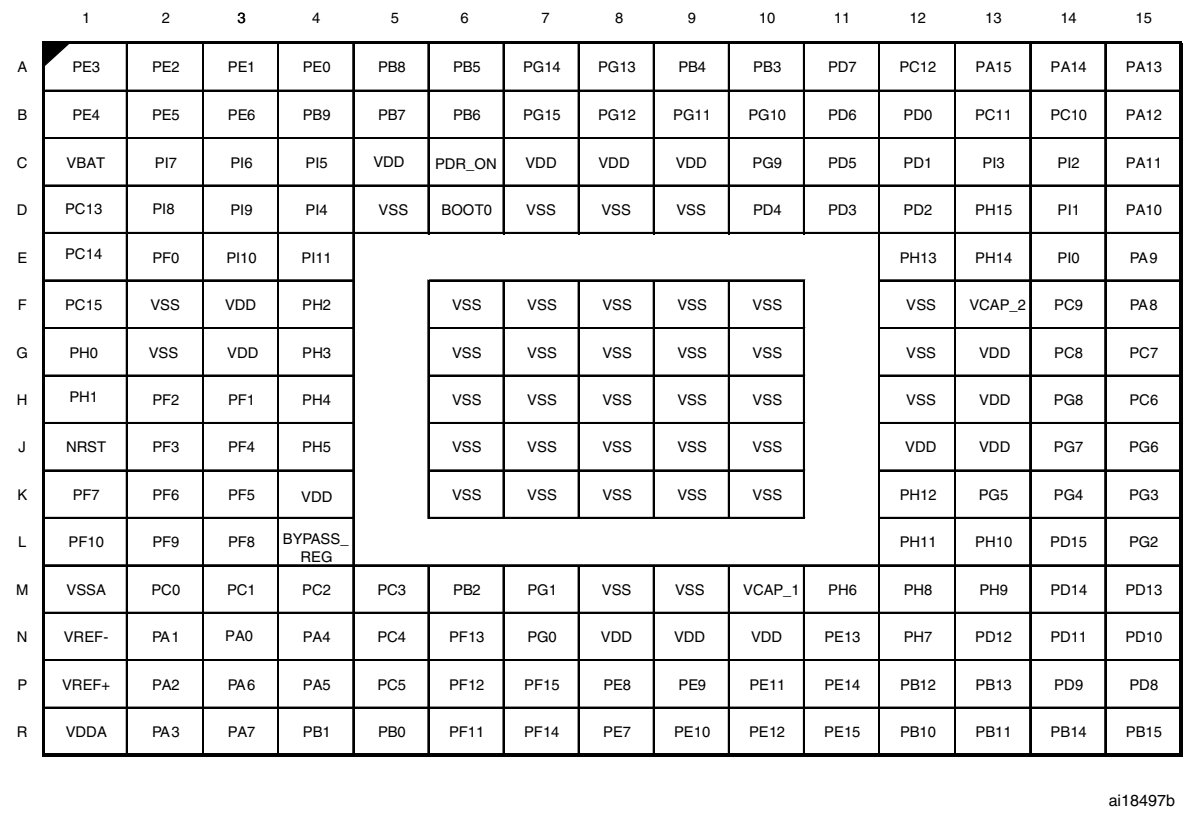
Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	168MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f405rgt6w

Table 2. STM32F405xx and STM32F407xx: features and peripheral counts (continued)

Peripherals		STM32F405RG	STM32F405OG	STM32F405VG	STM32F405ZG	STM32F405OE	STM32F407Vx	STM32F407Zx	STM32F407Ix
Communication interfaces	SPI / I2S	3/2 (full duplex)(2)							
	I^2C	3							
	USART/ UART	4/2							
	USB OTG FS	Yes							
	USB OTG HS	Yes							
	CAN	2							
	SDIO	Yes							
Camera interface		No					Yes		
GPIOs		51	72	82	114	72	82	114	140
12-bit ADC Number of channels		3							
		16	13	16	24	13	16	24	24
12-bit DAC Number of channels		Yes 2							
Maximum CPU frequency		168 MHz							
Operating voltage		1.8 to 3.6 V(3)							
Operating temperatures		Ambient temperatures: –40 to +85 °C /–40 to +105 °C							
		Junction temperature: –40 to + 125 °C							
Package		LQFP64	WLCSP90	LQFP100	LQFP144	WLCSP90	LQFP100	LQFP144	UFBGA176 LQFP176

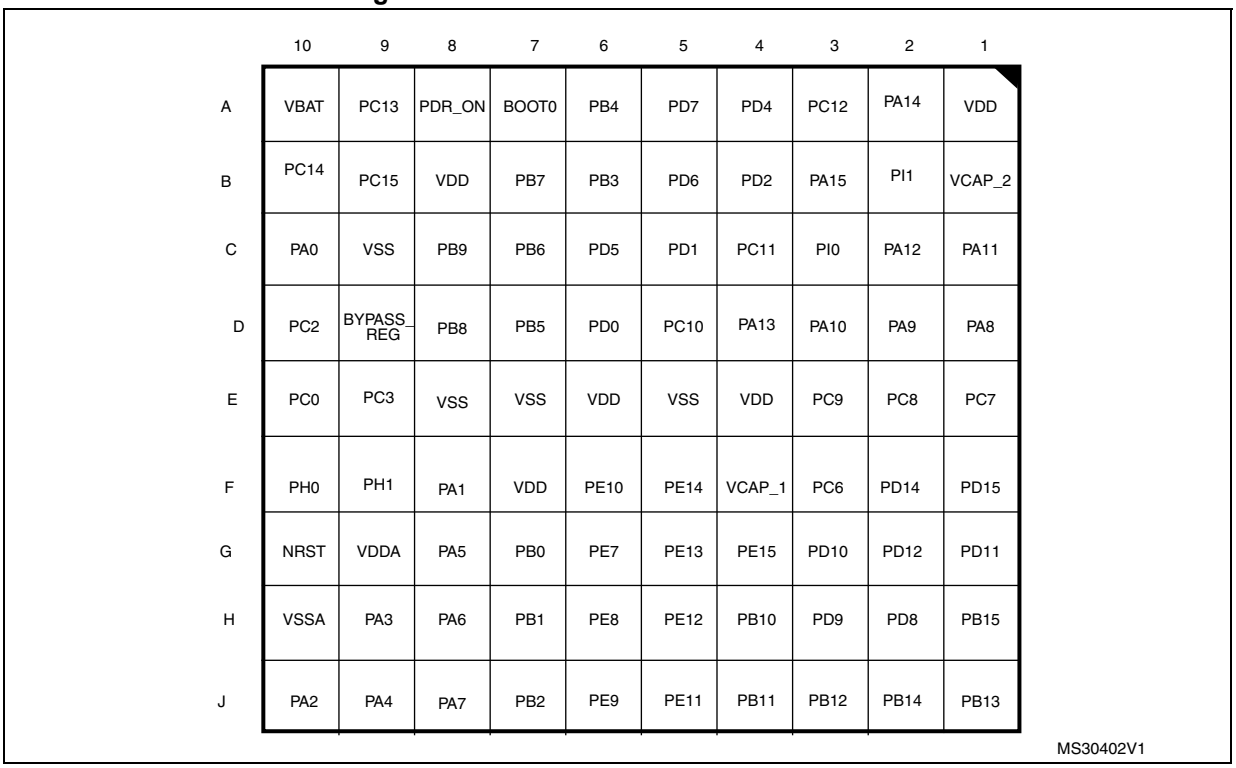
1. For the LQFP100 and WLCSP90 packages, only FSMC Bank1 or Bank2 are available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select. Bank2 can only support a 16- or 8-bit NAND Flash memory using the NCE2 Chip Select. The interrupt line cannot be used since Port G is not available in this package.
2. The SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I^2S audio mode.
3. V_{DD}/V_{DDA} minimum value of 1.7 V is obtained when the device operates in reduced temperature range, and with the use of an external power supply supervisor (refer to *Section : Internal reset OFF*).

Figure 16. STM32F40xxx UFBGA176 ballout



1. This figure shows the package top view.

Figure 17. STM32F40xxx WLCSP90 ballout



1. This figure shows the package bump view.

Table 6. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
I/O structure	FT	5 V tolerant I/O
	TTa	3.3 V tolerant I/O directly connected to ADC
	B	Dedicated BOOT0 pin
	RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Alternate functions	Functions selected through GPIOx_AFR registers	
Additional functions	Functions directly selected/enabled through peripheral registers	

Table 7. STM32F40xxx pin and ball definitions

Pin number						Pin name (function after reset)[1]	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP64	WLCSP90	LQFP100	LQFP144	UFBGA176	LQFP176						
-	-	1	1	A2	1	PE2	I/O	FT	-	TRACECLK/ FSMC_A23 / ETH_MII_TXD3 / EVENTOUT	-
-	-	2	2	A1	2	PE3	I/O	FT	-	TRACED0/FSMC_A19 / EVENTOUT	-
-	-	3	3	B1	3	PE4	I/O	FT	-	TRACED1/FSMC_A20 / DCMI_D4/ EVENTOUT	-
-	-	4	4	B2	4	PE5	I/O	FT	-	TRACED2 / FSMC_A21 / TIM9_CH1 / DCMI_D6 / EVENTOUT	-
-	-	5	5	B3	5	PE6	I/O	FT	-	TRACED3 / FSMC_A22 / TIM9_CH2 / DCMI_D7 / EVENTOUT	-
1	A10	6	6	C1	6	V_{BAT}	S	-	-	-	-
-	-	-	-	D2	7	PI8	I/O	FT	(2)(3)	EVENTOUT	RTC_TAMP1, RTC_TAMP2, RTC_TS
2	A9	7	7	D1	8	PC13	I/O	FT	(2)(3)	EVENTOUT	RTC_OUT, RTC_TAMP1, RTC_TS
3	B10	8	8	E1	9	PC14/OSC32_IN (PC14)	I/O	FT	(2)(3)	EVENTOUT	OSC32_IN[4]
4	B9	9	9	F1	10	PC15/ OSC32_OUT (PC15)	I/O	FT	(2)(3)	EVENTOUT	OSC32_OUT[4]
-	-	-	-	D3	11	PI9	I/O	FT	-	CAN1_RX / EVENTOUT	-
-	-	-	-	E3	12	PI10	I/O	FT	-	ETH_MII_RX_ER / EVENTOUT	-
-	-	-	-	E4	13	PI11	I/O	FT	-	OTG_HS_ULPI_DIR / EVENTOUT	-
-	-	-	-	F2	14	V_{SS}	S	-	-	-	-
-	-	-	-	F3	15	V_{DD}	S	-	-	-	-
-	-	-	10	E2	16	PF0	I/O	FT	-	FSMC_A0 / I2C2_SDA / EVENTOUT	-

Table 9. Alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10 /11	I2C1/2/3	SPI1/SPI2/ I2S2/I2S2ext	SPI3/I2Sext /I2S3	USART1/2/3/ I2S3ext	UART4/5/ USART6	CAN1/2 TIM12/13/ 14	OTG_FS/ OTG_HS	ETH	FSMC/SDIO /OTG_FS	DCMI		
Port C	PC0	-	-	-	-	-	-	-	-	-	-	OTG_HS_ULPI_ STP	-	-	-	-	EVENTOUT
	PC1	-	-	-	-	-	-	-	-	-	-	-	ETH_MDC	-	-	-	EVENTOUT
	PC2	-	-	-	-	-	SPI2_MISO	I2S2ext_SD	-	-	-	OTG_HS_ULPI_ DIR	ETH _MII_TXD2	-	-	-	EVENTOUT
	PC3	-	-	-	-	-	SPI2_MOSI I2S2_SD	-	-	-	-	OTG_HS_ULPI_ NXT	ETH _MII_TX_CLK	-	-	-	EVENTOUT
	PC4	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_RXD0 ETH_RMII_RXD0	-	-	-	EVENTOUT
	PC5	-	-	-	-	-	-	-	-	-	-	-	ETH _MII_RXD1 ETH _RMII_RXD1	-	-	-	EVENTOUT
	PC6	-	-	TIM3_CH1	TIM8_CH1		I2S2_MCK		-	USART6_TX	-	-	-	SDIO_D6	DCMI_D0	-	EVENTOUT
	PC7	-	-	TIM3_CH2	TIM8_CH2	-	-	I2S3_MCK	-	USART6_RX	-	-	-	SDIO_D7	DCMI_D1	-	EVENTOUT
	PC8	-	-	TIM3_CH3	TIM8_CH3	-	-	-	-	USART6_CK	-	-	-	SDIO_D0	DCMI_D2	-	EVENTOUT
	PC9	MCO2	-	TIM3_CH4	TIM8_CH4	I2C3_SDA	I2S_CKIN	-	-	-	-	-	-	SDIO_D1	DCMI_D3	-	EVENTOUT
	PC10	-	-	-	-	-	-	SPI3_SCK/ I2S3_CK	USART3_TX/	UART4_TX	-	-	-	SDIO_D2	DCMI_D8	-	EVENTOUT
	PC11	-	-	-	-	-	I2S3ext_SD	SPI3_MISO/	USART3_RX	UART4_RX	-	-	-	SDIO_D3	DCMI_D4	-	EVENTOUT
	PC12	-	-	-	-	-	-	SPI3_MOSI I2S3_SD	USART3_CK	UART5_TX	-	-	-	SDIO_CK	DCMI_D9	-	EVENTOUT
	PC13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT

Table 15. Limitations depending on the operating power supply range

Operating power supply range	ADC operation	Maximum Flash memory access frequency with no wait state ($f_{Flashmax}$)	Maximum Flash memory access frequency with wait states(1) (2)	I/O operation	Clock output Frequency on I/O pins	Possible Flash memory operations
V_{DD} =1.8 to 2.1 V(3)	Conversion time up to 1.2 Msps	20 MHz(4)	160 MHz with 7 wait states	– Degraded speed performance – No I/O compensation	up to 30 MHz	8-bit erase and program operations only
V_{DD} = 2.1 to 2.4 V	Conversion time up to 1.2 Msps	22 MHz	168 MHz with 7 wait states	– Degraded speed performance – No I/O compensation	up to 30 MHz	16-bit erase and program operations
V_{DD} = 2.4 to 2.7 V	Conversion time up to 2.4 Msps	24 MHz	168 MHz with 6 wait states	– Degraded speed performance – I/O compensation works	up to 48 MHz	16-bit erase and program operations
V_{DD} = 2.7 to 3.6 V(5)	Conversion time up to 2.4 Msps	30 MHz	168 MHz with 5 wait states	– Full-speed operation – I/O compensation works	– up to 60 MHz when V_{DD} = 3.0 to 3.6 V – up to 48 MHz when V_{DD} = 2.7 to 3.0 V	32-bit erase and program operations

1. It applies only when code executed from Flash memory access, when code executed from RAM, no wait state is required.
2. Thanks to the ART accelerator and the 128-bit Flash memory, the number of wait states given here does not impact the execution speed from Flash memory since the ART accelerator allows to achieve a performance equivalent to 0 wait state program execution.
3. V_{DD}/VDDA minimum value of 1.7 V is obtained when the device operates in reduced temperature range, and with the use of an external power supply supervisor (refer to *Section : Internal reset OFF*).
4. Prefetch is not available. Refer to AN3430 application note for details on how to adjust performance and power.
5. The voltage range for OTG USB FS can drop down to 2.7 V. However it is degraded between 2.7 and 3 V.

5.3.5 Embedded reset and power control block characteristics

The parameters given in *Table 19* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Table 19. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.09	2.14	2.19	V
		PLS[2:0]=000 (falling edge)	1.98	2.04	2.08	V
		PLS[2:0]=001 (rising edge)	2.23	2.30	2.37	V
		PLS[2:0]=001 (falling edge)	2.13	2.19	2.25	V
		PLS[2:0]=010 (rising edge)	2.39	2.45	2.51	V
		PLS[2:0]=010 (falling edge)	2.29	2.35	2.39	V
		PLS[2:0]=011 (rising edge)	2.54	2.60	2.65	V
		PLS[2:0]=011 (falling edge)	2.44	2.51	2.56	V
		PLS[2:0]=100 (rising edge)	2.70	2.76	2.82	V
		PLS[2:0]=100 (falling edge)	2.59	2.66	2.71	V
		PLS[2:0]=101 (rising edge)	2.86	2.93	2.99	V
		PLS[2:0]=101 (falling edge)	2.65	2.84	2.92	V
		PLS[2:0]=110 (rising edge)	2.96	3.03	3.10	V
		PLS[2:0]=110 (falling edge)	2.85	2.93	2.99	V
		PLS[2:0]=111 (rising edge)	3.07	3.14	3.21	V
		PLS[2:0]=111 (falling edge)	2.95	3.03	3.09	V
$V_{PVDhyst}$(1)	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power-on/power-down reset threshold	Falling edge	1.60	1.68	1.76	V
		Rising edge	1.64	1.72	1.80	V
$V_{PDRhyst}$(1)	PDR hysteresis	-	-	40	-	mV
V_{BOR1}	Brownout level 1 threshold	Falling edge	2.13	2.19	2.24	V
		Rising edge	2.23	2.29	2.33	V

Table 19. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BOR2}	Brownout level 2 threshold	Falling edge	2.44	2.50	2.56	V
		Rising edge	2.53	2.59	2.63	V
V_{BOR3}	Brownout level 3 threshold	Falling edge	2.75	2.83	2.88	V
		Rising edge	2.85	2.92	2.97	V
$V_{BORhyst}$(1)	BOR hysteresis	-	-	100	-	mV
$T_{RSTTEMPO}$(1)(2)	Reset temporization	-	0.5	1.5	3.0	ms
I_{RUSH}(1)	InRush current on voltage regulator power-on (POR or wakeup from Standby)	-	-	160	200	mA
E_{RUSH}(1)	InRush energy on voltage regulator power-on (POR or wakeup from Standby)	V_{DD} = 1.8 V, T_A = 105 °C, I_{RUSH} = 171 mA for 31 µs	-	-	5.4	µC

1. Guaranteed by design.
2. The reset temporization is measured from the power-on (POR reset or wakeup from V_{BAT}) to the instant when first instruction is read by the user application code.

5.3.6 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.
The current consumption is measured as described in *Figure 22: Current consumption measurement scheme*.

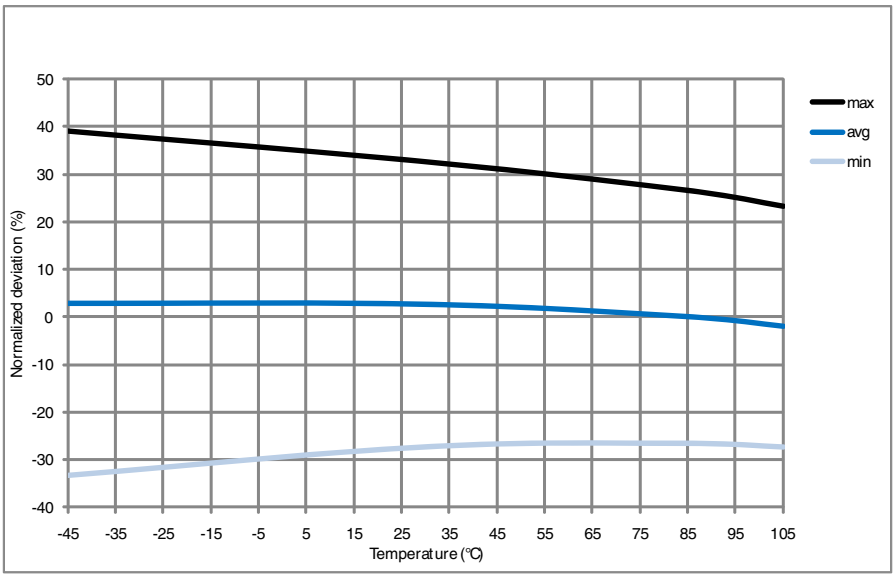
All Run mode current consumption measurements given in this section are performed using a CoreMark-compliant code.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- At startup, all I/O pins are configured as analog inputs by firmware.
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash memory access time is adjusted to f_{HCLK} frequency (0 wait state from 0 to 30 MHz, 1 wait state from 30 to 60 MHz, 2 wait states from 60 to 90 MHz, 3 wait states from 90 to 120 MHz, 4 wait states from 120 to 150 MHz, and 5 wait states from 150 to 168 MHz).
- When the peripherals are enabled HCLK is the system clock, $f_{PCLK1} = f_{HCLK}/4$, and $f_{PCLK2} = f_{HCLK}/2$, except is explicitly mentioned.
- The maximum values are obtained for V_{DD} = 3.6 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Figure 34. ACC_{LSI} versus temperature



5.3.10 PLL characteristics

The parameters given in *Table 36* and *Table 37* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Table 36. Main PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock(1)	-	0.95(2)	1	2.10	MHz
f_{PLL_OUT}	PLL multiplier output clock	-	24	-	168	MHz
f_{PLL48_OUT}	48 MHz PLL multiplier output clock	-	-	48	75	MHz
f_{VCO_OUT}	PLL VCO output	-	100	-	432	MHz
t_{LOCK}	PLL lock time	VCO freq = 100 MHz	75	-	200	µs
		VCO freq = 432 MHz	100	-	300	

Table 37. PLLI2S (audio PLL) characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD(PLLI2S)}$(4)	PLLI2S power consumption on V_{DD}	VCO freq = 100 MHz VCO freq = 432 MHz	0.15 0.45	-	0.40 0.75	mA
$I_{DDA(PLLI2S)}$(4)	PLLI2S power consumption on V_{DDA}	VCO freq = 100 MHz VCO freq = 432 MHz	0.30 0.55	-	0.40 0.85	mA

1. Take care of using the appropriate division factor M to have the specified PLL input clock values.
2. Guaranteed by design.
3. Value given with main PLL running.
4. Guaranteed by characterization.

5.3.11 PLL spread spectrum clock generation (SSCG) characteristics

The spread spectrum clock generation (SSCG) feature allows to reduce electromagnetic interferences (see *Table 44: EMI characteristics*). It is available only on the main PLL.

Table 38. SSCG parameters constraint

Symbol	Parameter	Min	Typ	Max(1)	Unit
f_{Mod}	Modulation frequency	-	-	10	KHz
md	Peak modulation depth	0.25	-	2	%
MODEPER * INCSTEP		-	-	$2^{15}-1$	-

1. Guaranteed by design.

Equation 1

The frequency modulation period (MODEPER) is given by the equation below:

$$MODEPER = round[f_{PLL\_IN} / (4 \times f_{Mod})]$$

f_{PLL_IN} and f_{Mod} must be expressed in Hz.

As an example:

If f_{PLL_IN} = 1 MHz, and f_{MOD} = 1 kHz, the modulation depth (MODEPER) is given by equation 1:

$$MODEPER = round[10^6 / (4 \times 10^3)] = 250$$

Equation 2

Equation 2 allows to calculate the increment step (INCSTEP):

$$INCSTEP = round[((2^{15} - 1) \times md \times PLLN) / (100 \times 5 \times MODEPER)]$$

f_{VCO_OUT} must be expressed in MHz.

Static latchup

Two complementary static tests are required on six parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latchup standard.

Table 46. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

5.3.15 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibilty to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of 5 µA/+0 µA range), or other functional failure (for example reset, oscillator frequency deviation).

Negative induced leakage current is caused by negative injection and positive induced leakage current by positive injection.

The test results are given in *Table 47*.

5.3.18 TIM timer characteristics

The parameters given in *Table 52* and *Table 53* are guaranteed by design.

Refer to *Section 5.3.16: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 52. Characteristics of TIMx connected to the APB1 domain(1)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	AHB/APB1 prescaler distinct from 1, $f_{TIMxCLK}$ = 84 MHz	1	-	$t_{TIMxCLK}$
			11.9	-	ns
		AHB/APB1 prescaler = 1, $f_{TIMxCLK}$ = 42 MHz	1	-	$t_{TIMxCLK}$
			23.8	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	$f_{TIMxCLK}$ = 84 MHz APB1= 42 MHz	0	$f_{TIMxCLK}/2$	MHz
			0	42	MHz
Res_{TIM}	Timer resolution		-	16/32	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected		1	65536	$t_{TIMxCLK}$
			0.0119	780	µs
	32-bit counter clock period when internal clock is selected		1	-	$t_{TIMxCLK}$
			0.0119	51130563	µs
t_{MAX_COUNT}	Maximum possible count		-	65536 × 65536	$t_{TIMxCLK}$
			-	51.1	s

1. TIMx is used as a general term to refer to the TIM2, TIM3, TIM4, TIM5, TIM6, TIM7, and TIM12 timers.

Figure 41. SPI timing diagram - master mode

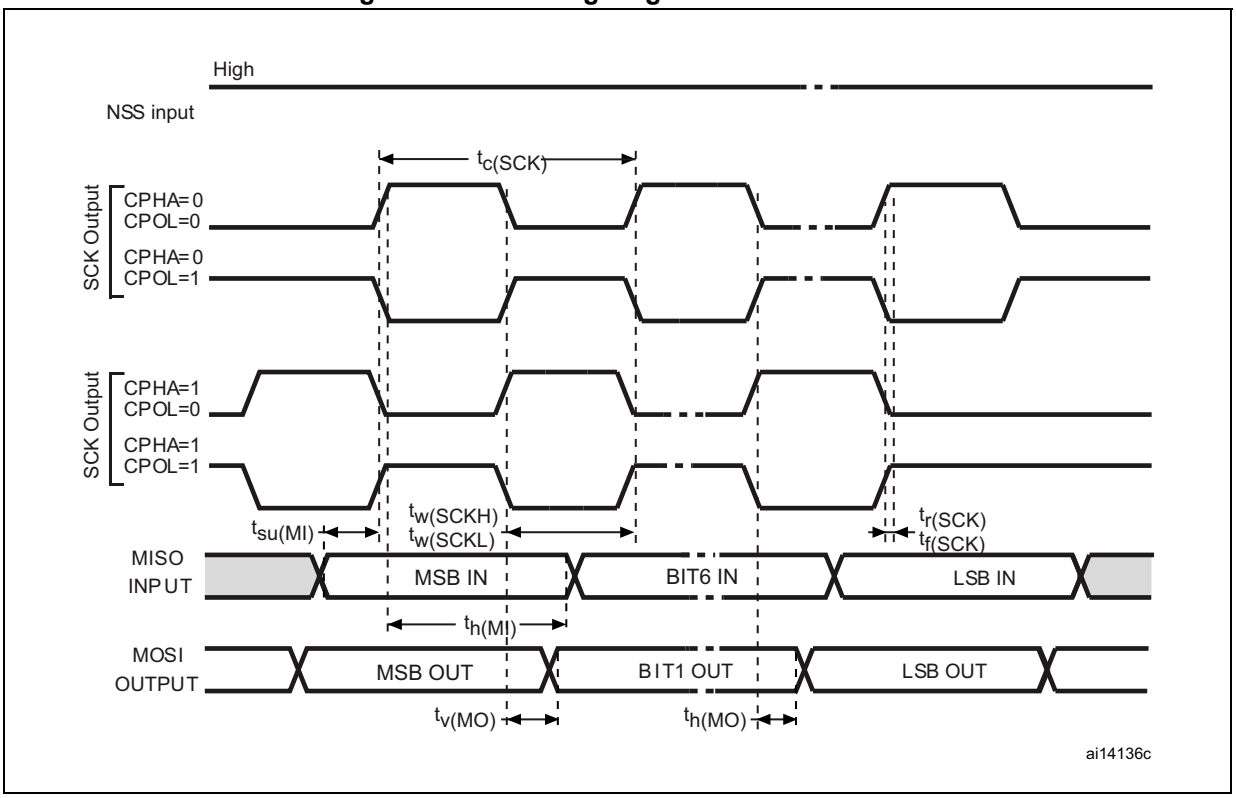


Figure 70. NAND controller waveforms for common memory read access

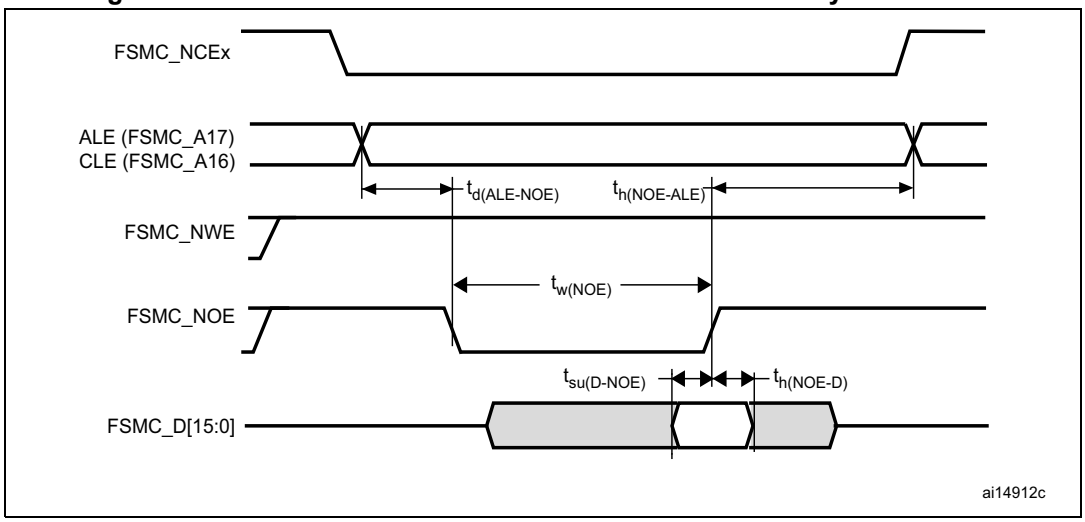


Figure 71. NAND controller waveforms for common memory write access

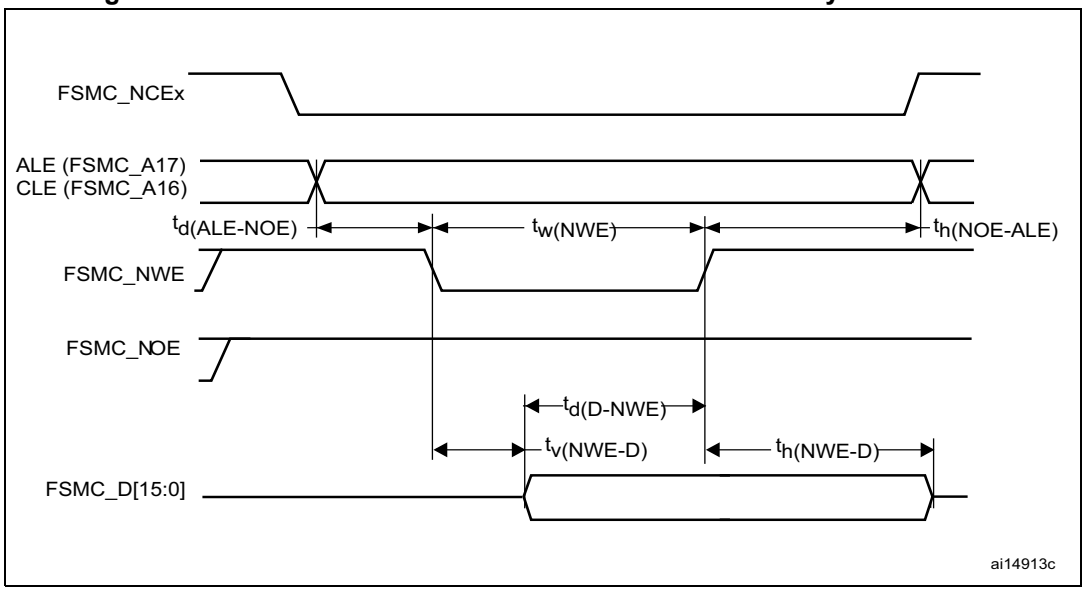


Table 85. Switching characteristics for NAND Flash read cycles(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(N0E)}$	FSMC_NOE low width	$4T_{HCLK}-0.5$	$4T_{HCLK}+3$	ns
$t_{su(D-NOE)}$	FSMC_D[15-0] valid data before FSMC_NOE high	10	-	ns
$t_{h(NOE-D)}$	FSMC_D[15-0] valid data after FSMC_NOE high	0	-	ns
$t_{d(ALE-NOE)}$	FSMC_ALE valid before FSMC_NOE low	-	$3T_{HCLK}$	ns
$t_{h(NOE-ALE)}$	FSMC_NWE high to FSMC_ALE invalid	$3T_{HCLK}-2$	-	ns

1. C_L = 30 pF.

Table 86. Switching characteristics for NAND Flash write cycles(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NWE)}$	FSMC_NWE low width	$4T_{HCLK}-1$	$4T_{HCLK}+3$	ns
$t_{v(NWE-D)}$	FSMC_NWE low to FSMC_D[15-0] valid	-	0	ns
$t_{h(NWE-D)}$	FSMC_NWE high to FSMC_D[15-0] invalid	$3T_{HCLK}-2$	-	ns
$t_{d(D-NWE)}$	FSMC_D[15-0] valid before FSMC_NWE high	$5T_{HCLK}-3$	-	ns
$t_{d(ALE-NWE)}$	FSMC_ALE valid before FSMC_NWE low	-	$3T_{HCLK}$	ns
$t_{h(NWE-ALE)}$	FSMC_NWE high to FSMC_ALE invalid	$3T_{HCLK}-2$	-	ns

1. C_L = 30 pF.

5.3.27 Camera interface (DCMI) timing specifications

Unless otherwise specified, the parameters given in *Table 87* for DCMI are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage summarized in *Table 13*, with the following configuration:

- PCK polarity: falling
- VSYNC and HSYNC polarity: high
- Data format: 14 bits

Figure 72. DCMI timing diagram

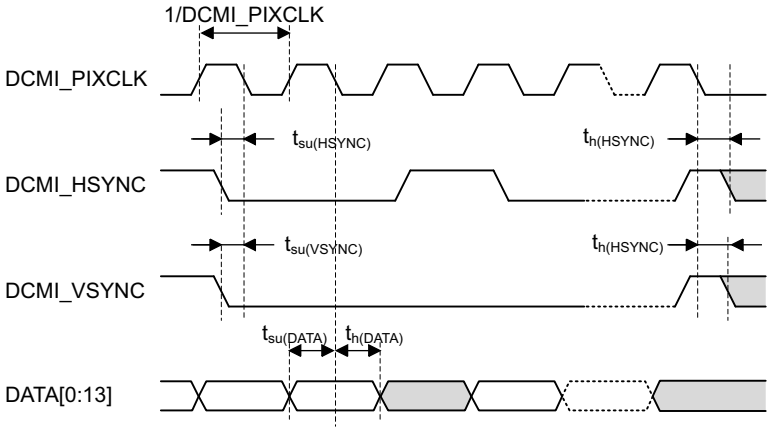


Table 87. DCMI characteristics(1)

Symbol	Parameter	Min	Max	Unit
	Frequency ratio DCMI_PIXCLK/f_{HCLK}	-	0.4	
DCMI_PIXCLK	Pixel clock input	-	54	MHz
D_{pixel}	Pixel clock input duty cycle	30	70	%

Table 87. DCMI characteristics(1) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{su(DATA)}$	Data input setup time	2.5	-	ns
$t_{h(DATA)}$	Data hold time	1	-	
$t_{su(HSYNC)}$, $t_{su(VSYNC)}$	HSYNC/VSYNC input setup time	2	-	
$t_{h(HSYNC)}$, $t_{h(VSYNC)}$	HSYNC/VSYNC input hold time	0.5	-	

1. Guaranteed by characterization.

5.3.28 SD/SDIO MMC card host interface (SDIO) characteristics

Unless otherwise specified, the parameters given in *Table 88* are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 14* with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 5.3.16: I/O port characteristics* for more details on the input/output characteristics.

Figure 73. SDIO high-speed mode

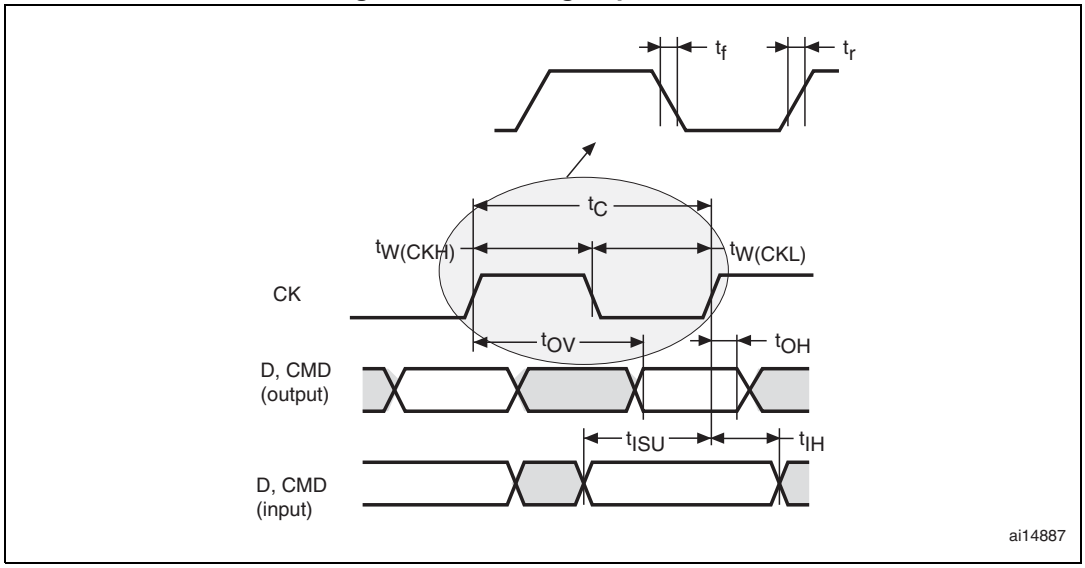
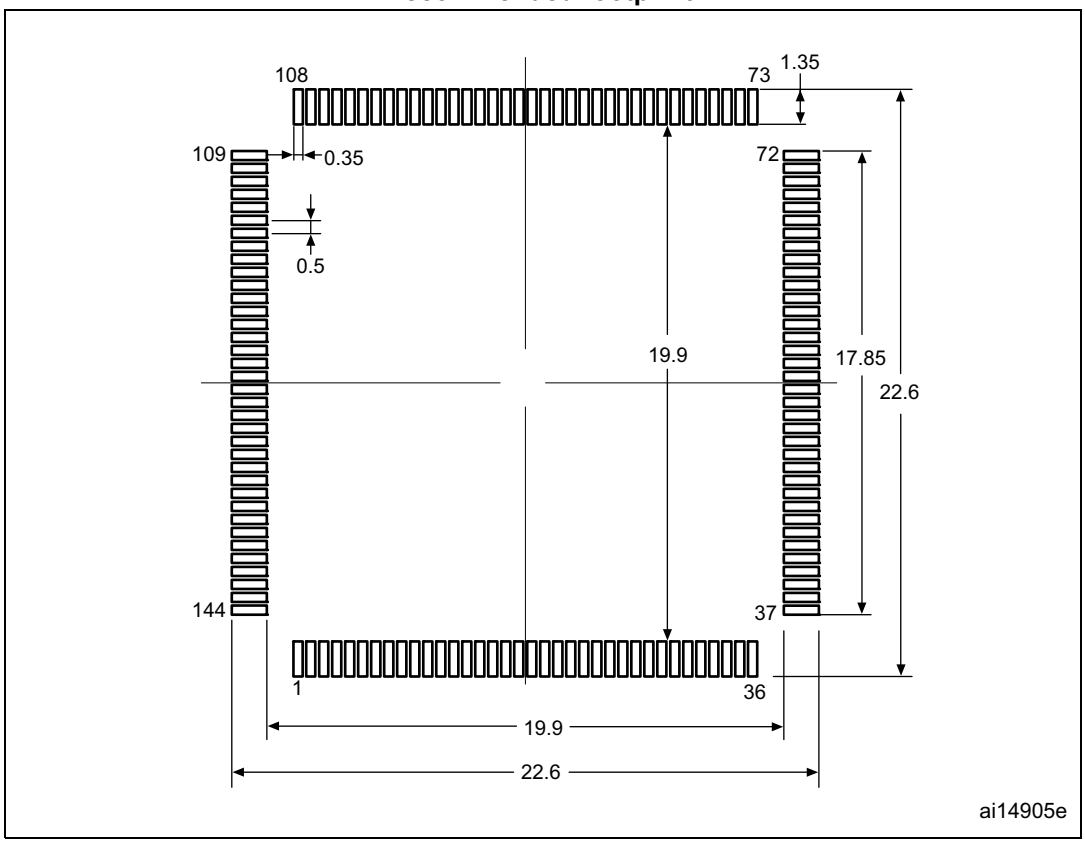


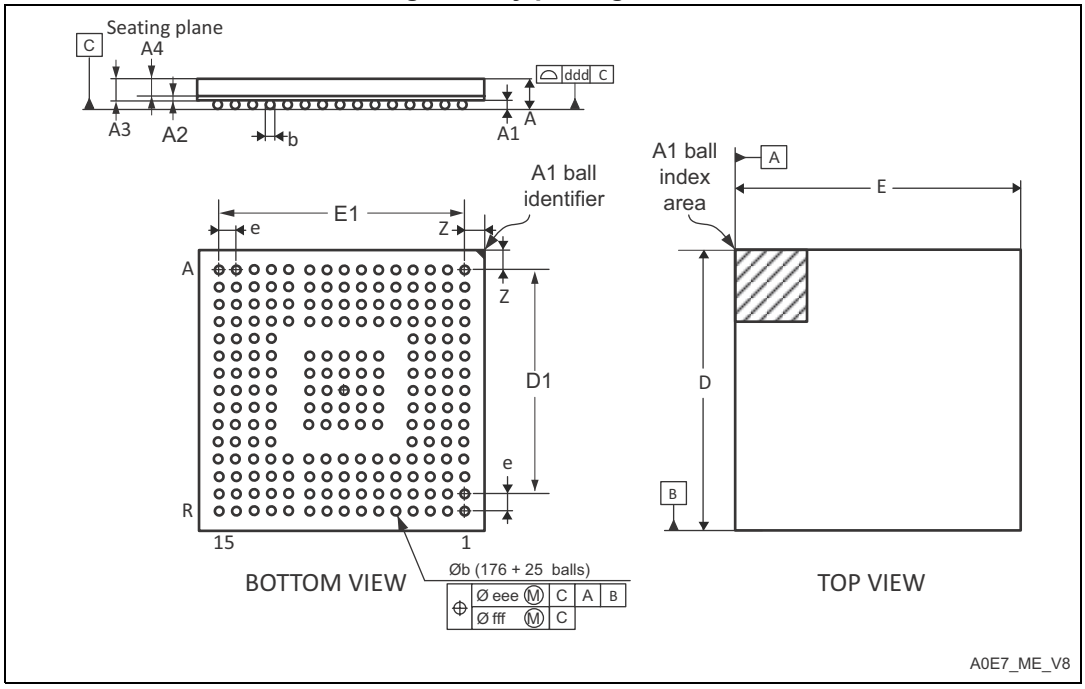
Figure 85. LQFP144 - 144-pin,20 x 20 mm low-profile quad flat package recommended footprint



1. Dimensions are in millimeters.

6.5 UFBGA176+25 package information

Figure 87. UFBGA176+25 ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 95. UFBGA176+25 ball, 10 × 10 × 0.65 mm pitch, ultra thin fine pitch ball grid array mechanical data

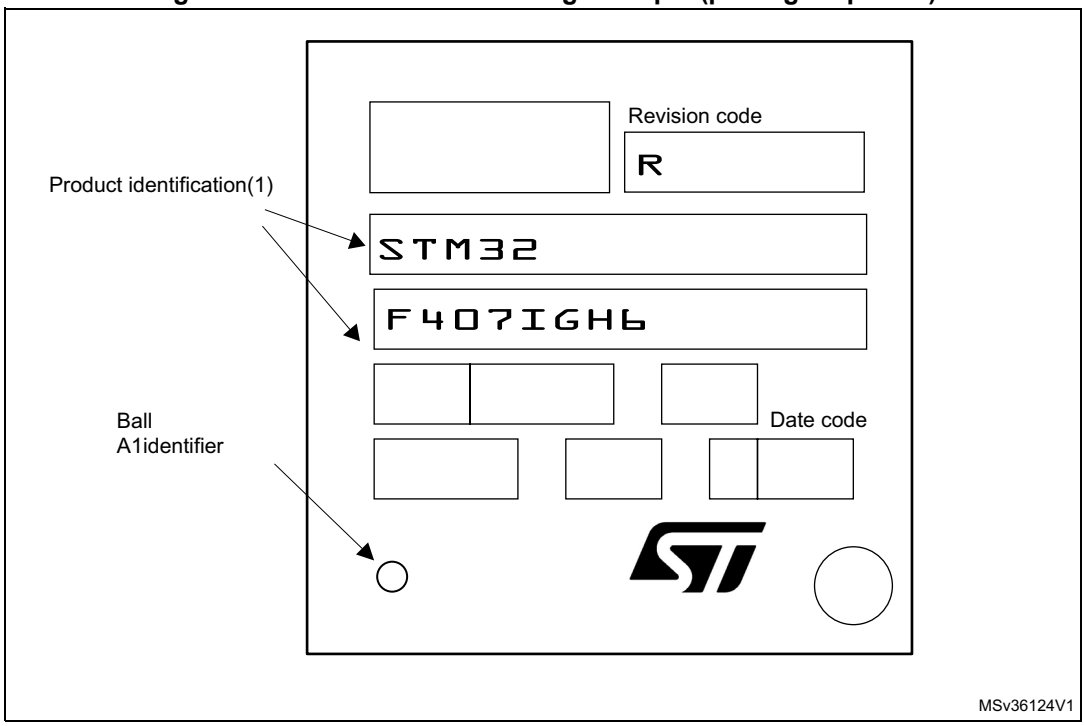
Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.130	-	-	0.0051	-
A3	-	0.450	-	-	0.0177	-
A4	-	0.320	-	-	0.0126	-
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	9.850	10.000	10.150	0.3878	0.3937	0.3996
D1	-	9.100	-	-	0.3583	-
E	9.850	10.000	10.150	0.3878	0.3937	0.3996
E1	-	9.100	-	-	0.3583	-
e	-	0.650	-	-	0.0256	-
Z	-	0.450	-	-	0.0177	-
ddd	-	-	0.080	-	-	0.0031

Device marking for UFBGA176+25

The following figure gives an example of topside marking and ball A 1 position identifier location.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

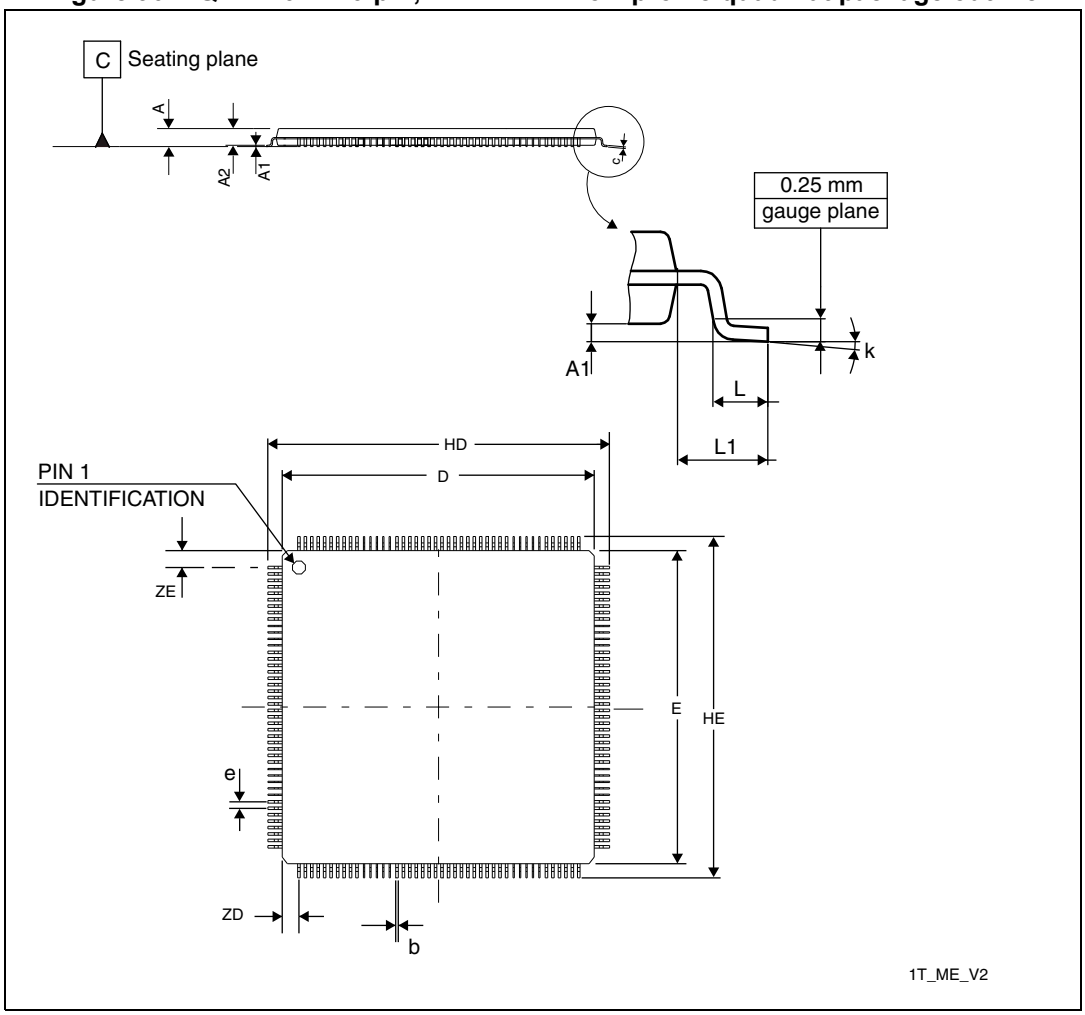
Figure 89. UFBGA176+25 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

6.6 LQFP176 package information

Figure 90. LQFP176 - 176-pin, 24 x 24 mm low profile quad flat package outline



1. Drawing is not to scale.

Table 97. LQFP176 - 176-pin, 24 x 24 mm low profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	-	1.450	0.0531	-	0.0571
b	0.170	-	0.270	0.0067	-	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	23.900	-	24.100	0.9409	-	0.9488
HD	25.900	-	26.100	1.0197	-	1.0276