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#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	168MHz
Connectivity	CANbus, I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I <sup>2</sup> S, LCD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f405rgt7

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

# 1 Introduction

This datasheet provides the description of the STM32F405xx and STM32F407xx lines of microcontrollers. For more details on the whole STMicroelectronics STM32<sup>™</sup> family, please refer to Section 2.1: Full compatibility throughout the family.

The STM32F405xx and STM32F407xx datasheet should be read in conjunction with the STM32F4xx reference manual which is available from the STMicroelectronics website *www.st.com*.

For information on the Cortex<sup>®</sup>-M4 core, please refer to the Cortex<sup>®</sup>-M4 programming manual (PM0214) available from *www.st.com*.



clock entry is available when necessary (for example if an indirectly used external oscillator fails).

Several prescalers allow the configuration of the three AHB buses, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the three AHB buses is 168 MHz while the maximum frequency of the high-speed APB domains is 84 MHz. The maximum allowed frequency of the low-speed APB domain is 42 MHz.

The devices embed a dedicated PLL (PLLI2S) which allows to achieve audio class performance. In this case, the  $I^2S$  master clock can generate all standard sampling frequencies from 8 kHz to 192 kHz.

# 2.2.13 Boot modes

At startup, boot pins are used to select one out of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART1 (PA9/PA10), USART3 (PC10/PC11 or PB10/PB11), CAN2 (PB5/PB13), USB OTG FS in Device mode (PA11/PA12) through DFU (device firmware upgrade).

# 2.2.14 **Power supply schemes**

- V<sub>DD</sub> = 1.8 to 3.6 V: external power supply for I/Os and the internal regulator (when enabled), provided externally through V<sub>DD</sub> pins.
- V<sub>SSA</sub>, V<sub>DDA</sub> = 1.8 to 3.6 V: external analog power supplies for ADC, DAC, Reset blocks, RCs and PLL. V<sub>DDA</sub> and V<sub>SSA</sub> must be connected to V<sub>DD</sub> and V<sub>SS</sub>, respectively.
- V<sub>BAT</sub> = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V<sub>DD</sub> is not present.

Refer to Figure 21: Power supply scheme for more details.

Note:  $V_{DD}/V_{DDA}$  minimum value of 1.7 V is obtained when the device operates in reduced temperature range, and with the use of an external power supply supervisor (refer to Section : Internal reset OFF).

Refer to Table 2 in order to identify the packages supporting this option.

# 2.2.15 **Power supply supervisor**

# Internal reset ON

On packages embedding the PDR\_ON pin, the power supply supervisor is enabled by holding PDR\_ON high. On all other packages, the power supply supervisor is always enabled.

The device has an integrated power-on reset (POR) / power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry. At power-on, POR/PDR is always active and ensures proper operation starting from 1.8 V. After the 1.8 V POR threshold level is reached, the option byte loading process starts, either to confirm or modify default BOR threshold levels, or to disable BOR permanently. Three BOR thresholds are available through option bytes. The device remains in reset mode when V<sub>DD</sub> is below a specified threshold, V<sub>POR/PDR</sub> or V<sub>BOR</sub>, without the need for an external reset circuit.



		Pin r	numb	er							
LQFP64	WLCSP90	LQFP100	LQFP144	UFBGA176	LQFP176	Pin name (function after reset) <sup>(1)</sup>	Pin type	I / O structure	Notes	Alternate functions	Additional functions
	D9			L4	48	BYPASS_REG	Ι	FT	-	-	-
19	E4	28	39	K4	49	V <sub>DD</sub>	S	-	1	-	_
20	J9	29	40	N4	50	PA4	I/O	TTa	(4)	SPI1_NSS / SPI3_NSS / USART2_CK / DCMI_HSYNC / OTG_HS_SOF/ I2S3_WS/ EVENTOUT	ADC12_IN4 /DAC_OUT1
21	G8	30	41	P4	51	PA5	I/O	ТТа	(4)	SPI1_SCK/ OTG_HS_ULPI_CK / TIM2_CH1_ETR/ TIM8_CH1N/ EVENTOUT	ADC12_IN5/DAC_ OUT2
22	H8	31	42	P3	52	PA6	I/O	FT	(4)	SPI1_MISO / TIM8_BKIN/TIM13_CH1 / DCMI_PIXCLK / TIM3_CH1 / TIM1_BKIN/ EVENTOUT	ADC12_IN6
23	J8	32	43	R3	53	PA7	I/O	FT	(4)	SPI1_MOSI/ TIM8_CH1N / TIM14_CH1/TIM3_CH2/ ETH_MII_RX_DV / TIM1_CH1N / ETH_RMII_CRS_DV/ EVENTOUT	ADC12_IN7
24	-	33	44	N5	54	PC4	I/O	FT	(4)	ETH_RMII_RX_D0 / ETH_MII_RX_D0/ EVENTOUT	ADC12_IN14
25	-	34	45	P5	55	PC5	I/O	FT	(4)	ETH_RMII_RX_D1 / ETH_MII_RX_D1/ EVENTOUT	ADC12_IN15
26	G7	35	46	R5	56	PB0	I/O	FT	(4)	TIM3_CH3 / TIM8_CH2N/ OTG_HS_ULPI_D1/ ETH_MII_RXD2 / TIM1_CH2N/ EVENTOUT	ADC12_IN8
27	H7	36	47	R4	57	PB1	I/O	FT	(4)	TIM3_CH4 / TIM8_CH3N/ OTG_HS_ULPI_D2/ ETH_MII_RXD3 / TIM1_CH3N/ EVENTOUT	ADC12_IN9
28	J7	37	48	M6	58	PB2/BOOT1 (PB2)	I/O	FT	-	EVENTOUT	-



67/202

DocID022152 Rev 8

						Tab	ole 9. Alt	ernate fu	unction m	apping	(contin	ued)					
		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13		
P	ort	SYS	TIM1/2	TIM3/4/5	TIM8/9/10 /11	I2C1/2/3	SPI1/SPI2/ I2S2/I2S2e xt	SPI3/I2Sext /I2S3	USART1/2/3/ I2S3ext	UART4/5/ USART6	CAN1/2 TIM12/13/ 14	OTG_FS/ OTG_HS	ETH	FSMC/SDIO /OTG_FS	DCMI	AF14	AF15
	PF0	-	-	-	-	I2C2_SDA	-	-	-	-	-	-	-	FSMC_A0	-	-	EVENTOUT
	PF1	-	-	-	-	I2C2_SCL	-	-	-	-	-	-	-	FSMC_A1	-	-	EVENTOUT
	PF2	-	-	-	-	I2C2_ SMBA	-	-	-	-	-	-	-	FSMC_A2	-	-	EVENTOUT
	PF3	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A3	-	-	EVENTOUT
	PF4	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A4	-	-	EVENTOUT
	PF5	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A5	-	-	EVENTOUT
	PF6	-	-	-	TIM10_CH1	-	-	-	-	-	-	-	-	FSMC_NIORD	-	-	EVENTOUT
Port F	PF7	-	-	-	TIM11_CH1	-	-	-	-	-	-	-	-	FSMC_NREG	-	-	EVENTOUT
, or the	PF8	-	-	-	-	-	-	-	-	-	TIM13_CH1	-	-	FSMC_ NIOWR	-	-	EVENTOUT
	PF9	-	-	-	-	-	-	-	-	-	TIM14_CH1	-	-	FSMC_CD	-	-	EVENTOUT
	PF10	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_INTR	-	-	EVENTOUT
	PF11	-	-	-	-	-	-	-	-	-	-	-	-		DCMI_D12	-	EVENTOUT
	PF12	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A6	-	-	EVENTOUT
	PF13	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A7	-	-	EVENTOUT
	PF14	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A8	-	-	EVENTOUT
	PF15	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A9	-	-	EVENTOUT

Pinouts and pin description

5

# 5.1.6 Power supply scheme



#### Figure 21. Power supply scheme

1. Each power supply pair must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

- 2. To connect BYPASS\_REG and PDR\_ON pins, refer to Section 2.2.16: Voltage regulator and Table 2.2.15: Power supply supervisor.
- 3. The two 2.2  $\mu F$  ceramic capacitors should be replaced by two 100 nF decoupling capacitors when the voltage regulator is OFF.
- 4. The 4.7  $\mu F$  ceramic capacitor must be connected to one of the  $V_{DD}$  pin.
- 5.  $V_{DDA}=V_{DD}$  and  $V_{SSA}=V_{SS}$ .



Symbol	Ratings	Max.	Unit
I <sub>VDD</sub>	Total current into V <sub>DD</sub> power lines (source) <sup>(1)</sup>	240	
I <sub>VSS</sub>	Total current out of $V_{SS}$ ground lines (sink) <sup>(1)</sup>	240	
	Output current sunk by any I/O and control pin	25	
IO	Output current source by any I/Os and control pin	25	mA
(2)	Injected current on five-volt tolerant I/O <sup>(3)</sup>	-5/+0	
I <sub>INJ</sub> (PIN)	Injected current on any other pin <sup>(4)</sup>	±5	
$\Sigma I_{\rm INJ(PIN)}^{(4)}$	Total injected current (sum of all I/O and control pins) <sup>(5)</sup>	±25	

#### Table 12. Current characteristics

1. All main power ( $V_{DD}$ ,  $V_{DDA}$ ) and ground ( $V_{SS}$ ,  $V_{SSA}$ ) pins must always be connected to the external power supply, in the permitted range.

2. Negative injection disturbs the analog performance of the device. See note in Section 5.3.21: 12-bit ADC characteristics.

3. Positive injection is not possible on these I/Os. A negative injection is induced by  $V_{IN} < V_{SS}$ .  $I_{INJ(PIN)}$  must never be exceeded. Refer to *Table 11* for the values of the maximum allowed input voltage.

4. A positive injection is induced by  $V_{IN}$  >  $V_{DD}$  while a negative injection is induced by  $V_{IN}$  <  $V_{SS}$ .  $I_{INJ(PIN)}$  must never be exceeded. Refer to *Table 11* for the values of the maximum allowed input voltage.

5. When several inputs are submitted to a current injection, the maximum  $\Sigma I_{INJ(PIN)}$  is the absolute sum of the positive and negative injected currents (instantaneous values).

#### Table 13. Thermal characteristics

Symbol	Ratings	Value	Unit
T <sub>STG</sub>	Storage temperature range	–65 to +150	°C
TJ	Maximum junction temperature	125	°C

# 5.3 Operating conditions

# 5.3.1 General operating conditions

#### Table 14. General operating conditions

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
f <sub>HCLK</sub>	Internal AHR clock frequency	VOS bit in PWR_CR register = $0^{(1)}$	0	-	144	N 41 1-
	Internal AITB Clock frequency	VOS bit in PWR_CR register= 1	0	-	168	
f <sub>PCLK1</sub>	Internal APB1 clock frequency	-	0	-	42	
f <sub>PCLK2</sub>	Internal APB2 clock frequency	-	0	-	84	
V <sub>DD</sub>	Standard operating voltage	-	1.8 <sup>(2)</sup>	-	3.6	V
V(3)(4)	Analog operating voltage (ADC limited to 1.2 M samples)	Must be the same potential as	1.8 <sup>(2)</sup>	-	2.4	v
V <sub>DDA</sub> <sup>(3)(4)</sup>	Analog operating voltage (ADC limited to 1.4 M samples)	V <sub>DD</sub> <sup>(5)</sup>	2.4	-	3.6	
V <sub>BAT</sub>	Backup operating voltage	-	1.65	-	3.6	V



# 5.3.5 Embedded reset and power control block characteristics

The parameters given in *Table 19* are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in *Table 14*.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
		PLS[2:0]=000 (rising edge)	2.09	2.14	2.19	V
		PLS[2:0]=000 (falling edge)	1.98	2.04	2.08	V
		PLS[2:0]=001 (rising edge)	2.23	2.30	2.37	V
		PLS[2:0]=001 (falling edge)	2.13	2.19	2.25	V
		PLS[2:0]=010 (rising edge)	2.39	2.45	2.51	V
		PLS[2:0]=010 (falling edge)	2.29	2.35	2.39	V
		PLS[2:0]=011 (rising edge)	2.54	2.60	2.65	V
V <sub>PVD</sub>	Programmable voltage detector level selection	PLS[2:0]=011 (falling edge)	2.44	2.51	2.56	V
		PLS[2:0]=100 (rising edge)	2.70	2.76	2.82	V
		PLS[2:0]=100 (falling edge)	2.59	2.66	2.71	V
		PLS[2:0]=101 (rising edge)	2.86	2.93	2.99	V
		PLS[2:0]=101 (falling edge)	2.65	2.84	2.92	V
		PLS[2:0]=110 (rising edge)	2.96	3.03	3.10	V
		PLS[2:0]=110 (falling edge)	2.85	2.93	2.99	V
		PLS[2:0]=111 (rising edge)	3.07	3.14	3.21	V
		PLS[2:0]=111 (falling edge)	2.95	3.03	3.09	V
V <sub>PVDhyst</sub> <sup>(1)</sup>	PVD hysteresis	-	-	100	-	mV
V	Power-on/power-down	Falling edge	1.60	1.68	1.76	V
Y POR/PDR	reset threshold	Rising edge	1.64	1.72	1.80	V
V <sub>PDRhyst</sub> <sup>(1)</sup>	PDR hysteresis	-	-	40	-	mV
Vacat	Brownout level 1	Falling edge	2.13	2.19	2.24	V
¥BOR1	threshold	Rising edge	2.23	2.29	2.33	V

Table 19. Embedded reset and	power control block characteristics
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57



Figure 26. Typical current consumption versus temperature, Run mode, code with data processing running from Flash (ART accelerator OFF) or RAM, and peripherals OFF

# Figure 27. Typical current consumption versus temperature, Run mode, code with data processing running from Flash (ART accelerator OFF) or RAM, and peripherals ON





				Тур	Max	к <sup>(1)</sup>	Unit
Symbol	Parameter	Conditions	f <sub>HCLK</sub>	T <sub>A</sub> = 25 °C	T <sub>A</sub> = 85 °C	T <sub>A</sub> = 105 °C	
			168 MHz	59	77	84	
			144 MHz	46	61	67	
			120 MHz	38	53	60	
			90 MHz	30	44	51	
		(2)	60 MHz	20	34	41	
		External clock <sup>(2)</sup> , all peripherals enabled <sup>(3)</sup>	30 MHz	11	24	31	
			25 MHz	8	21	28	
	Supply current in		16 MHz	6	18	25	- mA
			8 MHz	3	16	23	
			4 MHz	2	15	22	
1			2 MHz	2	14	21	
DD	Sleep mode		168 MHz	12	27	35	
			144 MHz	9	22	29	
			120 MHz	8	20	28	
			90 MHz	7	19	26	
			60 MHz	5	17	24	
		External clock <sup>(2)</sup> , all peripherals disabled	30 MHz	3	16	23	
			25 MHz	2	15	22	-
			16 MHz	2	14	21	
			8 MHz	1	14	21	
			4 MHz	1	13	21	
			2 MHz	1	13	21	

Table 22. Ty	ypical and	maximum	current	consum	ption in	Sleep	mode
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1. Guaranteed by characterization, tested in production at  $V_{DD}$  max and  $f_{HCLK}$  max with peripherals enabled.

2. External clock is 4 MHz and PLL is on when  $f_{HCLK}$  > 25 MHz.

3. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC\_CR2 register).



Symbol	Parameter	Conditions	Min <sup>(1)</sup>	Тур	Max <sup>(1)</sup>	Unit
t <sub>prog</sub>	Double word programming		-	16	100 <sup>(2)</sup>	μs
t <sub>ERASE16KB</sub>	Sector (16 KB) erase time	T <sub>A</sub> = 0 to +40 °C	-	230	-	
t <sub>ERASE64KB</sub>	Sector (64 KB) erase time	V <sub>DD</sub> = 3.3 V	-	490	-	ms
t <sub>ERASE128KB</sub>	Sector (128 KB) erase time	V <sub>PP</sub> = 8.5 V	-	875	-	
t <sub>ME</sub>	Mass erase time		-	6.9	-	s
V <sub>prog</sub>	Programming voltage	-	2.7	-	3.6	V
V <sub>PP</sub>	V <sub>PP</sub> voltage range	-	7	-	9	V
I <sub>PP</sub>	Minimum current sunk on the $V_{\rm PP}$ pin	-	10	-	-	mA
t <sub>VPP</sub> <sup>(3)</sup>	Cumulative time during which V <sub>PP</sub> is applied	-	-	-	1	hour

able 41. Flash memo	y programming	with \	
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1. Guaranteed by design.

2. The maximum programming time is measured after 100K erase operations.

3.  $V_{PP}$  should only be connected during programming/erasing.

		Osmalikismo	Value	
Symbol P	Parameter	Conditions	Min <sup>(1)</sup>	Unit
N <sub>END</sub>	Endurance	$T_A = -40$ to +85 °C (6 suffix versions) $T_A = -40$ to +105 °C (7 suffix versions)	10	kcycles
		1 kcycle <sup>(2)</sup> at T <sub>A</sub> = 85 °C	30	
t <sub>RET</sub>	Data retention	1 kcycle <sup>(2)</sup> at T <sub>A</sub> = 105 °C	10	Years
		10 kcycles <sup>(2)</sup> at T <sub>A</sub> = 55 °C	20	

#### Table 42. Flash memory endurance and data retention

1. Guaranteed by characterization.

2. Cycling performed over the whole temperature range.

# 5.3.13 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

# Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- Electrostatic discharge (ESD) (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- FTB: A burst of fast transient voltage (positive and negative) is applied to V<sub>DD</sub> and V<sub>SS</sub> through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.



# Static latchup

Two complementary static tests are required on six parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latchup standard.

Table	46	Electrical	sensitivities
Table	τυ.	LICCUICAI	30113111411103

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	$T_A = +105 \text{ °C conforming to JESD78A}$	II level A

# 5.3.15 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below  $V_{SS}$  or above  $V_{DD}$  (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

## Functional susceptibilty to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of 5  $\mu$ A/+0  $\mu$ A range), or other functional failure (for example reset, oscillator frequency deviation).

Negative induced leakage current is caused by negative injection and positive induced leakage current by positive injection.

The test results are given in Table 47.



# SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 55* for SPI are derived from tests performed under the ambient temperature,  $f_{PCLKx}$  frequency and  $V_{DD}$  supply voltage conditions summarized in *Table 14* with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 V<sub>DD</sub>

Refer to Section 5.3.16: I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
4	fSCK SPI clock frequency 1/t <sub>c(SCK)</sub>	Master mode, SPI1, 2.7V < V <sub>DD</sub> < 3.6V	_	-	42	MHz
ISCK		Slave mode, SPI1, 2.7V < V <sub>DD</sub> < 3.6V			42	
1/t <sub>c(SCK)</sub>		Master mode, SPI1/2/3, 1.7V < V <sub>DD</sub> < 3.6V		-	21	
		Slave mode, SPI1/2/3, 1.7V < V <sub>DD</sub> < 3.6V			21	
Duty(SCK)	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%

# Table 55. SPI dynamic characteristics<sup>(1)</sup>





Figure 42. I<sup>2</sup>S slave timing diagram (Philips protocol)

LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.



## Figure 43. I<sup>2</sup>S master timing diagram (Philips protocol)<sup>(1)</sup>

1. Guaranteed by characterization.

2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.



#### Equation 1: R<sub>AIN</sub> max formula

$$R_{AIN} = \frac{(k - 0.5)}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. N = 12 (from 12-bit resolution) and k is the number of sampling periods defined in the ADC\_SMPR1 register.

Symbol	Parameter	Test conditions	Тур	Max <sup>(1)</sup>	Unit
ET	Total unadjusted error	fpouvo = 60 MHz	±2	±5	
EO	Offset error		±1.5	±2.5	
EG	Gain error	$f_{ADC} = 30 \text{ MHz}, R_{AIN} < 10 \text{ k}\Omega$	±1.5	±3	LSB
ED	Differential linearity error	$V_{DDA} = 1.8^{(2)}$ to 3.6 V	±1	±2	
EL	Integral linearity error		±1.5	±3	

Table 68. A	DC accurac	;y at f <sub>ADC</sub> :	= 30 MHz
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1. Guaranteed by characterization.

 V<sub>DD</sub>/V<sub>DDA</sub> minimum value of 1.7 V is obtained when the device operates in reduced temperature range, and with the use of an external power supply supervisor (refer to Section : Internal reset OFF).

Note:

te: ADC accuracy vs. negative injection current: injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents. Any positive injection current within the limits specified for I<sub>INJ(PIN)</sub> and SI<sub>INJ(PIN)</sub> in Section 5.3.16 does not affect the ADC accuracy.







- See also Table 68. 1.
- 2. Example of an actual transfer curve.
- Ideal transfer curve. 3.
- 4. End point correlation line.
- $E_T$  = Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves. 5. EG = Offset Error: deviation between the first actual transition and the first ideal one. EG = Gain Error: deviation between the last ideal transition and the last actual one.
  - ED = Differential Linearity Error: maximum deviation between actual steps and the ideal one.

EL = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.





- Refer to Table 67 for the values of  $\mathsf{R}_{AIN},\,\mathsf{R}_{ADC}\,\text{and}\,\mathsf{C}_{ADC}.$ 1.
- $C_{parasitic}$  represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 5 pF). A high  $C_{parasitic}$  value downgrades conversion accuracy. To remedy this,  $f_{ADC}$  should be reduced. 2.





Figure 53. 12-bit buffered /non-buffered DAC

 The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC\_CR register.

# 5.3.26 FSMC characteristics

Unless otherwise specified, the parameters given in *Table 75* to *Table 86* for the FSMC interface are derived from tests performed under the ambient temperature,  $f_{HCLK}$  frequency and  $V_{DD}$  supply voltage conditions summarized in *Table 14*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5V<sub>DD</sub>

Refer to Section Section 5.3.16: I/O port characteristics for more details on the input/output characteristics.

#### Asynchronous waveforms and timings

*Figure 54* through *Figure 57* represent asynchronous waveforms and *Table 75* through *Table 78* provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- AddressSetupTime = 1
- AddressHoldTime = 0x1
- DataSetupTime = 0x1
- BusTurnAroundDuration = 0x0

In all timing tables, the  $T_{\text{HCLK}}$  is the HCLK clock period.





Symbol	Parameter	Min	Мах	Unit
t <sub>w(CLK)</sub>	FSMC_CLK period	2T <sub>HCLK</sub>	-	ns
t <sub>d(CLKL-NExL)</sub>	FSMC_CLK low to FSMC_NEx low (x=02)	-	0	ns
t <sub>d(CLKL-NExH)</sub>	FSMC_CLK low to FSMC_NEx high (x= 02)	2	-	ns
t <sub>d(CLKL-NADVL)</sub>	FSMC_CLK low to FSMC_NADV low	-	2	ns
t <sub>d(CLKL-NADVH)</sub>	FSMC_CLK low to FSMC_NADV high	2	-	ns
t <sub>d(CLKL-AV)</sub>	FSMC_CLK low to FSMC_Ax valid (x=1625)	-	0	ns
t <sub>d(CLKL-AIV)</sub>	FSMC_CLK low to FSMC_Ax invalid (x=1625)	0	-	ns
t <sub>d(CLKL-NOEL)</sub>	FSMC_CLK low to FSMC_NOE low	-	0	ns
t <sub>d(CLKL-NOEH)</sub>	FSMC_CLK low to FSMC_NOE high	2	-	ns
t <sub>d(CLKL-ADV)</sub>	FSMC_CLK low to FSMC_AD[15:0] valid	-	4.5	ns
t <sub>d(CLKL-ADIV)</sub>	FSMC_CLK low to FSMC_AD[15:0] invalid	0	-	ns
t <sub>su(ADV-CLKH)</sub>	FSMC_A/D[15:0] valid data before FSMC_CLK high	6	-	ns
t <sub>h(CLKH-ADV)</sub>	FSMC_A/D[15:0] valid data after FSMC_CLK high	0	-	ns
t <sub>su(NWAIT-CLKH)</sub>	FSMC_NWAIT valid before FSMC_CLK high	4	-	ns
t <sub>h(CLKH-NWAIT)</sub>	FSMC_NWAIT valid after FSMC_CLK high	0	-	ns

Table 79. Synchronous multiplexed NOR/PSRAM read timings<sup>(1)(2)</sup>

1. C<sub>L</sub> = 30 pF.

2. Guaranteed by characterization.







1. Dimensions are in millimeters.



### **Device marking for LQFP176**

The following figure gives an example of topside marking and pin 1 position identifier location.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.



Figure 92. LQFP176 marking example (package top view)

 Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.



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