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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	168MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f405rgt7tr

2 Description

The STM32F405xx and STM32F407xx family is based on the high-performance ARM® Cortex®-M4 32-bit RISC core operating at a frequency of up to 168 MHz. The Cortex-M4 core features a Floating point unit (FPU) single precision which supports all ARM single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The STM32F405xx and STM32F407xx family incorporates high-speed embedded memories (Flash memory up to 1 Mbyte, up to 192 Kbytes of SRAM), up to 4 Kbytes of backup SRAM, and an extensive range of enhanced I/Os and peripherals connected to two APB buses, three AHB buses and a 32-bit multi-AHB bus matrix.

All devices offer three 12-bit ADCs, two DACs, a low-power RTC, twelve general-purpose 16-bit timers including two PWM timers for motor control, two general-purpose 32-bit timers. a true random number generator (RNG). They also feature standard and advanced communication interfaces.

- Up to three I^2Cs
- Three SPIs, two I^2Ss full duplex. To achieve audio class accuracy, the I2S peripherals can be clocked via a dedicated internal audio PLL or via an external clock to allow synchronization.
- Four USARTs plus two UARTs
- An USB OTG full-speed and a USB OTG high-speed with full-speed capability (with the ULPI),
- Two CANs
- An SDIO/MMC interface
- Ethernet and the camera interface available on STM32F407xx devices only.

New advanced peripherals include an SDIO, an enhanced flexible static memory control (FSMC) interface (for devices offered in packages of 100 pins and more), a camera interface for CMOS sensors. Refer to *Table 2: STM32F405xx and STM32F407xx: features and peripheral counts* for the list of peripherals available on each part number.

The STM32F405xx and STM32F407xx family operates in the –40 to +105 °C temperature range from a 1.8 to 3.6 V power supply. The supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range using an external power supply supervisor: refer to *Section : Internal reset OFF*. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F405xx and STM32F407xx family offers devices in various packages ranging from 64 pins to 176 pins. The set of included peripherals changes with the device chosen.

These features make the STM32F405xx and STM32F407xx microcontroller family suitable for a wide range of applications:

- Motor drive and application control
- Medical equipment
- Industrial applications: PLC, inverters, circuit breakers
- Printers, and scanners
- Alarm systems, video intercom, and HVAC
- Home audio appliances

Figure 2. Compatible board design STM32F10xx/STM32F2/STM32F40xxx for LQFP100 package

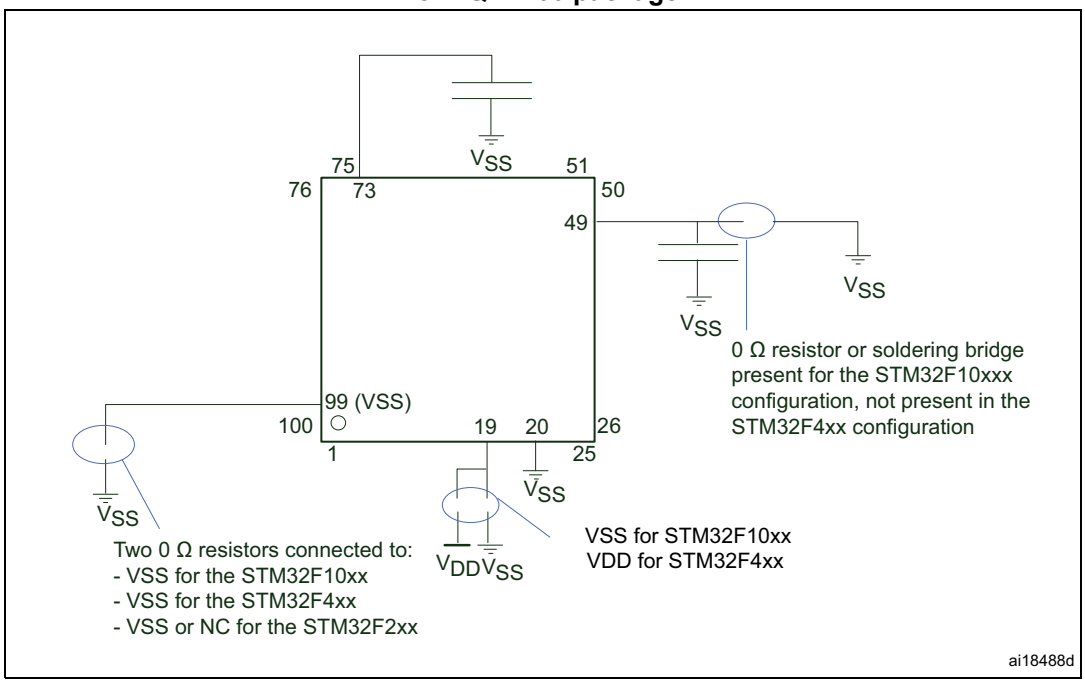
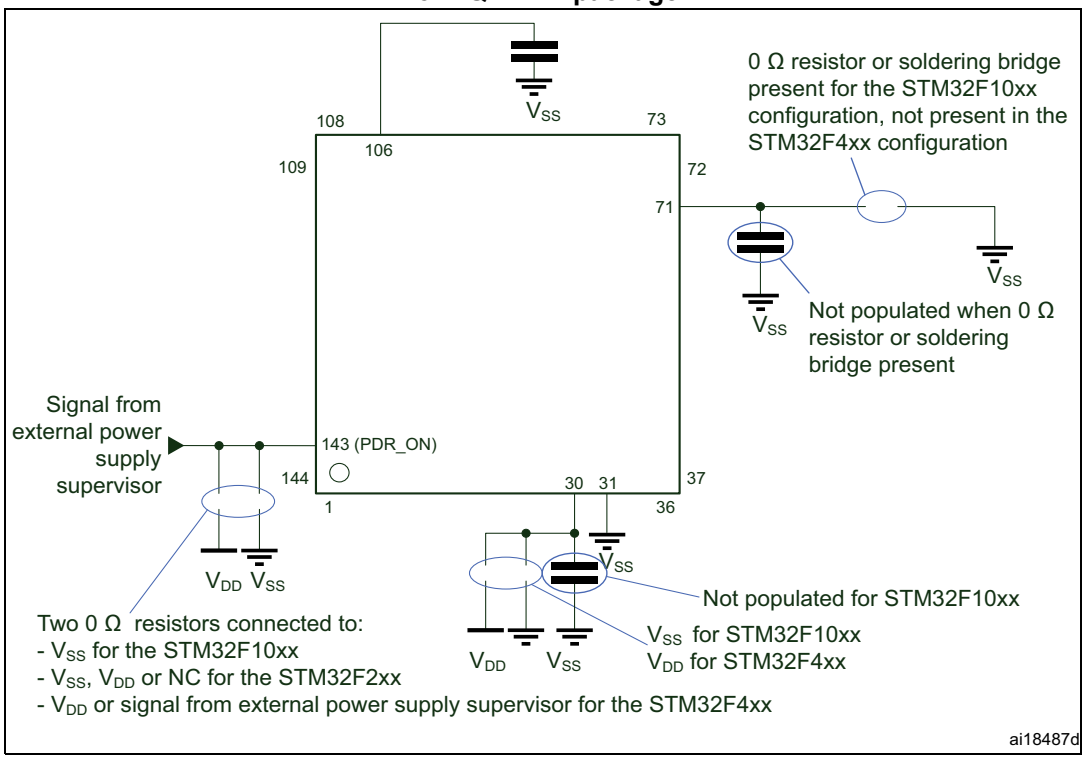


Figure 3. Compatible board design between STM32F10xx/STM32F2/STM32F40xxx for LQFP144 package



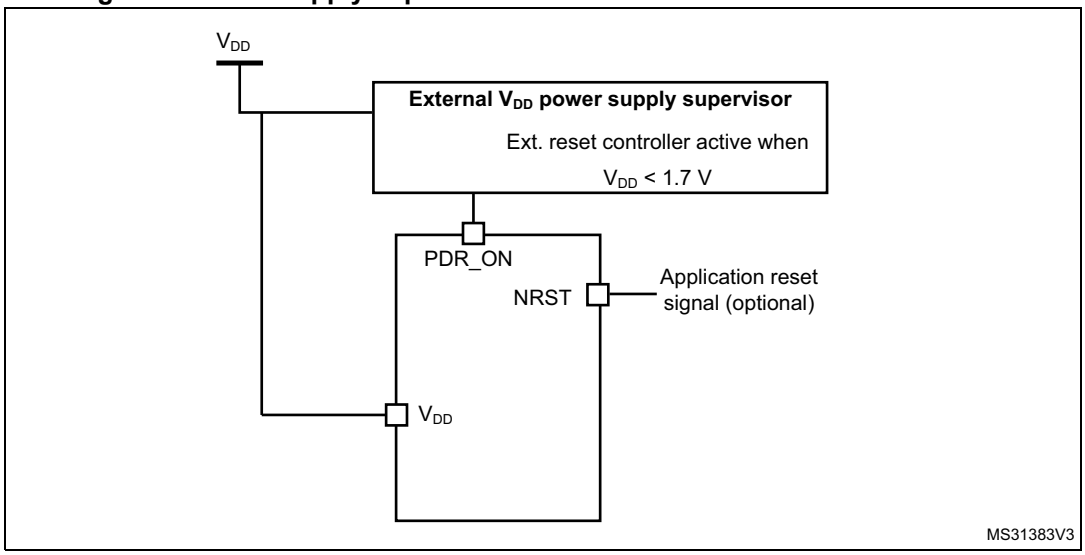
The device also features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

Internal reset OFF

This feature is available only on packages featuring the PDR_ON pin. The internal power-on reset (POR) / power-down reset (PDR) circuitry is disabled with the PDR_ON pin.

An external power supply supervisor should monitor V_{DD} and should maintain the device in reset mode as long as V_{DD} is below a specified threshold. PDR_ON should be connected to this external power supply supervisor. Refer to *Figure 7: Power supply supervisor interconnection with internal reset OFF*.

Figure 7. Power supply supervisor interconnection with internal reset OFF



1. PDR = 1.7 V for reduce temperature range; PDR = 1.8 V for all temperature range.

The V_{DD} specified threshold, below which the device must be maintained under reset, is 1.8 V (see *Figure 7*). This supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range.

A comprehensive set of power-saving mode allows to design low-power applications.

When the internal reset is OFF, the following integrated features are no more supported:

- The integrated power-on reset (POR) / power-down reset (PDR) circuitry is disabled
- The brownout reset (BOR) circuitry is disabled
- The embedded programmable voltage detector (PVD) is disabled
- V_{BAT} functionality is no more available and V_{BAT} pin should be connected to V_{DD}

All packages, except for the LQFP64 and LQFP100, allow to disable the internal reset through the PDR_ON signal.

Table 7. STM32F40xxx pin and ball definitions (continued)

Pin number						Pin name (function after reset)[1]	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP64	WLCSP90	LQFP100	LQFP144	UFBGA176	LQFP176						
-	-	-	49	R6	59	PF11	I/O	FT	-	DCMI_D12/ EVENTOUT	-
-	-	-	50	P6	60	PF12	I/O	FT	-	FSMC_A6/ EVENTOUT	-
-	-	-	51	M8	61	V_{SS}	S	-	-	-	-
-	-	-	52	N8	62	V_{DD}	S	-	-	-	-
-	-	-	53	N6	63	PF13	I/O	FT	-	FSMC_A7/ EVENTOUT	-
-	-	-	54	R7	64	PF14	I/O	FT	-	FSMC_A8/ EVENTOUT	-
-	-	-	55	P7	65	PF15	I/O	FT	-	FSMC_A9/ EVENTOUT	-
-	-	-	56	N7	66	PG0	I/O	FT	-	FSMC_A10/ EVENTOUT	-
-	-	-	57	M7	67	PG1	I/O	FT	-	FSMC_A11/ EVENTOUT	-
-	G6	38	58	R8	68	PE7	I/O	FT	-	FSMC_D4/TIM1_ETR/ EVENTOUT	-
-	H6	39	59	P8	69	PE8	I/O	FT	-	FSMC_D5/ TIM1_CH1N/ EVENTOUT	-
-	J6	40	60	P9	70	PE9	I/O	FT	-	FSMC_D6/TIM1_CH1/ EVENTOUT	-
-	-	-	61	M9	71	V_{SS}	S	-	-	-	-
-	-	-	62	N9	72	V_{DD}	S	-	-	-	-
-	F6	41	63	R9	73	PE10	I/O	FT	-	FSMC_D7/TIM1_CH2N/ EVENTOUT	-
-	J5	42	64	P10	74	PE11	I/O	FT	-	FSMC_D8/TIM1_CH2/ EVENTOUT	-
-	H5	43	65	R10	75	PE12	I/O	FT	-	FSMC_D9/TIM1_CH3N/ EVENTOUT	-
-	G5	44	66	N11	76	PE13	I/O	FT	-	FSMC_D10/TIM1_CH3/ EVENTOUT	-
-	F5	45	67	P11	77	PE14	I/O	FT	-	FSMC_D11/TIM1_CH4/ EVENTOUT	-
-	G4	46	68	R11	78	PE15	I/O	FT	-	FSMC_D12/TIM1_BKIN/ EVENTOUT	-

Table 7. STM32F40xxx pin and ball definitions (continued)

Pin number						Pin name (function after reset)[1]	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP64	WLCSP90	LQFP100	LQFP144	UFBGA176	LQFP176						
-	-	60	82	M15	101	PD13	I/O	FT	-	FSMC_A18/TIM4_CH2/ EVENTOUT	-
-	-	-	83	-	102	V_{SS}	S		-	-	-
-	-	-	84	J13	103	V_{DD}	S		-	-	-
-	F2	61	85	M14	104	PD14	I/O	FT	-	FSMC_D0/TIM4_CH3/ EVENTOUT/ EVENTOUT	-
-	F1	62	86	L14	105	PD15	I/O	FT	-	FSMC_D1/TIM4_CH4/ EVENTOUT	-
-	-	-	87	L15	106	PG2	I/O	FT	-	FSMC_A12/ EVENTOUT	-
-	-	-	88	K15	107	PG3	I/O	FT	-	FSMC_A13/ EVENTOUT	-
-	-	-	89	K14	108	PG4	I/O	FT	-	FSMC_A14/ EVENTOUT	-
-	-	-	90	K13	109	PG5	I/O	FT	-	FSMC_A15/ EVENTOUT	-
-	-	-	91	J15	110	PG6	I/O	FT	-	FSMC_INT2/ EVENTOUT	-
-	-	-	92	J14	111	PG7	I/O	FT	-	FSMC_INT3 /USART6_CK/ EVENTOUT	-
-	-	-	93	H14	112	PG8	I/O	FT	-	USART6_RTS / ETH_PPS_OUT/ EVENTOUT	-
-	-	-	94	G12	113	V_{SS}	S		-	-	-
-	-	-	95	H13	114	V_{DD}	S		-	-	-
37	F3	63	96	H15	115	PC6	I/O	FT	-	I2S2_MCK / TIM8_CH1/SDIO_D6 / USART6_TX / DCMI_D0/TIM3_CH1/ EVENTOUT	-
38	E1	64	97	G15	116	PC7	I/O	FT	-	I2S3_MCK / TIM8_CH2/SDIO_D7 / USART6_RX / DCMI_D1/TIM3_CH2/ EVENTOUT	-
39	E2	65	98	G14	117	PC8	I/O	FT	-	TIM8_CH3/SDIO_D0 /TIM3_CH3/ USART6_CK / DCMI_D2/ EVENTOUT	-

Table 8. FSMC pin definition (continued)

Pins[1]	FSMC				LQFP100[2]	WLCSP90 (2)
	CF	NOR/PSRAM/ SRAM	NOR/PSRAM Mux	NAND 16 bit		
PF1	A1	A1	-	-	-	-
PF2	A2	A2	-	-	-	-
PF3	A3	A3	-	-	-	-
PF4	A4	A4	-	-	-	-
PF5	A5	A5	-	-	-	-
PF6	NIORD	-	-	-	-	-
PF7	NREG	-	-	-	-	-
PF8	NIOWR	-	-	-	-	-
PF9	CD	-	-	-	-	-
PF10	INTR	-	-	-	-	-
PF12	A6	A6	-	-	-	-
PF13	A7	A7	-	-	-	-
PF14	A8	A8	-	-	-	-
PF15	A9	A9	-	-	-	-
PG0	A10	A10	-	-	-	-
PG1		A11	-	-	-	-
PE7	D4	D4	DA4	D4	Yes	Yes
PE8	D5	D5	DA5	D5	Yes	Yes
PE9	D6	D6	DA6	D6	Yes	Yes
PE10	D7	D7	DA7	D7	Yes	Yes
PE11	D8	D8	DA8	D8	Yes	Yes
PE12	D9	D9	DA9	D9	Yes	Yes
PE13	D10	D10	DA10	D10	Yes	Yes
PE14	D11	D11	DA11	D11	Yes	Yes
PE15	D12	D12	DA12	D12	Yes	Yes
PD8	D13	D13	DA13	D13	Yes	Yes
PD9	D14	D14	DA14	D14	Yes	Yes
PD10	D15	D15	DA15	D15	Yes	Yes
PD11	-	A16	A16	CLE	Yes	Yes
PD12	-	A17	A17	ALE	Yes	Yes
PD13	-	A18	A18	-	Yes	-
PD14	D0	D0	DA0	D0	Yes	Yes
PD15	D1	D1	DA1	D1	Yes	Yes

Table 9. Alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10 /11	I2C1/2/3	SPI1/SPI2/ I2S2/I2S2ext	SPI3/I2Sext /I2S3	USART1/2/3/ I2S3ext	UART4/5/ USART6	CAN1/2 TIM12/13/ 14	OTG_FS/ OTG_HS	ETH	FSMC/SDIO /OTG_FS	DCMI		
Port C	PC0	-	-	-	-	-	-	-	-	-	-	OTG_HS_ULPI_ STP	-	-	-	-	EVENTOUT
	PC1	-	-	-	-	-	-	-	-	-	-	-	ETH_MDC	-	-	-	EVENTOUT
	PC2	-	-	-	-	-	SPI2_MISO	I2S2ext_SD	-	-	-	OTG_HS_ULPI_ DIR	ETH _MII_TXD2	-	-	-	EVENTOUT
	PC3	-	-	-	-	-	SPI2_MOSI I2S2_SD	-	-	-	-	OTG_HS_ULPI_ NXT	ETH _MII_TX_CLK	-	-	-	EVENTOUT
	PC4	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_RXD0 ETH_RMII_RXD0	-	-	-	EVENTOUT
	PC5	-	-	-	-	-	-	-	-	-	-	-	ETH _MII_RXD1 ETH _RMII_RXD1	-	-	-	EVENTOUT
	PC6	-	-	TIM3_CH1	TIM8_CH1		I2S2_MCK		-	USART6_TX	-	-	-	SDIO_D6	DCMI_D0	-	EVENTOUT
	PC7	-	-	TIM3_CH2	TIM8_CH2	-	-	I2S3_MCK	-	USART6_RX	-	-	-	SDIO_D7	DCMI_D1	-	EVENTOUT
	PC8	-	-	TIM3_CH3	TIM8_CH3	-	-	-	-	USART6_CK	-	-	-	SDIO_D0	DCMI_D2	-	EVENTOUT
	PC9	MCO2	-	TIM3_CH4	TIM8_CH4	I2C3_SDA	I2S_CKIN	-	-	-	-	-	-	SDIO_D1	DCMI_D3	-	EVENTOUT
	PC10	-	-	-	-	-	-	SPI3_SCK/ I2S3_CK	USART3_TX/	UART4_TX	-	-	-	SDIO_D2	DCMI_D8	-	EVENTOUT
	PC11	-	-	-	-	-	I2S3ext_SD	SPI3_MISO/	USART3_RX	UART4_RX	-	-	-	SDIO_D3	DCMI_D4	-	EVENTOUT
	PC12	-	-	-	-	-	-	SPI3_MOSI I2S3_SD	USART3_CK	UART5_TX	-	-	-	SDIO_CK	DCMI_D9	-	EVENTOUT
	PC13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT

Table 9. Alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/SPI2/I2S2/I2S2ext	SPI3/I2Sext/I2S3	USART1/2/3/I2S3ext	UART4/5/USART6	CAN1/2 TIM12/13/14	OTG_FS/OTG_HS	ETH	FSMC/SDIO/OTG_FS	DCMI		
Port F	PF0	-	-	-	-	I2C2_SDA	-	-	-	-	-	-	-	FSMC_A0	-	-	EVENTOUT
	PF1	-	-	-	-	I2C2_SCL	-	-	-	-	-	-	-	FSMC_A1	-	-	EVENTOUT
	PF2	-	-	-	-	I2C2_SMBA	-	-	-	-	-	-	-	FSMC_A2	-	-	EVENTOUT
	PF3	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A3	-	-	EVENTOUT
	PF4	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A4	-	-	EVENTOUT
	PF5	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A5	-	-	EVENTOUT
	PF6	-	-	-	TIM10_CH1	-	-	-	-	-	-	-	-	FSMC_NIORD	-	-	EVENTOUT
	PF7	-	-	-	TIM11_CH1	-	-	-	-	-	-	-	-	FSMC_NREG	-	-	EVENTOUT
	PF8	-	-	-	-	-	-	-	-	-	TIM13_CH1	-	-	FSMC_NIOWR	-	-	EVENTOUT
	PF9	-	-	-	-	-	-	-	-	-	TIM14_CH1	-	-	FSMC_CD	-	-	EVENTOUT
	PF10	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_INTR	-	-	EVENTOUT
	PF11	-	-	-	-	-	-	-	-	-	-	-	-		DCMI_D12	-	EVENTOUT
	PF12	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A6	-	-	EVENTOUT
	PF13	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A7	-	-	EVENTOUT
	PF14	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A8	-	-	EVENTOUT
	PF15	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A9	-	-	EVENTOUT

Table 14. General operating conditions (continued)

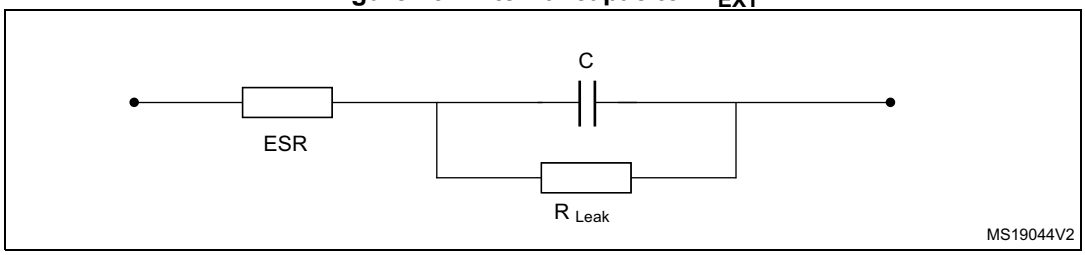
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{12}	Regulator ON: 1.2 V internal voltage on V_{CAP_1}/V_{CAP_2} pins	VOS bit in PWR_CR register = 0(1) Max frequency 144MHz	1.08	1.14	1.20	V
		VOS bit in PWR_CR register= 1 Max frequency 168MHz	1.20	1.26	1.32	V
	Regulator OFF: 1.2 V external voltage must be supplied from external regulator on V_{CAP_1}/V_{CAP_2} pins	Max frequency 144MHz	1.10	1.14	1.20	V
		Max frequency 168MHz	1.20	1.26	1.30	V
V_{IN}	Input voltage on RST and FT pins(6)	2 V ≤ V_{DD} ≤ 3.6 V	–0.3	-	5.5	V
		V_{DD} ≤ 2 V	–0.3	-	5.2	
	Input voltage on TTa pins	-	–0.3	-	V_{DDA}+ 0.3	
	Input voltage on B pin	-	-	-	5.5	
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(7)	LQFP64	-	-	435	mW
		LQFP100	-	-	465	
		LQFP144	-	-	500	
		LQFP176	-	-	526	
		UFBGA176	-	-	513	
		WLCSP90	-	-	543	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	–40	-	85	°C
		Low-power dissipation(8)	–40	-	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	–40	-	105	°C
		Low-power dissipation(8)	–40	-	125	
T_J	Junction temperature range	6 suffix version	–40	-	105	°C
		7 suffix version	–40	-	125	

1. The average expected gain in power consumption when VOS = 0 compared to VOS = 1 is around 10% for the whole temperature range, when the system clock frequency is between 30 and 144 MHz.
2. V_{DD}/V_{DDA} minimum value of 1.7 V is obtained when the device operates in reduced temperature range, and with the use of an external power supply supervisor (refer to *Section : Internal reset OFF*).
3. When the ADC is used, refer to *Table 67: ADC characteristics*.
4. If V_{REF+} pin is present, it must respect the following condition: V_{DDA}-V_{REF+} < 1.2 V.
5. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and power-down operation.
6. To sustain a voltage higher than V_{DD}+0.3, the internal pull-up and pull-down resistors must be disabled.
7. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax}.
8. In low-power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax}.

5.3.2 V_{CAP_1}/V_{CAP_2} external capacitor

Stabilization for the main regulator is achieved by connecting an external capacitor C_{EXT} to the V_{CAP_1}/V_{CAP_2} pins. C_{EXT} is specified in *Table 16*.

Figure 23. External capacitor C_{EXT}



1. Legend: ESR is the equivalent series resistance.

Table 16. V_{CAP_1}/V_{CAP_2} operating conditions(1)

Symbol	Parameter	Conditions
CEXT	Capacitance of external capacitor	2.2 µF
ESR	ESR of external capacitor	< 2 Ω

1. When bypassing the voltage regulator, the two 2.2 µF V_{CAP} capacitors are not required and should be replaced by two 100 nF decoupling capacitors.

5.3.3 Operating conditions at power-up / power-down (regulator ON)

Subject to general operating conditions for T_A.

Table 17. Operating conditions at power-up / power-down (regulator ON)

Symbol	Parameter	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	20	∞	µs/V
	V_{DD} fall time rate	20	∞	

5.3.4 Operating conditions at power-up / power-down (regulator OFF)

Subject to general operating conditions for T_A.

Table 18. Operating conditions at power-up / power-down (regulator OFF)(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	Power-up	20	∞	µs/V
	V_{DD} fall time rate	Power-down	20	∞	
t_{VCAP}	V_{CAP_1} and V_{CAP_2} rise time rate	Power-up	20	∞	
	V_{CAP_1} and V_{CAP_2} fall time rate	Power-down	20	∞	

1. To reset the internal logic at power-down, a reset must be applied on pin PA0 when V_{DD} reach below minimum value of V_{12}.

Low-speed external user clock generated from an external source

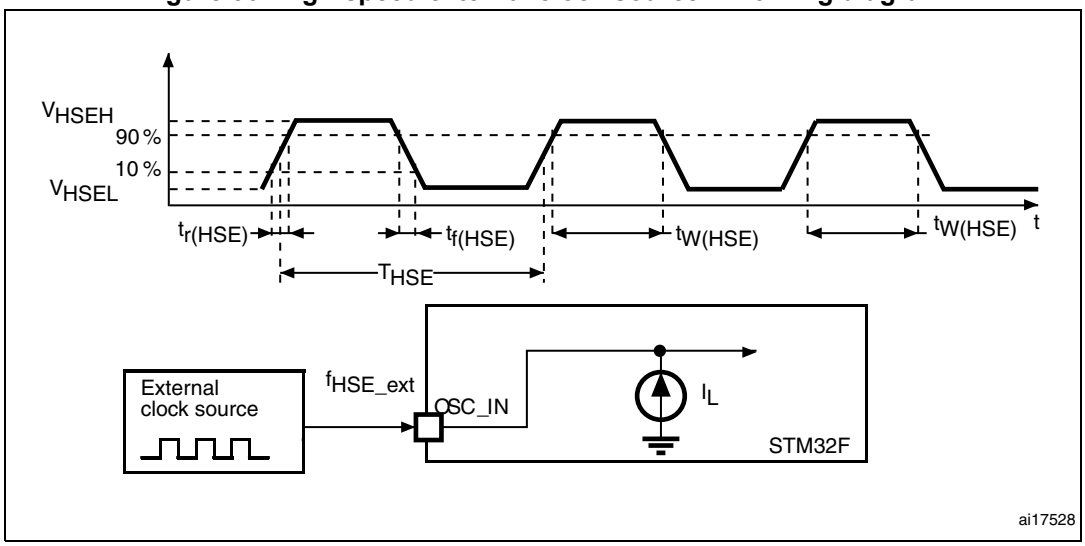
The characteristics given in *Table 31* result from tests performed using an low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 14*.

Table 31. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency(1)	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	-	$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{f(LSE)}$	OSC32_IN high or low time(1)		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)		-	-	50	
$C_{in(LSE)}$	OSC32_IN input capacitance(1)	-	-	5	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	30	-	70	%
I_L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design.

Figure 30. High-speed external clock source AC timing diagram



Static latchup

Two complementary static tests are required on six parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latchup standard.

Table 46. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

5.3.15 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibilty to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of 5 µA/+0 µA range), or other functional failure (for example reset, oscillator frequency deviation).

Negative induced leakage current is caused by negative injection and positive induced leakage current by positive injection.

The test results are given in *Table 47*.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 37* and *Table 50*, respectively.

Unless otherwise specified, the parameters given in *Table 50* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Table 50. I/O AC characteristics(1)(2)

OSPEEDRy [1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
00	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} > 2.70 V	-	-	4	MHz
			C_L = 50 pF, V_{DD} > 1.8 V	-	-	2	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	8	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	4	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 50 pF, V_{DD} = 1.8 V to 3.6 V	-	-	100	ns
01	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} > 2.70 V	-	-	25	MHz
			C_L = 50 pF, V_{DD} > 1.8 V	-	-	12.5	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	50(4)	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	20	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 50 pF, V_{DD} >2.7 V	-	-	10	ns
			C_L = 50 pF, V_{DD} > 1.8 V	-	-	20	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	6	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	10	
10	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 40 pF, V_{DD} > 2.70 V	-	-	50(4)	MHz
			C_L = 40 pF, V_{DD} > 1.8 V	-	-	25	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	100(4)	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	50(4)	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 40 pF, V_{DD} > 2.70 V	-	-	6	ns
			C_L = 40 pF, V_{DD} > 1.8 V	-	-	10	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	4	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	6	

Figure 44. USB OTG FS timings: definition of data signal rise and fall time

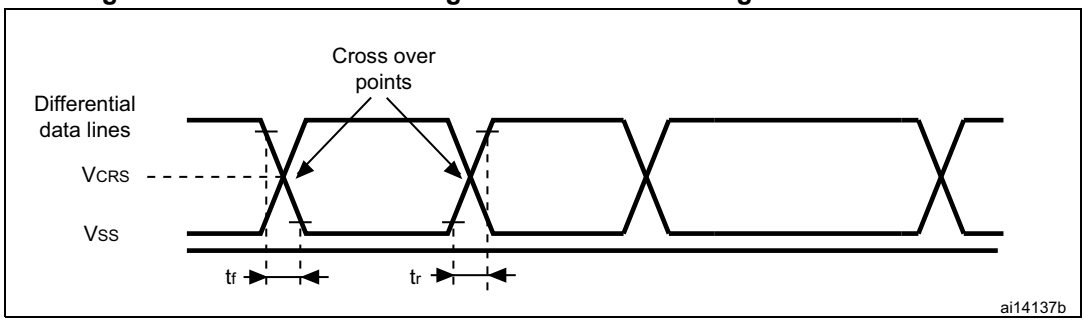


Table 59. USB OTG FS electrical characteristics(1)

Driver characteristics					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_r	Rise time(2)	C_L = 50 pF	4	20	ns
t_f	Fall time(2)	C_L = 50 pF	4	20	ns
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage	-	1.3	2.0	V

1. Guaranteed by design.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

USB HS characteristics

Unless otherwise specified, the parameters given in *Table 62* for ULPI are derived from tests performed under the ambient temperature, f_{HCLK} frequency summarized in *Table 61* and V_{DD} supply voltage conditions summarized in *Table 60*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$.

Refer to Section *Section 5.3.16: I/O port characteristics* for more details on the input/output characteristics.

Table 60. USB HS DC electrical characteristics

Symbol		**Parameter**	**Min.(1)**	**Max.(1)**	**Unit**
Input level	V_{DD}	USB OTG HS operating voltage	2.7	3.6	V

1. All the voltages are measured from the local ground potential.

Table 61. USB HS clock timing parameters(1)

Parameter		**Symbol**	**Min**	**Nominal**	**Max**	**Unit**
f_{HCLK} value to guarantee proper operation of USB HS interface		-	30	-	-	MHz
Frequency (first transition)	8-bit ±10%	F_{START_8BIT}	54	60	66	MHz

Table 61. USB HS clock timing parameters(1)

Parameter		Symbol	Min	Nominal	Max	Unit
Frequency (steady state) ±500 ppm		F_{STEADY}	59.97	60	60.03	MHz
Duty cycle (first transition)	8-bit ±10%	D_{START_8BIT}	40	50	60	%
Duty cycle (steady state) ±500 ppm		D_{STEADY}	49.975	50	50.025	%
Time to reach the steady state frequency and duty cycle after the first transition		T_{STEADY}	-	-	1.4	ms
Clock startup time after the de-assertion of SuspendM	Peripheral	T_{START_DEV}	-	-	5.6	ms
	Host	T_{START_HOST}	-	-	-	
PHY preparation time after the first transition of the input clock		T_{PREP}	-	-	-	µs

1. Guaranteed by design.

Table 62. ULPI timing

Parameter	Symbol	Value(1)		Unit
		Min.	Max.	
Control in (ULPI_DIR) setup time	t_{SC}	-	2.0	ns
Control in (ULPI_NXT) setup time		-	1.5	
Control in (ULPI_DIR, ULPI_NXT) hold time	t_{HC}	0	-	
Data in setup time	t_{SD}	-	2.0	
Data in hold time	t_{HD}	0	-	
Control out (ULPI_STP) setup time and hold time	t_{DC}	-	9.2	
Data out available from clock rising edge	t_{DD}	-	10.7	

1. V_{DD} = 2.7 V to 3.6 V and T_A = –40 to 85 °C.

Figure 45. ULPI timing diagram

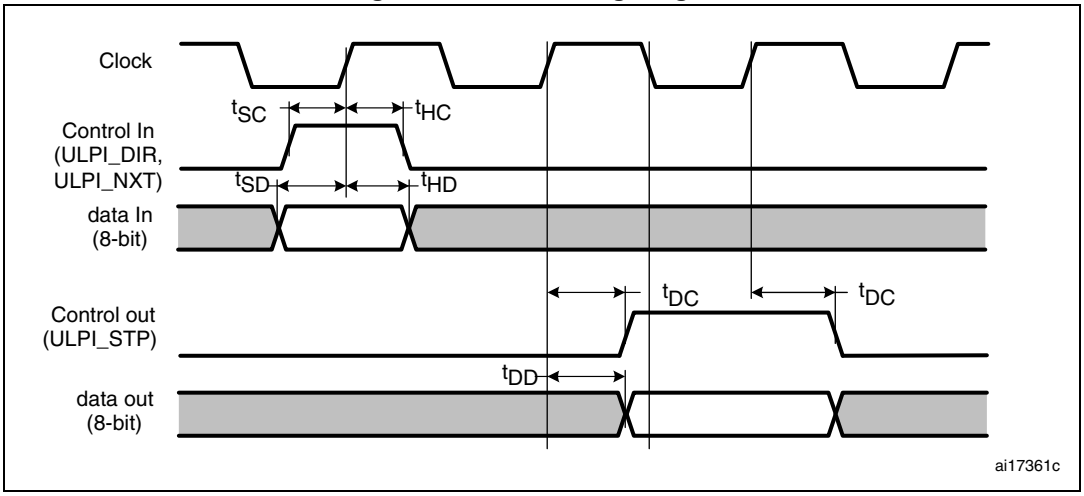


Figure 47. Ethernet RMII timing diagram

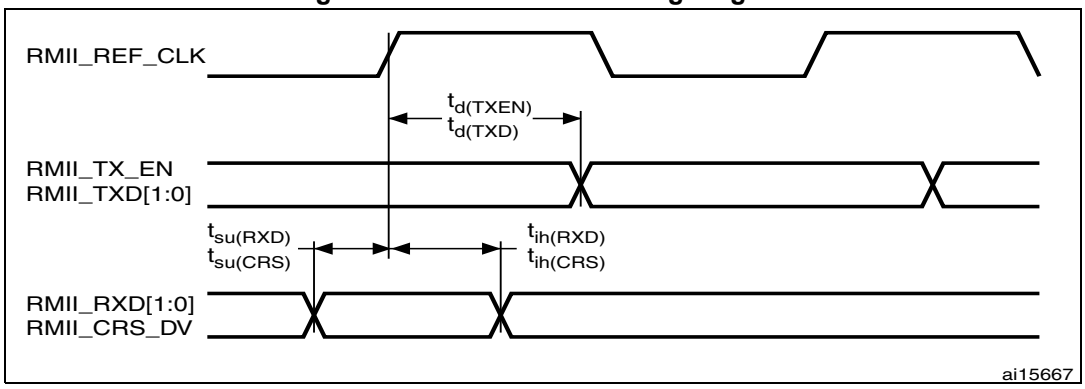


Table 65. Dynamic characteristics: Ethernet MAC signals for RMII

Symbol	Rating	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	2	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	1	-	-	ns
$t_{su(CRS)}$	Carrier sense set-up time	0.5	-	-	ns
$t_{ih(CRS)}$	Carrier sense hold time	2	-	-	ns
$t_{d(TXEN)}$	Transmit enable valid delay time	8	9.5	11	ns
$t_{d(TXD)}$	Transmit data valid delay time	8.5	10	11.5	ns

Table 66 gives the list of Ethernet MAC signals for MII and *Figure 47* shows the corresponding timing diagram.

Figure 48. Ethernet MII timing diagram

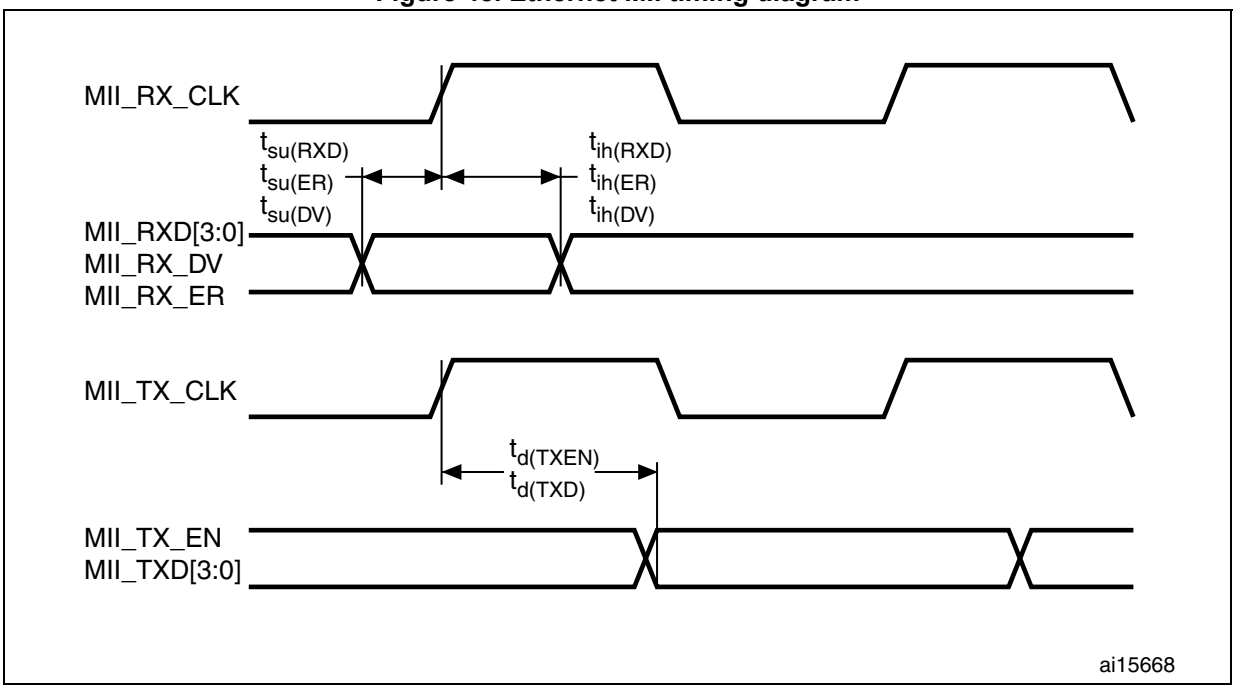


Table 66. Dynamic characteristics: Ethernet MAC signals for MII(1)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	9		-	ns
$t_{ih(RXD)}$	Receive data hold time	10		-	
$t_{su(DV)}$	Data valid setup time	9		-	
$t_{ih(DV)}$	Data valid hold time	8		-	
$t_{su(ER)}$	Error setup time	6		-	
$t_{ih(ER)}$	Error hold time	8		-	
$t_{d(TXEN)}$	Transmit enable valid delay time	0	10	14	
$t_{d(TXD)}$	Transmit data valid delay time	0	10	15	

1. Guaranteed by characterization.

5.3.20 CAN (controller area network) interface

Refer to *Section 5.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (CANTX and CANRX).

5.3.21 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 67* are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 14*.

Table 67. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	1.8(1)	-	3.6	V
V_{REF+}	Positive reference voltage	-	1.8(1)(2)(3)	-	V_{DDA}	
V_{REF-}	Negative reference voltage	-	-	0	-	
f_{ADC}	ADC clock frequency	V_{DDA} = 1.8(1)(3) to 2.4 V	0.6	15	18	MHz
		V_{DDA} = 2.4 to 3.6 V(3)	0.6	30	36	MHz
f_{TRIG}(4)	External trigger frequency	f_{ADC} = 30 MHz, 12-bit resolution	-	-	1764	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(5)	-	0 (V_{SSA} or V_{REF-} tied to ground)	-	V_{REF+}	V
R_{AIN}(4)	External input impedance	See *Equation 1* for details	-	-	50	kΩ
R_{ADC}(4)(6)	Sampling switch resistance	-	-	-	6	kΩ
C_{ADC}(4)	Internal sample and hold capacitor	-	-	4	-	pF

Table 74. DAC characteristics (continued)

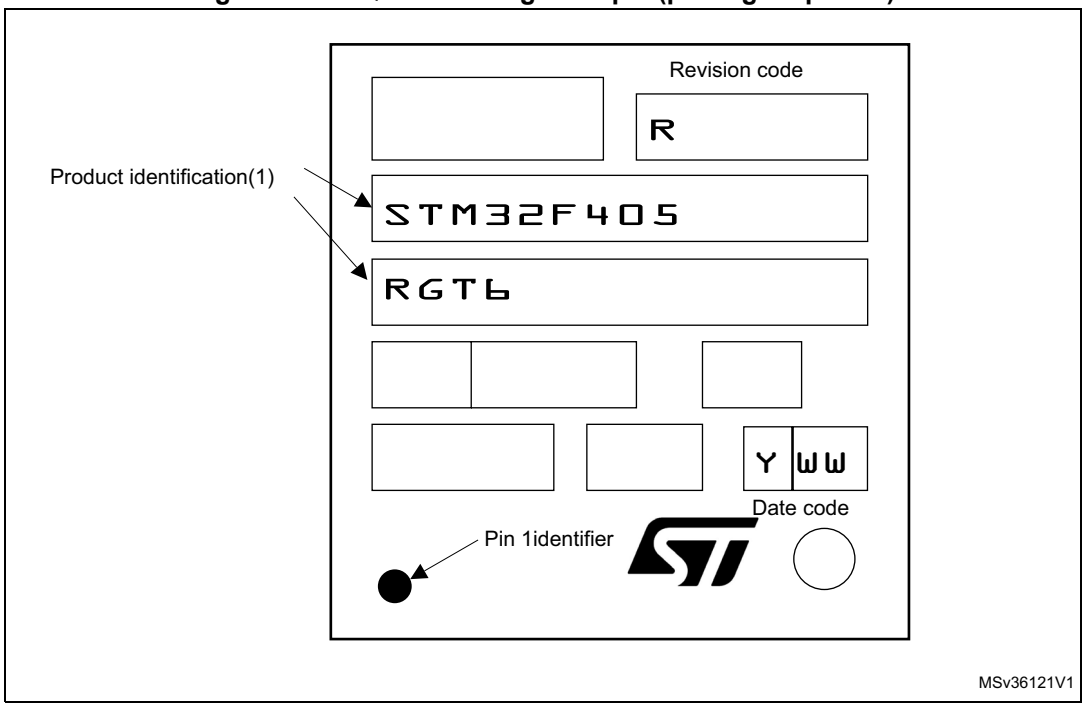
Symbol	Parameter	Min	Typ	Max	Unit	Comments
R_{LOAD}(2)	Resistive load with buffer ON	5	-	-	kΩ	
R_O(2)	Impedance output with buffer OFF	-	-	15	kΩ	When the buffer is OFF, the Minimum resistive load between DAC_OUT and V_{SS} to have a 1% accuracy is 1.5 MΩ
C_{LOAD}(2)	Capacitive load	-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
DAC_OUT min(2)	Lower DAC_OUT voltage with buffer ON	0.2	-	-	V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at V_{REF+} = 3.6 V and (0x1C7) to (0xE38) at V_{REF+} = 1.8 V
DAC_OUT max(2)	Higher DAC_OUT voltage with buffer ON	-	-	V_{DDA} – 0.2	V	
DAC_OUT min(2)	Lower DAC_OUT voltage with buffer OFF	-	0.5	-	mV	It gives the maximum output excursion of the DAC.
DAC_OUT max(2)	Higher DAC_OUT voltage with buffer OFF	-	-	V_{REF+} – 1LSB	V	
I_{VREF+}(4)	DAC DC V_{REF} current consumption in quiescent mode (Standby mode)	-	170	240	µA	With no load, worst code (0x800) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs
		-	50	75		With no load, worst code (0xF1C) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs
I_{DDA}(4)	DAC DC VDDA current consumption in quiescent mode(3)	-	280	380	µA	With no load, middle code (0x800) on the inputs
		-	475	625	µA	With no load, worst code (0xF1C) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs
DNL(4)	Differential non linearity Difference between two consecutive code-1LSB)	-	-	±0.5	LSB	Given for the DAC in 10-bit configuration.
		-	-	±2	LSB	Given for the DAC in 12-bit configuration.
INL(4)	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)	-	-	±1	LSB	Given for the DAC in 10-bit configuration.
		-	-	±4	LSB	Given for the DAC in 12-bit configuration.

Device marking for LQFP64

The following figure gives an example of topside marking and pin 1 position identifier location.

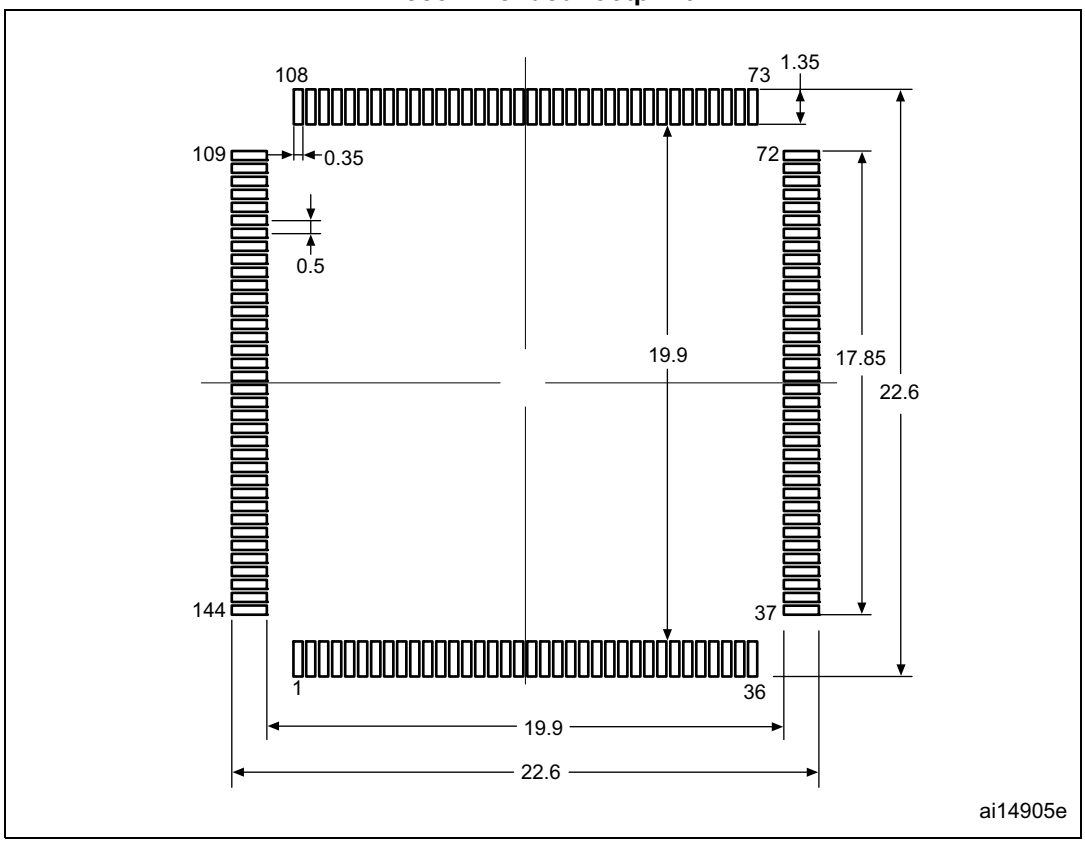
Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 80. LPQF64 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Figure 85. LQFP144 - 144-pin,20 x 20 mm low-profile quad flat package recommended footprint



1. Dimensions are in millimeters.