Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	168MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f405vgt6j

List of tables

Table 1. Device summary . . . 2
Table 2. STM32F405xx and STM32F407xx: features and peripheral counts. . . . 14
Table 3. Regulator ON/OFF and internal reset ON/OFF availability. . . . 29
Table 4. Timer feature comparison . . . 31
Table 5. USART feature comparison . . . 35
Table 6. Legend/abbreviations used in the pinout table . . . 46
Table 7. STM32F40xxx pin and ball definitions . . . 47
Table 8. FSMC pin definition . . . 59
Table 9. Alternate function mapping . . . 62
Table 10. register boundary addresses . . . 72
Table 11. Voltage characteristics . . . 78
Table 12. Current characteristics . . . 79
Table 13. Thermal characteristics. . . . 79
Table 14. General operating conditions . . . 79
Table 15. Limitations depending on the operating power supply range . . . 81
Table 16. VCAP_1/VCAP_2 operating conditions . . . 82
Table 17. Operating conditions at power-up / power-down (regulator ON) . . . 82
Table 18. Operating conditions at power-up / power-down (regulator OFF). . . . 82
Table 19. Embedded reset and power control block characteristics. . . . 83
Table 20. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled) or RAM . . . 85
Table 21. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled) . . . 86
Table 22. Typical and maximum current consumption in Sleep mode . . . 89
Table 23. Typical and maximum current consumptions in Stop mode . . . 90
Table 24. Typical and maximum current consumptions in Standby mode . . . 90
Table 25. Typical and maximum current consumptions in V_{BAT} mode. . . . 91
Table 26. Typical current consumption in Run mode, code with data processing running from Flash memory, regulator ON (ART accelerator enabled except prefetch), V_{DD} = 1.8 V . . . 93
Table 27. Switching output I/O current consumption . . . 95
Table 28. Peripheral current consumption . . . 96
Table 29. Low-power mode wakeup timings . . . 99
Table 30. High-speed external user clock characteristics. . . . 99
Table 31. Low-speed external user clock characteristics . . . 100
Table 32. HSE 4-26 MHz oscillator characteristics . . . 101
Table 33. LSE oscillator characteristics (f_{LSE} = 32.768 kHz) . . . 102
Table 34. HSI oscillator characteristics . . . 103
Table 35. LSI oscillator characteristics . . . 103
Table 36. Main PLL characteristics. . . . 104
Table 37. PLLI2S (audio PLL) characteristics . . . 105
Table 38. SSCG parameters constraint . . . 106
Table 39. Flash memory characteristics . . . 108
Table 40. Flash memory programming . . . 108
Table 41. Flash memory programming with VPP . . . 110
Table 42. Flash memory endurance and data retention . . . 110
Table 43. EMS characteristics . . . 111
Table 44. EMI characteristics . . . 112

2.1 Full compatibility throughout the family

The STM32F405xx and STM32F407xx are part of the STM32F4 family. They are fully pin-to-pin, software and feature compatible with the STM32F2xx devices, allowing the user to try different memory densities, peripherals, and performances (FPU, higher frequency) for a greater degree of freedom during the development cycle.

The STM32F405xx and STM32F407xx devices maintain a close compatibility with the whole STM32F10xxx family. All functional pins are pin-to-pin compatible. The STM32F405xx and STM32F407xx, however, are not drop-in replacements for the STM32F10xxx devices: the two families do not have the same power scheme, and so their power pins are different. Nonetheless, transition from the STM32F10xxx to the STM32F40xxx family remains simple as only a few pins are impacted.

Figure 4, *Figure 3*, *Figure 2*, and *Figure 1* give compatible board designs between the STM32F40xxx, STM32F2, and STM32F10xxx families.

Figure 1. Compatible board design between STM32F10xx/STM32F40xxx for LQFP64

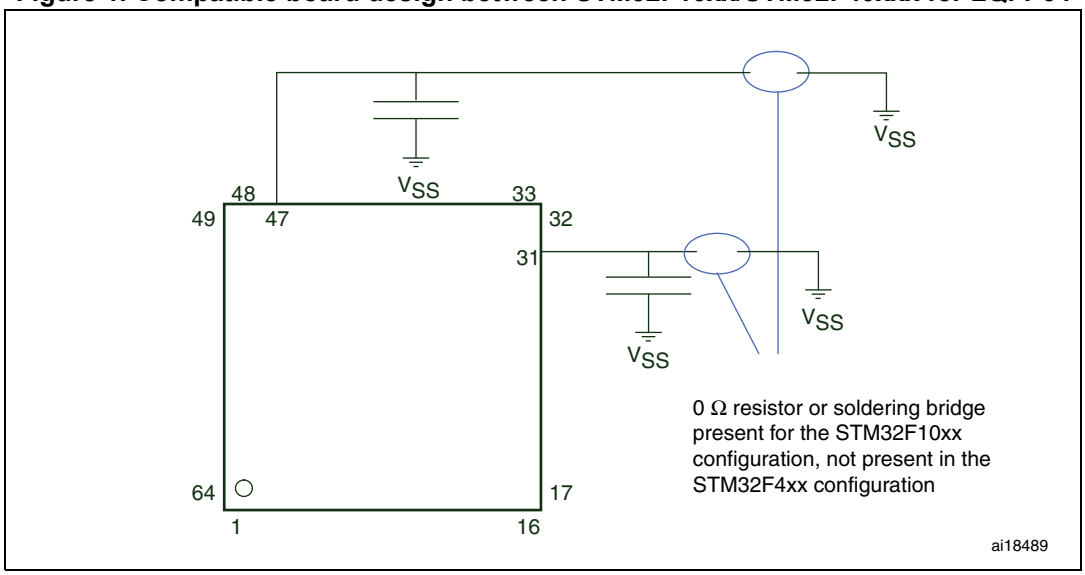
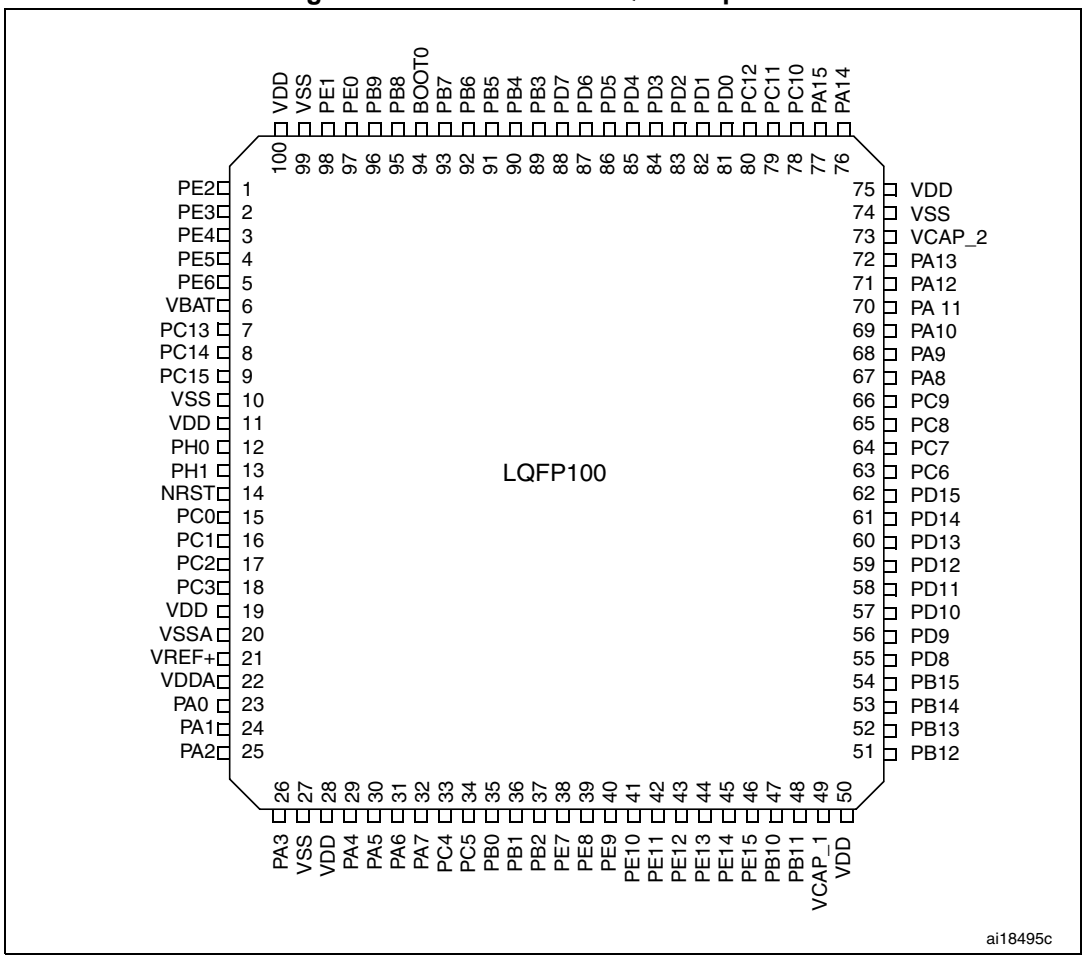


Figure 13. STM32F40xxx LQFP100 pinout



1. The above figure shows the package top view.

Table 8. FSMC pin definition (continued)

Pins[1]	FSMC				LQFP100[2]	WLCSP90 (2)
	CF	NOR/PSRAM/ SRAM	NOR/PSRAM Mux	NAND 16 bit		
PG2	-	A12	-	-	-	-
PG3	-	A13	-	-	-	-
PG4	-	A14	-	-	-	-
PG5	-	A15	-	-	-	-
PG6	-	-	-	INT2	-	-
PG7	-	-	-	INT3	-	-
PD0	D2	D2	DA2	D2	Yes	Yes
PD1	D3	D3	DA3	D3	Yes	Yes
PD3	-	CLK	CLK	-	Yes	-
PD4	NOE	NOE	NOE	NOE	Yes	Yes
PD5	NWE	NWE	NWE	NWE	Yes	Yes
PD6	NWAIT	NWAIT	NWAIT	NWAIT	Yes	Yes
PD7	-	NE1	NE1	NCE2	Yes	Yes
PG9	-	NE2	NE2	NCE3	-	-
PG10	NCE4_1	NE3	NE3	-	-	-
PG11	NCE4_2	-	-	-	-	-
PG12	-	NE4	NE4	-	-	-
PG13	-	A24	A24	-	-	-
PG14	-	A25	A25	-	-	-
PB7	-	NADV	NADV	-	Yes	Yes
PE0	-	NBL0	NBL0	-	Yes	-
PE1	-	NBL1	NBL1	-	Yes	-

1. Full FSMC features are available on LQFP144, LQFP176, and UFBGA176. The features available on smaller packages are given in the dedicated package column.
2. Ports F and G are not available in devices delivered in 100-pin packages.

Table 9. Alternate function mapping

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10 /11	I2C1/2/3	SPI1/SPI2/ I2S2/I2S2ext	SPI3/I2Sext /I2S3	USART1/2/3/ I2S3ext	UART4/5/ USART6	CAN1/2 TIM12/13/ 14	OTG_FS/ OTG_HS	ETH	FSMC/SDIO /OTG_FS	DCMI		
Port A	PA0	-	TIM2_CH1_ ETR	TIM 5_CH1	TIM8_ETR	-	-	-	USART2_CTS	UART4_TX	-	-	ETH_MII_CRS	-	-	-	EVENTOUT
	PA1	-	TIM2_CH2	TIM5_CH2	-	-	-	-	USART2_RTS	UART4_RX	-	-	ETH_MII _RX_CLK ETH_RMII__REF _CLK	-	-	-	EVENTOUT
	PA2	-	TIM2_CH3	TIM5_CH3	TIM9_CH1	-	-	-	USART2_TX	-	-	-	ETH_MDIO	-	-	-	EVENTOUT
	PA3	-	TIM2_CH4	TIM5_CH4	TIM9_CH2	-	-	-	USART2_RX	-	-	OTG_HS_ULPI_ D0	ETH _MII_COL	-	-	-	EVENTOUT
	PA4	-	-	-	-	-	SPI1_NSS	SPI3_NSS I2S3_WS	USART2_CK	-	-	-	-	OTG_HS_SOF	DCMI_ HSYNC	-	EVENTOUT
	PA5	-	TIM2_CH1_ ETR	-	TIM8_CH1N	-	SPI1_SCK	-	-	-	-	OTG_HS_ULPI_ CK	-	-	-	-	EVENTOUT
	PA6	-	TIM1_BKIN	TIM3_CH1	TIM8_BKIN	-	SPI1_MISO	-	-	-	TIM13_CH1	-	-	-	DCMI_PIXCK	-	EVENTOUT
	PA7	-	TIM1_CH1N	TIM3_CH2	TIM8_CH1N	-	SPI1_MOSI	-	-	-	TIM14_CH1	-	ETH_MII _RX_DV ETH_RMII _CRS_DV	-	-	-	EVENTOUT
	PA8	MCO1	TIM1_CH1	-	-	I2C3_SCL	-	-	USART1_CK	-	-	OTG_FS_SOF	-	-	-	-	EVENTOUT
	PA9	-	TIM1_CH2	-	-	I2C3_ SMBA	-	-	USART1_TX	-	-	-	-	-	DCMI_D0	-	EVENTOUT
	PA10	-	TIM1_CH3	-	-	-	-	-	USART1_RX	-	-	OTG_FS_ID	-	-	DCMI_D1	-	EVENTOUT
	PA11	-	TIM1_CH4	-	-	-	-	-	USART1_CTS	-	CAN1_RX	OTG_FS_DM	-	-	-	-	EVENTOUT
	PA12	-	TIM1_ETR	-	-	-	-	-	USART1_RTS	-	CAN1_TX	OTG_FS_DP	-	-	-	-	EVENTOUT
	PA13	JTMS-SWDIO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PA14	JTCK-SWCLK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PA15	JTDI	TIM 2_CH1 TIM 2_ETR	-	-	-	SPI1_NSS	SPI3_NSS/ I2S3_WS	-	-	-	-	-	-	-	-	EVENTOUT

Table 14. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{12}	Regulator ON: 1.2 V internal voltage on V_{CAP_1}/V_{CAP_2} pins	VOS bit in PWR_CR register = 0(1) Max frequency 144MHz	1.08	1.14	1.20	V
		VOS bit in PWR_CR register= 1 Max frequency 168MHz	1.20	1.26	1.32	V
	Regulator OFF: 1.2 V external voltage must be supplied from external regulator on V_{CAP_1}/V_{CAP_2} pins	Max frequency 144MHz	1.10	1.14	1.20	V
		Max frequency 168MHz	1.20	1.26	1.30	V
V_{IN}	Input voltage on RST and FT pins(6)	2 V ≤ V_{DD} ≤ 3.6 V	–0.3	-	5.5	V
		V_{DD} ≤ 2 V	–0.3	-	5.2	
	Input voltage on TTa pins	-	–0.3	-	V_{DDA}+ 0.3	
	Input voltage on B pin	-	-	-	5.5	
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(7)	LQFP64	-	-	435	mW
		LQFP100	-	-	465	
		LQFP144	-	-	500	
		LQFP176	-	-	526	
		UFBGA176	-	-	513	
		WLCSP90	-	-	543	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	–40	-	85	°C
		Low-power dissipation(8)	–40	-	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	–40	-	105	°C
		Low-power dissipation(8)	–40	-	125	
T_J	Junction temperature range	6 suffix version	–40	-	105	°C
		7 suffix version	–40	-	125	

1. The average expected gain in power consumption when VOS = 0 compared to VOS = 1 is around 10% for the whole temperature range, when the system clock frequency is between 30 and 144 MHz.
2. V_{DD}/V_{DDA} minimum value of 1.7 V is obtained when the device operates in reduced temperature range, and with the use of an external power supply supervisor (refer to *Section : Internal reset OFF*).
3. When the ADC is used, refer to *Table 67: ADC characteristics*.
4. If V_{REF+} pin is present, it must respect the following condition: V_{DDA}-V_{REF+} < 1.2 V.
5. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and power-down operation.
6. To sustain a voltage higher than V_{DD}+0.3, the internal pull-up and pull-down resistors must be disabled.
7. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax}.
8. In low-power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax}.

floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption measured previously (see *Table 28: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DD} is the MCU supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT}$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Table 29. Low-power mode wakeup timings

Symbol	Parameter	Min(1)	Typ(1)	Max(1)	Unit
$t_{WUSLEEP}$(2)	Wakeup from Sleep mode	-	5	-	CPU clock cycle
t_{WUSTOP}(2)	Wakeup from Stop mode (regulator in Run mode and Flash memory in Stop mode)	-	13	-	µs
	Wakeup from Stop mode (regulator in low-power mode and Flash memory in Stop mode)	-	17	40	
	Wakeup from Stop mode (regulator in Run mode and Flash memory in Deep power-down mode)	-	105	-	
	Wakeup from Stop mode (regulator in low-power mode and Flash memory in Deep power-down mode)	-	110	-	
$t_{WUSTDBY}$(2)(3)	Wakeup from Standby mode	260	375	480	µs

1. Guaranteed by characterization.
2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first instruction.
3. $t_{WUSTDBY}$ minimum and maximum values are given at 105 °C and –45 °C, respectively.

5.3.8 External clock source characteristics

High-speed external user clock generated from an external source

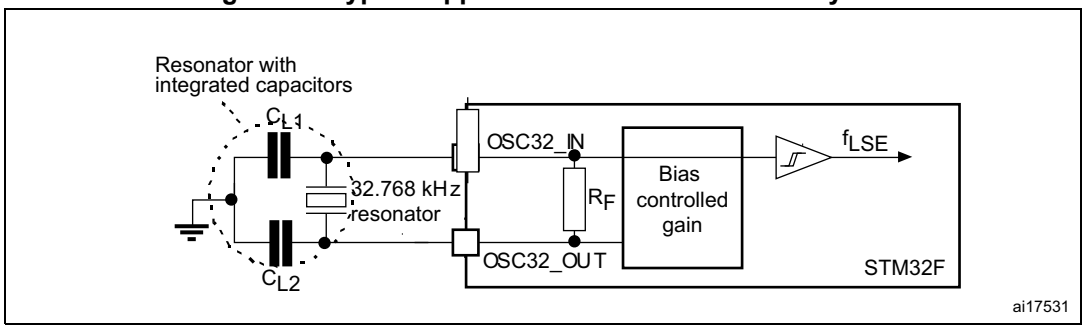
The characteristics given in *Table 30* result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 14*.

Table 30. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	External user clock source frequency(1)	-	1	-	50	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time(1)		5	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time(1)		-	-	10	
$C_{in(HSE)}$	OSC_IN input capacitance(1)	-	-	5	-	pF
$DuCy_{(HSE)}$	Duty cycle	-	45	-	55	%
I_L	OSC_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design.

Figure 33. Typical application with a 32.768 kHz crystal



5.3.9 Internal clock source characteristics

The parameters given in *Table 34* and *Table 35* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

High-speed internal (HSI) RC oscillator

Table 34. HSI oscillator characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	16	-	MHz
ACC_{HSI}	HSI user trimming step(2)	-	-	-	1	%
	Accuracy of the HSI oscillator	T_A = –40 to 105 °C(3)	–8	-	4.5	%
		T_A = –10 to 85 °C(3)	–4	-	4	%
		T_A = 25 °C(4)	–1	-	1	%
$t_{su(HSI)}$(2)	HSI oscillator startup time	-	-	2.2	4	µs
$I_{DD(HSI)}$(2)	HSI oscillator power consumption	-	-	60	80	µA

1. V_{DD} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design.
3. Guaranteed by characterization.
4. Factory calibrated, parts not soldered.

Low-speed internal (LSI) RC oscillator

Table 35. LSI oscillator characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}(2)	Frequency	17	32	47	kHz
$t_{su(LSI)}$(3)	LSI oscillator startup time	-	15	40	µs
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-	0.4	0.6	µA

1. V_{DD} = 3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by characterization.
3. Guaranteed by design.

Table 40. Flash memory programming (continued)

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
$t_{ERASE128KB}$	Sector (128 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	2	4	s
		Program/erase parallelism (PSIZE) = x 16	-	1.3	2.6	
		Program/erase parallelism (PSIZE) = x 32	-	1	2	
t_{ME}	Mass erase time	Program/erase parallelism (PSIZE) = x 8	-	16	32	s
		Program/erase parallelism (PSIZE) = x 16	-	11	22	
		Program/erase parallelism (PSIZE) = x 32	-	8	16	
V_{prog}	Programming voltage	32-bit program operation	2.7	-	3.6	V
		16-bit program operation	2.1	-	3.6	V
		8-bit program operation	1.8	-	3.6	V

1. Guaranteed by characterization.
2. The maximum programming time is measured after 100K erase operations.

Figure 39. SPI timing diagram - slave mode and CPHA = 0

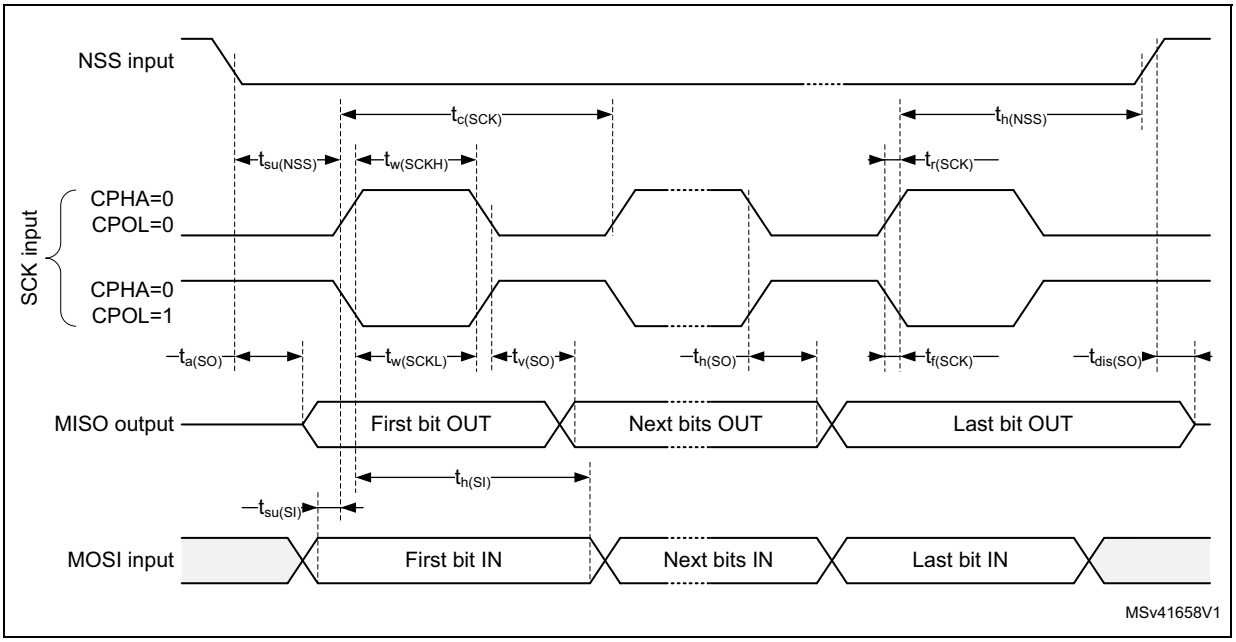
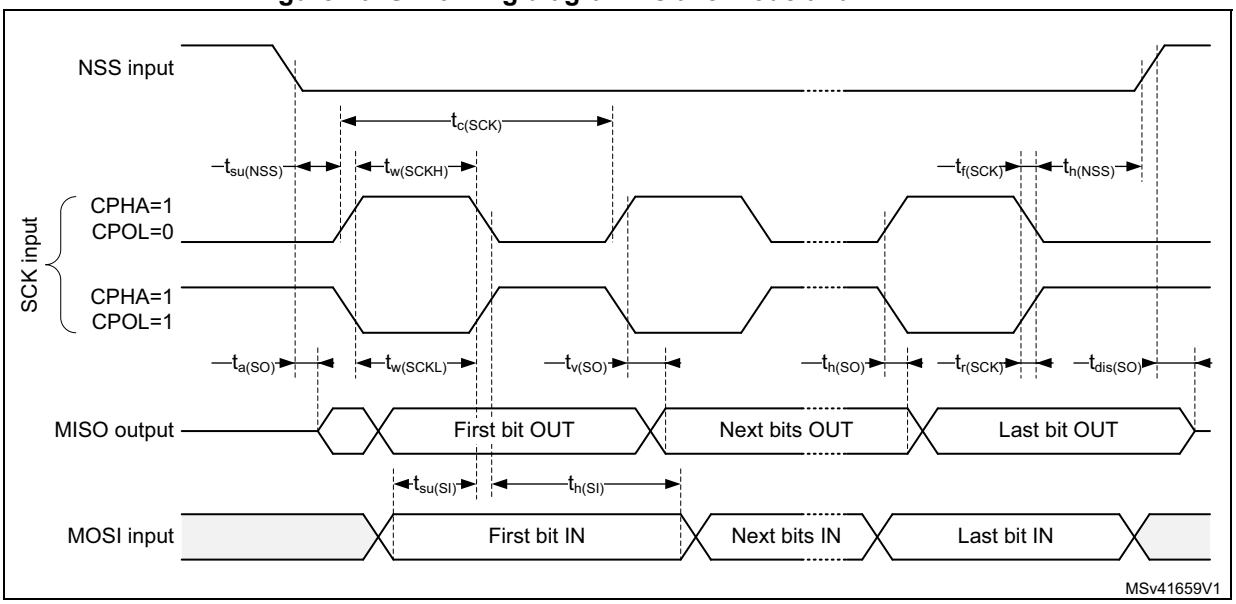


Figure 40. SPI timing diagram - slave mode and CPHA = 1



Equation 1: R_{AIN} max formula

$$R_{AIN} = \frac{(k - 0.5)}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. N = 12 (from 12-bit resolution) and k is the number of sampling periods defined in the ADC_SMPR1 register.

Table 68. ADC accuracy at f_{ADC} = 30 MHz

Symbol	Parameter	Test conditions	Typ	Max(1)	Unit
ET	Total unadjusted error	f_{PCLK2} = 60 MHz, f_{ADC} = 30 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 1.8(2) to 3.6 V	±2	±5	LSB
EO	Offset error		±1.5	±2.5	
EG	Gain error		±1.5	±3	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±1.5	±3	

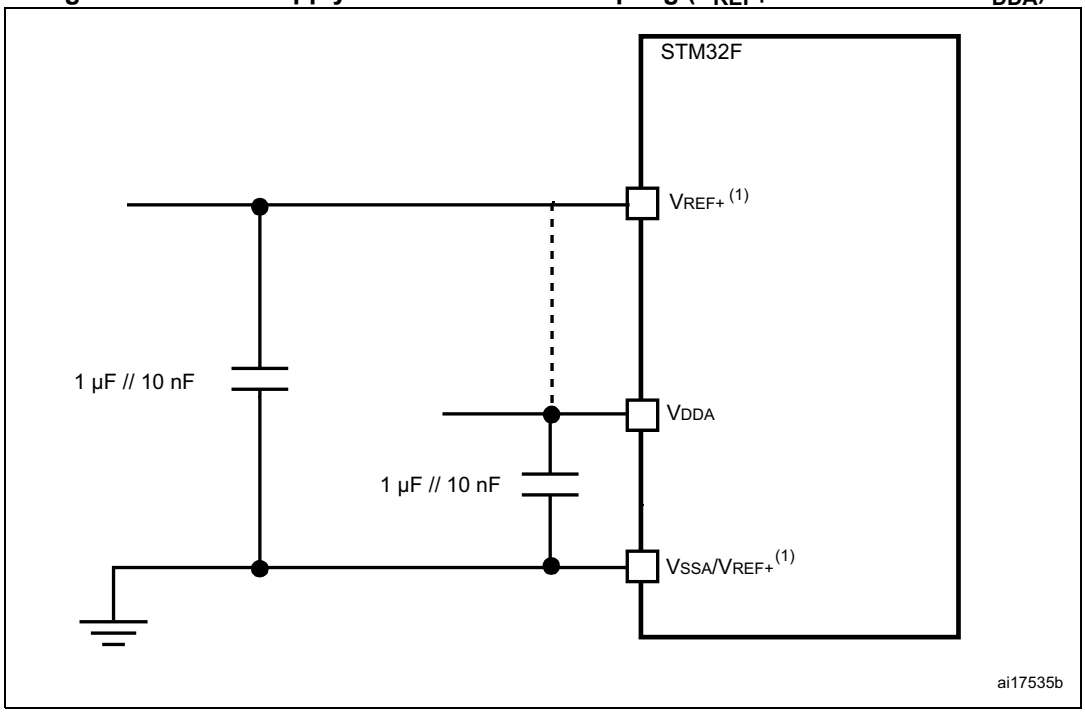
1. Guaranteed by characterization.
2. V_{DD}/V_{DDA} minimum value of 1.7 V is obtained when the device operates in reduced temperature range, and with the use of an external power supply supervisor (refer to *Section : Internal reset OFF*).

Note: ADC accuracy vs. negative injection current: injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $SI_{INJ(PIN)}$ in Section 5.3.16 does not affect the ADC accuracy.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 51* or *Figure 52*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 51. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are both available on UFBGA176. V_{REF+} is also available on LQFP100, LQFP144, and LQFP176. When V_{REF+} and V_{REF-} are not available, they are internally connected to V_{DDA} and V_{SSA}.

Figure 59. Synchronous multiplexed PSRAM write timings

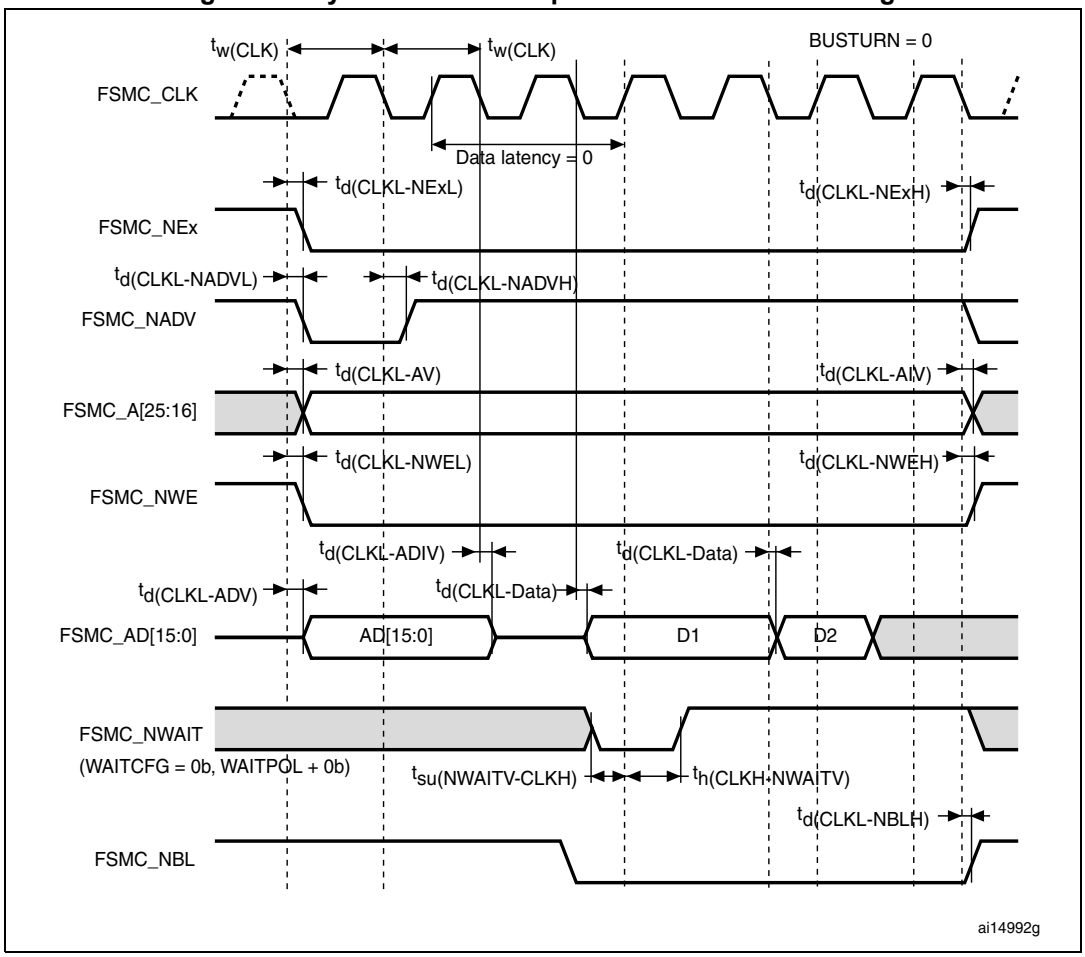


Table 80. Synchronous multiplexed PSRAM write timings(1)(2)

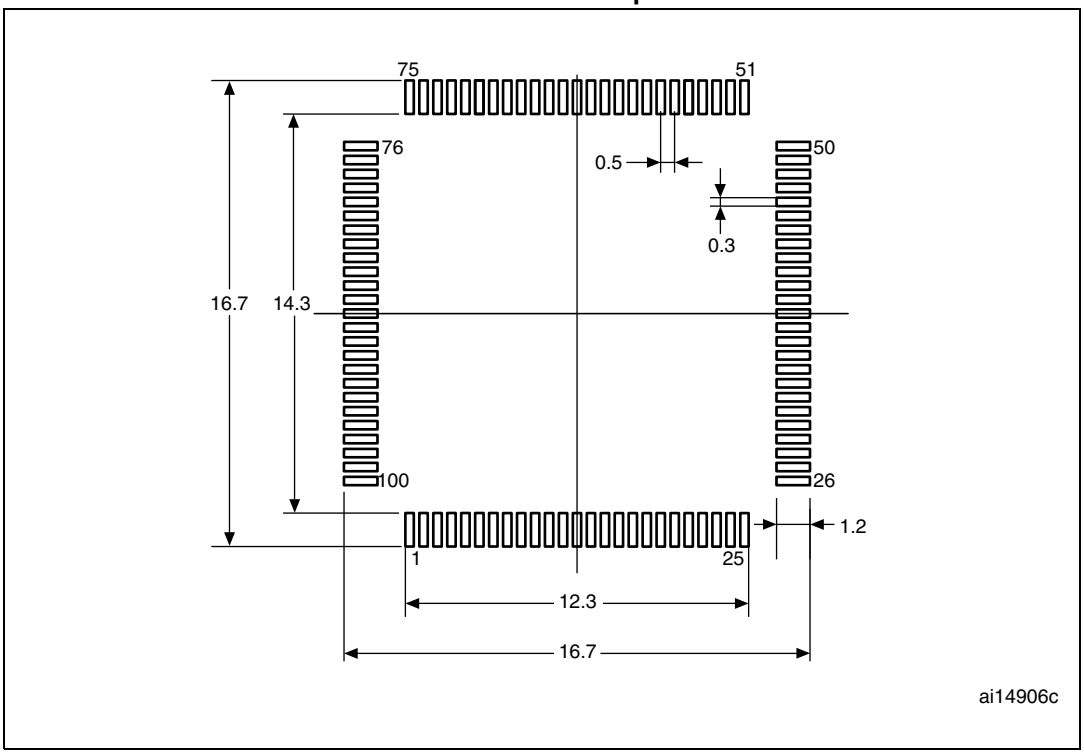
Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	$2T_{HCLK}$	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x=0..2)	-	1	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x= 0…2)	1	-	ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	0	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	0	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x=16…25)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x=16…25)	8	-	ns
$t_{d(CLKL-NWEL)}$	FSMC_CLK low to FSMC_NWE low	-	0.5	ns
$t_{d(CLKL-NWEH)}$	FSMC_CLK low to FSMC_NWE high	0	-	ns
$t_{d(CLKL-ADIV)}$	FSMC_CLK low to FSMC_AD[15:0] invalid	0	-	ns
$t_{d(CLKL-DATA)}$	FSMC_A/D[15:0] valid data after FSMC_CLK low	-	3	ns

Table 93. LQPF100 – 100-pin, 14 x 14 mm low-profile quad flat package mechanical data(1) (continued)

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 82. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint



1. Dimensions are expressed in millimeters.

Table 94. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.874
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	-	17.500	-	-	0.689	-
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	-	17.500	-	-	0.6890	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Table 95. UFBGA176+25 ball, 10 × 10 × 0.65 mm pitch, ultra thin fine pitch ball grid array mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 88. UFBGA176+25 - 201-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array recommended footprint

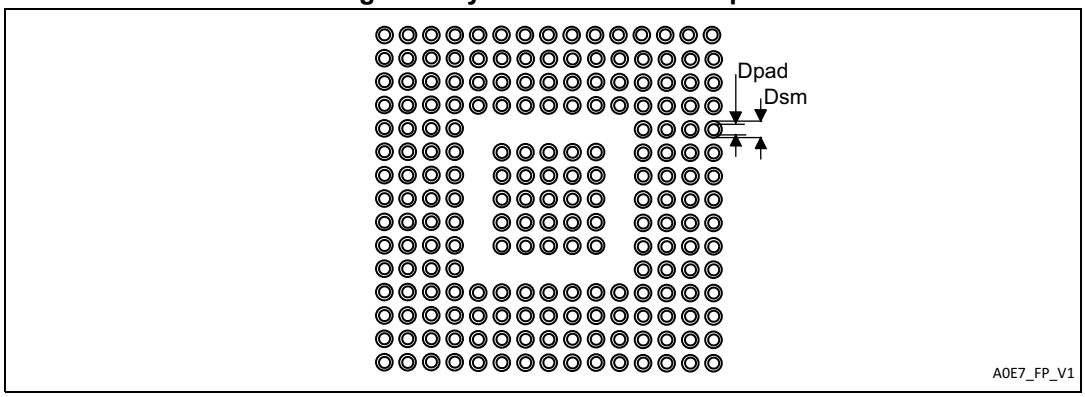


Table 96. UFBGA176+2 recommended PCB design rules (0.65 mm pitch BGA)

Dimension	Recommended values
Pitch	0.65
Dpad	0.300 mm
Dsm	0.400 mm typ. (depends on the soldermask registration tolerance)

Note: Non solder mask defined (NSMD) pads are recommended.

4 to 6 mils solder paste screen printing process.

Stencil opening is 0.300 mm.

Stencil thickness is between 0.100 mm and 0.125 mm.

Pad trace width is 0.100 mm.

Table 100. Document revision history (continued)

Date	Revision	Changes
24-Jan-2012	2 (continued)	Updated *Table 61: USB HS clock timing parameters* Updated *Table 67: ADC characteristics*. Updated *Table 68: ADC accuracy at fADC = 30 MHz*. Updated *Note 1* in *Table 74: DAC characteristics*. *Section 5.3.26: FSMC characteristics*: updated *Table 75* to *Table 86*, changed C_L value to 30 pF, and modified FSMC configuration for asynchronous timings and waveforms. Updated *Figure 59: Synchronous multiplexed PSRAM write timings*. Updated *Table 98: Package thermal characteristics*. Appendix *A.1: USB OTG full speed (FS) interface solutions*: modified *Figure 93: USB controller configured as peripheral-only and used in Full speed mode* added *Note 2*, updated *Figure 94: USB controller configured as host-only and used in full speed mode* and added *Note 2*, changed *Figure 95: USB controller configured in dual mode and used in full speed mode* and added *Note 3*. Appendix *A.2: USB OTG high speed (HS) interface solutions*: removed figures *USB OTG HS device-only connection in FS mode* and *USB OTG HS host-only connection in FS mode, and updated Figure 96: USB controller configured as peripheral, host, or dual-mode and used in high speed mode* and added *Note 2*. Added Appendix *A.3: Ethernet interface solutions*.

Table 100. Document revision history (continued)

Date	Revision	Changes
04-Jun-2013	4 (continued)	Updated *Figure 6: Multi-AHB matrix*. Updated *Figure 7: Power supply supervisor interconnection with internal reset OFF* Changed 1.2 V to V_{12} in *Section : Regulator OFF* Updated LQFP176 pin 48. Updated *Section 1: Introduction*. Updated *Section 2: Description*. Updated operating voltage in *Table 2: STM32F405xx and STM32F407xx: features and peripheral counts*. Updated *Note 1*. Updated *Section 2.2.15: Power supply supervisor*. Updated *Section 2.2.16: Voltage regulator*. Updated *Figure 9: Regulator OFF*. Updated *Table 3: Regulator ON/OFF and internal reset ON/OFF availability*. Updated *Section 2.2.19: Low-power modes*. Updated *Section 2.2.20: VBAT operation*. Updated *Section 2.2.22: Inter-integrated circuit interface (I²C)* . Updated pin 48 in *Figure 15: STM32F40xxx LQFP176 pinout*. Updated *Table 6: Legend/abbreviations used in the pinout table*. Updated *Table 7: STM32F40xxx pin and ball definitions*. Updated *Table 14: General operating conditions*. Updated *Table 15: Limitations depending on the operating power supply range*. Updated *Section 5.3.7: Wakeup time from low-power mode*. Updated *Table 34: HSI oscillator characteristics*. Updated *Section 5.3.15: I/O current injection characteristics*. Updated *Table 48: I/O static characteristics*. Updated *Table 51: NRST pin characteristics*. Updated *Table 56: I^2C characteristics*. Updated *Figure 39: I^2C bus AC waveforms and measurement circuit*. Updated *Section 5.3.19: Communications interfaces*. Updated *Table 67: ADC characteristics*. Added *Table 70: Temperature sensor calibration values*. Added *Table 73: Internal reference voltage calibration values*. Updated *Section 5.3.26: FSMC characteristics*. Updated *Section 5.3.28: SD/SDIO MMC card host interface (SDIO) characteristics*. Updated *Table 23: Typical and maximum current consumptions in Stop mode*. Updated *Section : SPI interface characteristics* included *Table 55*. Updated *Section : I2S interface characteristics* included *Table 56*. Updated *Table 64: Dynamic characteristics: Eternity MAC signals for SMI*. Updated *Table 66: Dynamic characteristics: Ethernet MAC signals for MII*.

Table 100. Document revision history (continued)

Date	Revision	Changes
22-Oct-2015	6	In the whole document, updated notes related to values guaranteed by design or by characterization. Updated *Table 34: HSI oscillator characteristics*. Changed f_{VCO_OUT} minimum value and VCO freq to 100 MHz in *Table 36: Main PLL characteristics* and *Table 37: PLLI2S (audio PLL) characteristics*. Updated *Figure 39: SPI timing diagram - slave mode and CPHA = 0*. Updated *Figure 53: 12-bit buffered /non-buffered DAC*. Removed note 1 related to better performance using a restricted V_{DD} range in *Table 68: ADC accuracy at fADC = 30 MHz*. Upated *Figure 84: LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package outline*. Updated *Figure 87: UFBGA176+25 ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package outline* and *Table 95: UFBGA176+25 ball, 10 × 10 × 0.65 mm pitch, ultra thin fine pitch ball grid array mechanical data*.
16-Mar-2016	7	Updated *Figure 2: Compatible board design STM32F10xx/STM32F2/STM32F40xxx for LQFP100 package*. Updated $\|V_{SSX}-V_{SS}\|$ in *Table 11: Voltage characteristics* to add V_{REF+} Added V_{REF-}in *Table 67: ADC characteristics*. Updated *Table 90: WLCSP90 - 4.223 x 3.969 mm, 0.400 mm pitch wafer level chip scale package mechanical data*.
09-Sep-2016	8	Remove note 1 below *Figure 5: STM32F40xxx block diagram*. Updated definition of stresses above maximum ratings in *Section 5.2: Absolute maximum ratings*. Updated $t_{h(NSS)}$) in *Figure 39: SPI timing diagram - slave mode and CPHA = 0Figure* and *Figure 40: SPI timing diagram - slave mode and CPHA = 1*. Added note related to optional marking and inset/upset marks in all package marking sections. Updated *Figure 87: UFBGA176+25 ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package outline* and *Table 95: UFBGA176+25 ball, 10 × 10 × 0.65 mm pitch, ultra thin fine pitch ball grid array mechanical data*.