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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	168MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f405vgt6tr

1 Introduction

This datasheet provides the description of the STM32F405xx and STM32F407xx lines of microcontrollers. For more details on the whole STMicroelectronics STM32™ family, please refer to *Section 2.1: Full compatibility throughout the family*.

The STM32F405xx and STM32F407xx datasheet should be read in conjunction with the STM32F4xx reference manual which is available from the STMicroelectronics website *www.st.com*.

For information on the Cortex®-M4 core, please refer to the Cortex®-M4 programming manual (PM0214) available from *www.st.com*.

Table 2. STM32F405xx and STM32F407xx: features and peripheral counts (continued)

Peripherals		STM32F405RG	STM32F405OG	STM32F405VG	STM32F405ZG	STM32F405OE	STM32F407Vx	STM32F407Zx	STM32F407Ix
Communication interfaces	SPI / I2S	3/2 (full duplex)(2)							
	I^2C	3							
	USART/ UART	4/2							
	USB OTG FS	Yes							
	USB OTG HS	Yes							
	CAN	2							
	SDIO	Yes							
Camera interface		No					Yes		
GPIOs		51	72	82	114	72	82	114	140
12-bit ADC Number of channels		3							
		16	13	16	24	13	16	24	24
12-bit DAC Number of channels		Yes 2							
Maximum CPU frequency		168 MHz							
Operating voltage		1.8 to 3.6 V(3)							
Operating temperatures		Ambient temperatures: –40 to +85 °C /–40 to +105 °C							
		Junction temperature: –40 to + 125 °C							
Package		LQFP64	WLCSP90	LQFP100	LQFP144	WLCSP90	LQFP100	LQFP144	UFBGA176 LQFP176

1. For the LQFP100 and WLCSP90 packages, only FSMC Bank1 or Bank2 are available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select. Bank2 can only support a 16- or 8-bit NAND Flash memory using the NCE2 Chip Select. The interrupt line cannot be used since Port G is not available in this package.
2. The SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I^2S audio mode.
3. V_{DD}/V_{DDA} minimum value of 1.7 V is obtained when the device operates in reduced temperature range, and with the use of an external power supply supervisor (refer to *Section : Internal reset OFF*).

Table 5. USART feature comparison

USART name	Standard features	Modem (RTS/ CTS)	LIN	SPI master	irDA	Smartcard (ISO 7816)	Max. baud rate in Mbit/s (oversampling by 16)	Max. baud rate in Mbit/s (oversampling by 8)	APB mapping
USART1	X	X	X	X	X	X	5.25	10.5	APB2 (max. 84 MHz)
USART2	X	X	X	X	X	X	2.62	5.25	APB1 (max. 42 MHz)
USART3	X	X	X	X	X	X	2.62	5.25	APB1 (max. 42 MHz)
UART4	X	-	X	-	X	-	2.62	5.25	APB1 (max. 42 MHz)
UART5	X	-	X	-	X	-	2.62	5.25	APB1 (max. 42 MHz)
USART6	X	X	X	X	X	X	5.25	10.5	APB2 (max. 84 MHz)

2.2.24 Serial peripheral interface (SPI)

The STM32F40xxx feature up to three SPIs in slave and master modes in full-duplex and simplex communication modes. SPI1 can communicate at up to 42 Mbits/s, SPI2 and SPI3 can communicate at up to 21 Mbit/s. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes. All SPIs can be served by the DMA controller.

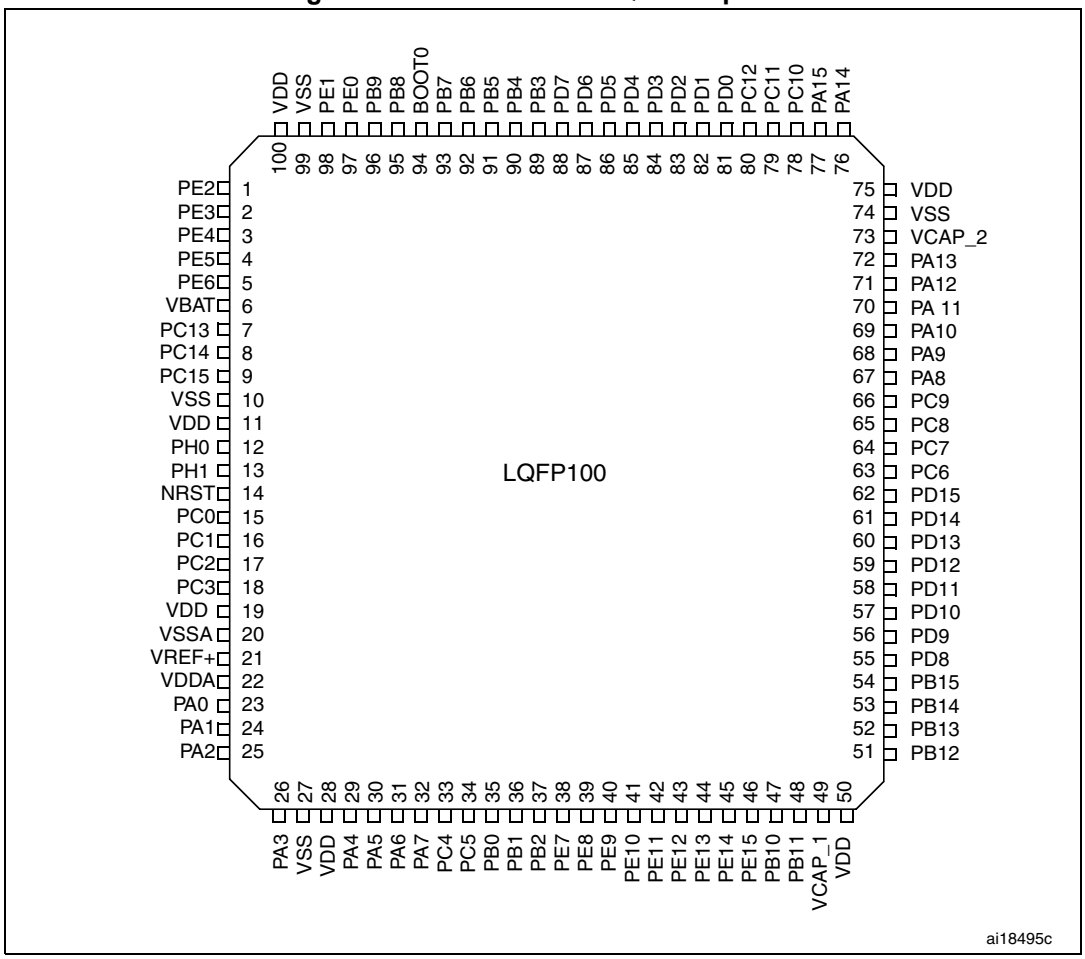
The SPI interface can be configured to operate in TI mode for communications in master mode and slave mode.

2.2.25 Inter-integrated sound (I^2S)

Two standard I^2S interfaces (multiplexed with SPI2 and SPI3) are available. They can be operated in master or slave mode, in full duplex and half-duplex communication modes, and can be configured to operate with a 16-/32-bit resolution as an input or output channel. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I^2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

All I^2Sx can be served by the DMA controller.

Figure 13. STM32F40xxx LQFP100 pinout



1. The above figure shows the package top view.

Table 9. Alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/SPI2/I2S2/I2S2ext	SPI3/I2Sext/I2S3	USART1/2/3/I2S3ext	UART4/5/USART6	CAN1/2 TIM12/13/14	OTG_FS/OTG_HS	ETH	FSMC/SDIO/OTG_FS	DCMI		
Port H	PH0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PH1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PH2	-	-	-	-	-	-	-	-	-	-	-	ETH _MII_CRS	-	-	-	EVENTOUT
	PH3	-	-	-	-	-	-	-	-	-	-	-	ETH _MII_COL	-	-	-	EVENTOUT
	PH4	-	-	-	-	I2C2_SCL	-	-	-	-	-	OTG_HS_ULPI_NXT	-	-	-	-	EVENTOUT
	PH5	-	-	-	-	I2C2_SDA	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PH6	-	-	-	-	I2C2_SMBA	-	-	-	-	TIM12_CH1	-	ETH _MII_RXD2	-	-	-	EVENTOUT
	PH7	-	-	-	-	I2C3_SCL	-	-	-	-	-	-	ETH _MII_RXD3	-	-	-	EVENTOUT
	PH8	-	-	-	-	I2C3_SDA	-	-	-	-	-	-	-	-	DCMI_HSYNC	-	EVENTOUT
	PH9	-	-	-	-	I2C3_SMBA	-	-	-	-	TIM12_CH2	-	-	-	DCMI_D0	-	EVENTOUT
	PH10	-	-	TIM5_CH1	-	-	-	-	-	-	-	-	-	-	DCMI_D1	-	EVENTOUT
	PH11	-	-	TIM5_CH2	-	-	-	-	-	-	-	-	-	-	DCMI_D2	-	EVENTOUT
	PH12	-	-	TIM5_CH3	-	-	-	-	-	-	-	-	-	-	DCMI_D3	-	EVENTOUT
	PH13	-	-	-	TIM8_CH1N	-	-	-	-	-	CAN1_TX	-	-	-	-	-	EVENTOUT
	PH14	-	-	-	TIM8_CH2N	-	-	-	-	-	-	-	-	-	DCMI_D4	-	EVENTOUT
	PH15	-	-	-	TIM8_CH3N	-	-	-	-	-	-	-	-	-	DCMI_D11	-	EVENTOUT

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V (for the 1.8 V ≤V_{DD} ≤3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 19*.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 20*.

Figure 19. Pin loading conditions

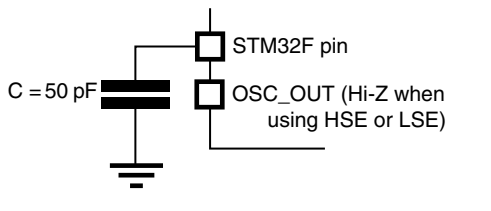


Figure 20. Pin input voltage

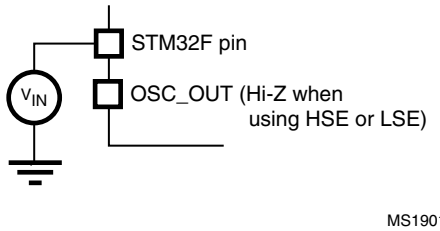


Table 22. Typical and maximum current consumption in Sleep mode

Symbol	Parameter	Conditions	f_{HCLK}	Typ	Max(1)		Unit
				T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Sleep mode	External clock(2), all peripherals enabled(3)	168 MHz	59	77	84	mA
			144 MHz	46	61	67	
			120 MHz	38	53	60	
			90 MHz	30	44	51	
			60 MHz	20	34	41	
			30 MHz	11	24	31	
			25 MHz	8	21	28	
			16 MHz	6	18	25	
			8 MHz	3	16	23	
			4 MHz	2	15	22	
			2 MHz	2	14	21	
		External clock(2), all peripherals disabled	168 MHz	12	27	35	
			144 MHz	9	22	29	
			120 MHz	8	20	28	
			90 MHz	7	19	26	
			60 MHz	5	17	24	
			30 MHz	3	16	23	
			25 MHz	2	15	22	
			16 MHz	2	14	21	
			8 MHz	1	14	21	
			4 MHz	1	13	21	
			2 MHz	1	13	21	

1. Guaranteed by characterization, tested in production at V_{DD} max and f_{HCLK} max with peripherals enabled.
2. External clock is 4 MHz and PLL is on when f_{HCLK} > 25 MHz.
3. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).

Table 23. Typical and maximum current consumptions in Stop mode

Symbol	Parameter	Conditions	Typ	Max			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_STOP}	Supply current in Stop mode with main regulator in Run mode	Flash in Stop mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	0.45	1.5	11.00	20.00	mA
		Flash in Deep power-down mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	0.40	1.5	11.00	20.00	
	Supply current in Stop mode with main regulator in Low-power mode	Flash in Stop mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	0.31	1.1	8.00	15.00	
		Flash in Deep power-down mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	0.28	1.1	8.00	15.00	

Table 24. Typical and maximum current consumptions in Standby mode

Symbol	Parameter	Conditions	Typ			Max(1)		Unit
			T_A = 25 °C			T_A = 85 °C	T_A = 105 °C	
			V_{DD} = 1.8 V	V_{DD}= 2.4 V	V_{DD} = 3.3 V	V_{DD} = 3.6 V		
I_{DD_STBY}	Supply current in Standby mode	Backup SRAM ON, low-speed oscillator and RTC ON	3.0	3.4	4.0	20	36	µA
		Backup SRAM OFF, low-speed oscillator and RTC ON	2.4	2.7	3.3	16	32	
		Backup SRAM ON, RTC OFF	2.4	2.6	3.0	12.5	24.8	
		Backup SRAM OFF, RTC OFF	1.7	1.9	2.2	9.8	19.2	

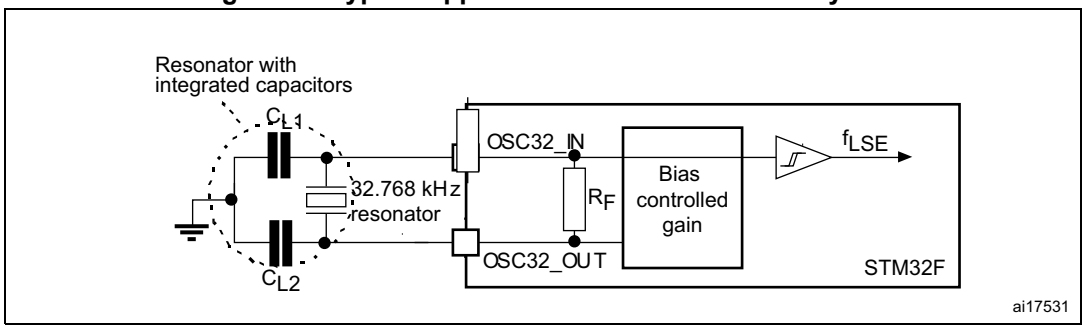
1. Guaranteed by characterization.

Table 27. Switching output I/O current consumption

Symbol	Parameter	Conditions(1)	I/O toggling frequency (f_{SW})	Typ	Unit
I_{DDIO}	I/O switching current	V_{DD} = 3.3 V(2) C = C_{INT}	2 MHz	0.02	mA
			8 MHz	0.14	
			25 MHz	0.51	
			50 MHz	0.86	
			60 MHz	1.30	
		V_{DD} = 3.3 V C_{EXT} = 0 pF C = C_{INT} + C_{EXT}+ C_S	2 MHz	0.10	
			8 MHz	0.38	
			25 MHz	1.18	
			50 MHz	2.47	
			60 MHz	2.86	
		V_{DD} = 3.3 V C_{EXT} = 10 pF C = C_{INT} + C_{EXT}+ C_S	2 MHz	0.17	
			8 MHz	0.66	
			25 MHz	1.70	
			50 MHz	2.65	
			60 MHz	3.48	
		V_{DD} = 3.3 V C_{EXT} = 22 pF C = C_{INT} + C_{EXT}+ C_S	2 MHz	0.23	
			8 MHz	0.95	
			25 MHz	3.20	
			50 MHz	4.69	
			60 MHz	8.06	
		V_{DD} = 3.3 V C_{EXT} = 33 pF C = C_{INT} + C_{EXT}+ C_S	2 MHz	0.30	
			8 MHz	1.22	
			25 MHz	3.90	
			50 MHz	8.82	
			60 MHz	-(3)	

1. C_S is the PCB board capacitance including the pad pin. C_S = 7 pF (estimated value).
2. This test is performed by cutting the LQFP package pin (pad removal).
3. At 60 MHz, C maximum load is specified 30 pF.

Figure 33. Typical application with a 32.768 kHz crystal



5.3.9 Internal clock source characteristics

The parameters given in *Table 34* and *Table 35* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

High-speed internal (HSI) RC oscillator

Table 34. HSI oscillator characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	16	-	MHz
ACC_{HSI}	HSI user trimming step(2)	-	-	-	1	%
	Accuracy of the HSI oscillator	T_A = –40 to 105 °C(3)	–8	-	4.5	%
		T_A = –10 to 85 °C(3)	–4	-	4	%
		T_A = 25 °C(4)	–1	-	1	%
$t_{su(HSI)}$(2)	HSI oscillator startup time	-	-	2.2	4	µs
$I_{DD(HSI)}$(2)	HSI oscillator power consumption	-	-	60	80	µA

1. V_{DD} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design.
3. Guaranteed by characterization.
4. Factory calibrated, parts not soldered.

Low-speed internal (LSI) RC oscillator

Table 35. LSI oscillator characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}(2)	Frequency	17	32	47	kHz
$t_{su(LSI)}$(3)	LSI oscillator startup time	-	15	40	µs
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-	0.4	0.6	µA

1. V_{DD} = 3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by characterization.
3. Guaranteed by design.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 37* and *Table 50*, respectively.

Unless otherwise specified, the parameters given in *Table 50* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Table 50. I/O AC characteristics(1)(2)

OSPEEDRy [1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
00	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} > 2.70 V	-	-	4	MHz
			C_L = 50 pF, V_{DD} > 1.8 V	-	-	2	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	8	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	4	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 50 pF, V_{DD} = 1.8 V to 3.6 V	-	-	100	ns
01	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} > 2.70 V	-	-	25	MHz
			C_L = 50 pF, V_{DD} > 1.8 V	-	-	12.5	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	50(4)	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	20	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 50 pF, V_{DD} >2.7 V	-	-	10	ns
			C_L = 50 pF, V_{DD} > 1.8 V	-	-	20	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	6	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	10	
10	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 40 pF, V_{DD} > 2.70 V	-	-	50(4)	MHz
			C_L = 40 pF, V_{DD} > 1.8 V	-	-	25	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	100(4)	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	50(4)	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 40 pF, V_{DD} > 2.70 V	-	-	6	ns
			C_L = 40 pF, V_{DD} > 1.8 V	-	-	10	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	4	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	6	

SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 55* for SPI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 14* with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 V_{DD}

Refer to *Section 5.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 55. SPI dynamic characteristics(1)

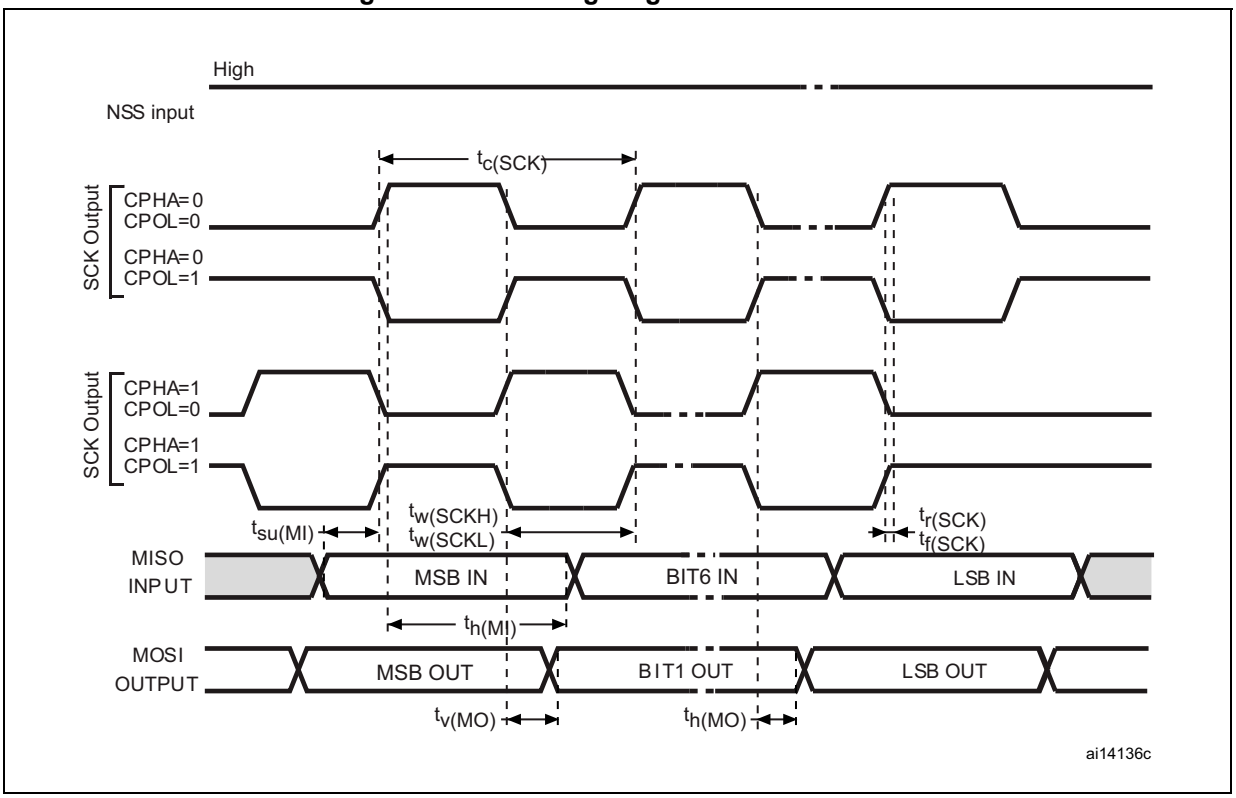
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SPI clock frequency	Master mode, SPI1, 2.7V < V_{DD} < 3.6V	-	-	42	MHz
		Slave mode, SPI1, 2.7V < V_{DD} < 3.6V			42	
$1/t_{c(SCK)}$		Master mode, SPI1/2/3, 1.7V < V_{DD} < 3.6V	-	-	21	
		Slave mode, SPI1/2/3, 1.7V < V_{DD} < 3.6V			21	
Duty(SCK)	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%

Table 55. SPI dynamic characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(SCKH)}$	SCK high and low time	Master mode, SPI presc = 2, 2.7V < V_{DD} < 3.6V	T_{PCLK}-0.5	T_{PCLK}	T_{PCLK}+0.5	ns
$t_{w(SCKL)}$		Master mode, SPI presc = 2, 1.7V < V_{DD} < 3.6V	T_{PCLK}-2	T_{PCLK}	T_{PCLK}+2	
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	4 x T_{PCLK}	-	-	
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	2 x T_{PCLK}			
$t_{su(MI)}$	Data input setup time	Master mode	6.5	-	-	
$t_{su(SI)}$		Slave mode	2.5	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	2.5	-	-	
$t_{h(SI)}$		Slave mode	4	-	-	
$t_{a(SO)}$(2)	Data output access time	Slave mode, SPI presc = 2	0	-	4 x T_{PCLK}	
$t_{dis(SO)}$(3)	Data output disable time	Slave mode, SPI1, 2.7V < V_{DD} < 3.6V	0	-	7.5	
		Slave mode, SPI1/2/3 1.7V < V_{DD} < 3.6V	0	-	16.5	
$t_{v(SO)}$ $t_{h(SO)}$	Data output valid/hold time	Slave mode (after enable edge), SPI1, 2.7V < V_{DD} < 3.6V	-	11	13	
		Slave mode (after enable edge), SPI2/3, 2.7V < V_{DD} < 3.6V	-	12	16.5	
		Slave mode (after enable edge), SPI1, 1.7V < V_{DD} < 3.6V	-	15.5	19	
		Slave mode (after enable edge), SPI2/3, 1.7V < V_{DD} < 3.6V	-	18	20.5	
$t_{v(MO)}$	Data output valid time	Master mode (after enable edge), SPI1, 2.7V < V_{DD} < 3.6V	-	-	2.5	
		Master mode (after enable edge), SPI1/2/3, 1.7V < V_{DD} < 3.6V	-	-	4.5	
$t_{h(MO)}$	Data output hold time	Master mode (after enable edge)	0	-	-	

1. Guaranteed by characterization.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

Figure 41. SPI timing diagram - master mode



I²S interface characteristics

Unless otherwise specified, the parameters given in *Table 56* for the i²S interface are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 14*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 V_{DD}

Refer to *Section 5.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (CK, SD, WS).

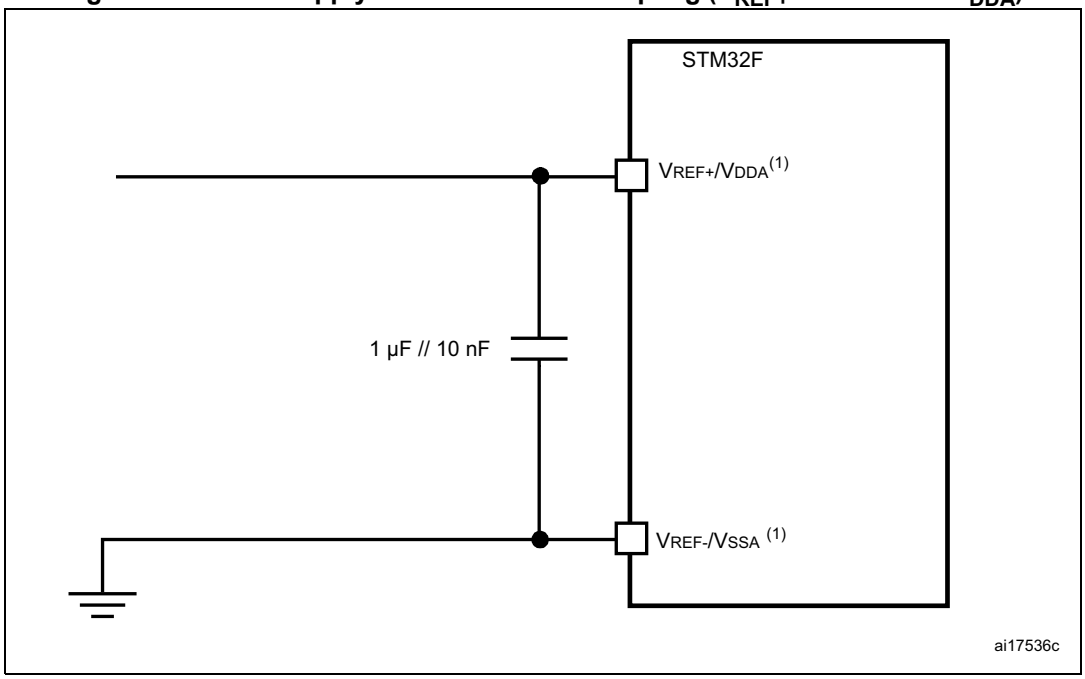
Table 56. I²S dynamic characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I²S main clock output	-	256 x 8K	256 x F_S(2)	MHz
f_{CK}	I²S clock frequency	Master data: 32 bits	-	64 x F_S	MHz
		Slave data: 32 bits	-	64 x F_S	
D_{CK}	I²S clock frequency duty cycle	Slave receiver	30	70	%
$t_{v(WS)}$	WS valid time	Master mode	0	6	ns
$t_{h(WS)}$	WS hold time	Master mode	0	-	
$t_{su(WS)}$	WS setup time	Slave mode	1	-	
$t_{h(WS)}$	WS hold time	Slave mode	0	-	
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	7.5	-	
$t_{su(SD\_SR)}$		Slave receiver	2	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver	0	-	
$t_{h(SD\_SR)}$		Slave receiver	0	-	
$t_{v(SD\_ST)}$ $t_{h(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	27	
$t_{v(SD\_MT)}$		Master transmitter (after enable edge)	-	20	
$t_{h(SD\_MT)}$	Data output hold time	Master transmitter (after enable edge)	2.5	-	

1. Guaranteed by characterization.
2. The maximum value of 256 x F_S is 42 MHz (APB1 maximum frequency).

Note: Refer to the I²S section of RM0090 reference manual for more details on the sampling frequency (F_S). f_{MCK}, f_{CK}, and D_{CK} values reflect only the digital peripheral behavior. The value of these parameters might be slightly impacted by the source clock accuracy. D_{CK} depends mainly on the value of ODD bit. The digital contribution leads to a minimum value of I2SDIV / (2 x I2SDIV + ODD) and a maximum value of (I2SDIV + ODD) / (2 x I2SDIV + ODD). F_S maximum value is supported for each mode/condition.

Figure 52. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are both available on UFBGA176. V_{REF+} is also available on LQFP100, LQFP144, and LQFP176. When V_{REF+} and V_{REF-} are not available, they are internally connected to V_{DDA} and V_{SSA}.

5.3.22 Temperature sensor characteristics

Table 69. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	-	2.5		mV/°C
V_{25}(1)	Voltage at 25 °C	-	0.76		V
t_{START}(2)	Startup time	-	6	10	µs
T_{S_temp}(2)	ADC sampling time when reading the temperature (1 °C accuracy)	10	-	-	µs

1. Guaranteed by characterization.
2. Guaranteed by design.

Table 70. Temperature sensor calibration values

Symbol	Parameter	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, V_{DDA}=3.3 V	0x1FFF 7A2C - 0x1FFF 7A2D
TS_CAL2	TS ADC raw data acquired at temperature of 110 °C, V_{DDA}=3.3 V	0x1FFF 7A2E - 0x1FFF 7A2F

5.3.23 V_{BAT} monitoring characteristics

Table 71. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	50	-	KΩ
Q	Ratio on V_{BAT} measurement	-	2	-	
Er(1)	Error on Q	–1	-	+1	%
T_{S_vbat}(2)(2)	ADC sampling time when reading the V_{BAT} 1 mV accuracy	5	-	-	µs

1. Guaranteed by design.
2. Shortest sampling time can be determined in the application by multiple iterations.

5.3.24 Embedded reference voltage

The parameters given in *Table 72* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Table 72. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +105 °C	1.18	1.21	1.24	V
$T_{S\_vrefint}$(1)	ADC sampling time when reading the internal reference voltage	-	10	-	-	µs
V_{RERINT_s}(2)	Internal reference voltage spread over the temperature range	V_{DD} = 3 V	-	3	5	mV
T_{Coeff}(2)	Temperature coefficient	-	-	30	50	ppm/°C
t_{START}(2)	Startup time	-	-	6	10	µs

1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design.

Table 73. Internal reference voltage calibration values

Symbol	Parameter	Memory address
V_{REFIN_CAL}	Raw data acquired at temperature of 30 °C, V_{DDA}=3.3 V	0x1FFF 7A2A - 0x1FFF 7A2B

5.3.25 DAC electrical characteristics

Table 74. DAC characteristics

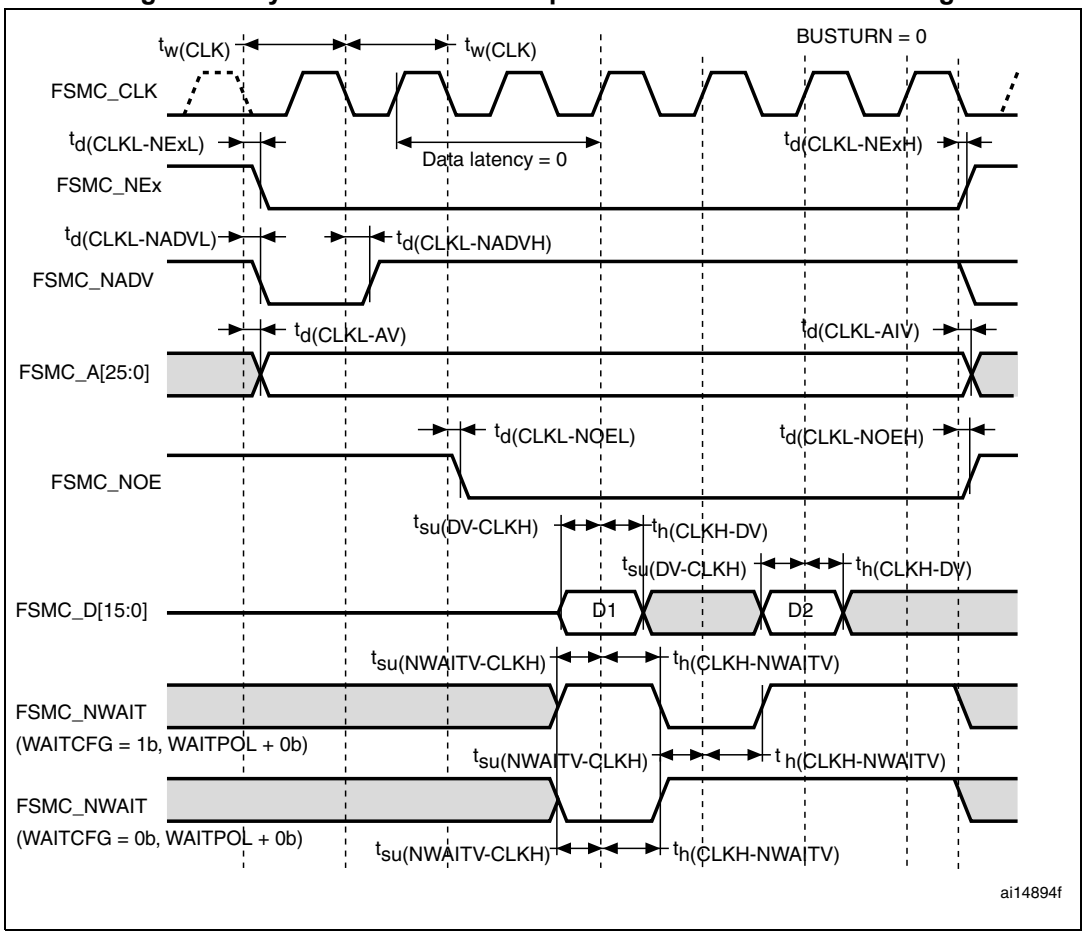
Symbol	Parameter	Min	Typ	Max	Unit	Comments
V_{DDA}	Analog supply voltage	1.8(1)	-	3.6	V	
V_{REF+}	Reference supply voltage	1.8(1)	-	3.6	V	$V_{REF+} \leq V_{DDA}$
V_{SSA}	Ground	0	-	0	V	

Table 80. Synchronous multiplexed PSRAM write timings(1)(2) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{d(CLKL-NBLH)}$	FSMC_CLK low to FSMC_NBL high	0	-	ns
$t_{su(NWAIT-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	4	-	ns
$t_{h(CLKH-NWAIT)}$	FSMC_NWAIT valid after FSMC_CLK high	0	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization.

Figure 60. Synchronous non-multiplexed NOR/PSRAM read timings

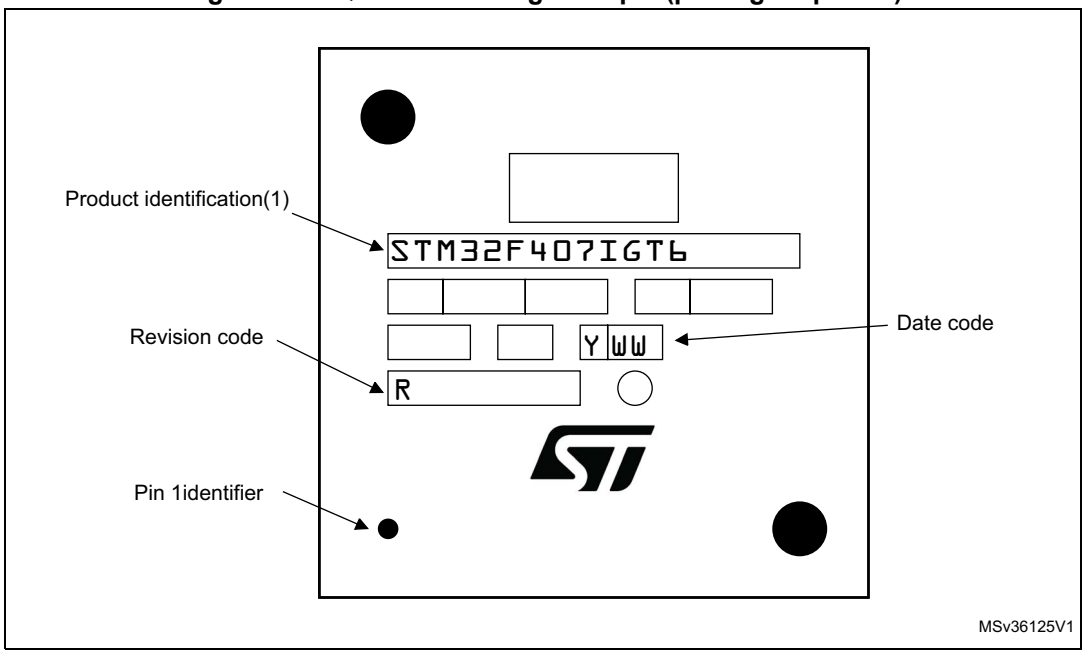


Device marking for LQFP176

The following figure gives an example of topside marking and pin 1 position identifier location.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 92. LQFP176 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.