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What is "Embedded - Microcontrollers"?

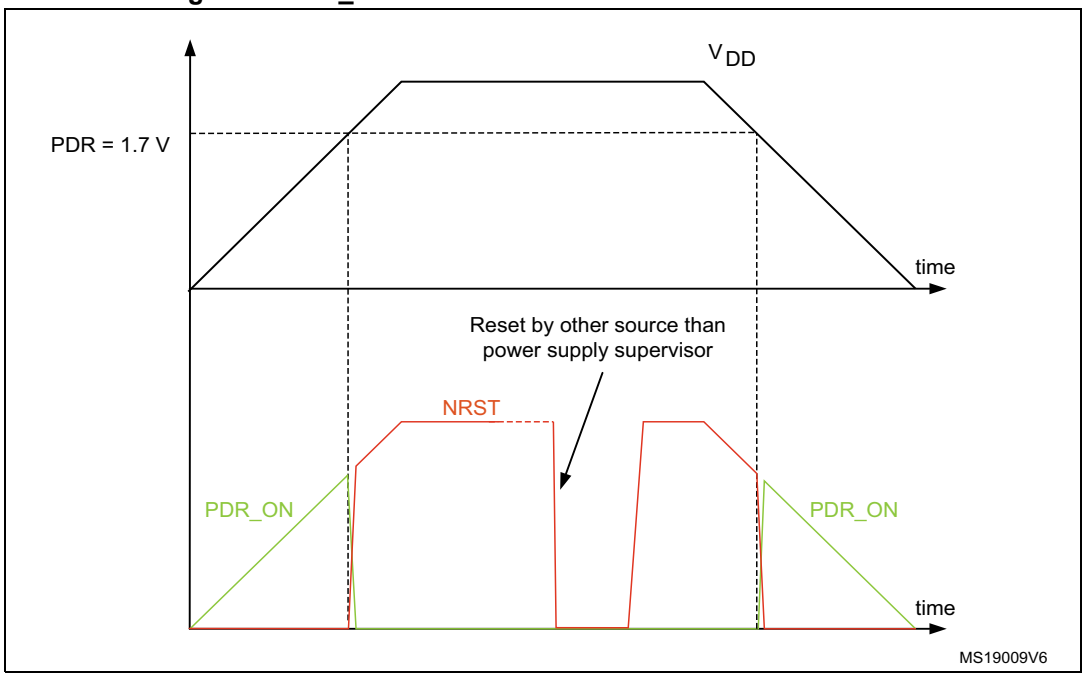
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	168MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f405vgt7

List of tables

Figure 8. PDR_ON and NRST control with internal reset OFF



1. PDR = 1.7 V for reduce temperature range; PDR = 1.8 V for all temperature range.

2.2.16 Voltage regulator

The regulator has four operating modes:

- Regulator ON
  - Main regulator mode (MR)
  - Low-power regulator (LPR)
  - Power-down
- Regulator OFF

Regulator ON

On packages embedding the BYPASS_REG pin, the regulator is enabled by holding BYPASS_REG low. On all other packages, the regulator is always enabled.

There are three power modes configured by software when regulator is ON:

- MR is used in the nominal regulation mode (With different voltage scaling in Run)

  In Main regulator mode (MR mode), different voltage scaling are provided to reach the best compromise between maximum frequency and dynamic power consumption. Refer to *Table 14: General operating conditions*.
- LPR is used in the Stop modes

  The LP regulator mode is configured by software when entering Stop mode.
- Power-down is used in Standby mode.

  The Power-down mode is activated only when entering in Standby mode. The regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption. The contents of the registers and SRAM are lost)

Table 5. USART feature comparison

USART name	Standard features	Modem (RTS/ CTS)	LIN	SPI master	irDA	Smartcard (ISO 7816)	Max. baud rate in Mbit/s (oversampling by 16)	Max. baud rate in Mbit/s (oversampling by 8)	APB mapping
USART1	X	X	X	X	X	X	5.25	10.5	APB2 (max. 84 MHz)
USART2	X	X	X	X	X	X	2.62	5.25	APB1 (max. 42 MHz)
USART3	X	X	X	X	X	X	2.62	5.25	APB1 (max. 42 MHz)
UART4	X	-	X	-	X	-	2.62	5.25	APB1 (max. 42 MHz)
UART5	X	-	X	-	X	-	2.62	5.25	APB1 (max. 42 MHz)
USART6	X	X	X	X	X	X	5.25	10.5	APB2 (max. 84 MHz)

2.2.24 Serial peripheral interface (SPI)

The STM32F40xxx feature up to three SPIs in slave and master modes in full-duplex and simplex communication modes. SPI1 can communicate at up to 42 Mbits/s, SPI2 and SPI3 can communicate at up to 21 Mbit/s. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes. All SPIs can be served by the DMA controller.

The SPI interface can be configured to operate in TI mode for communications in master mode and slave mode.

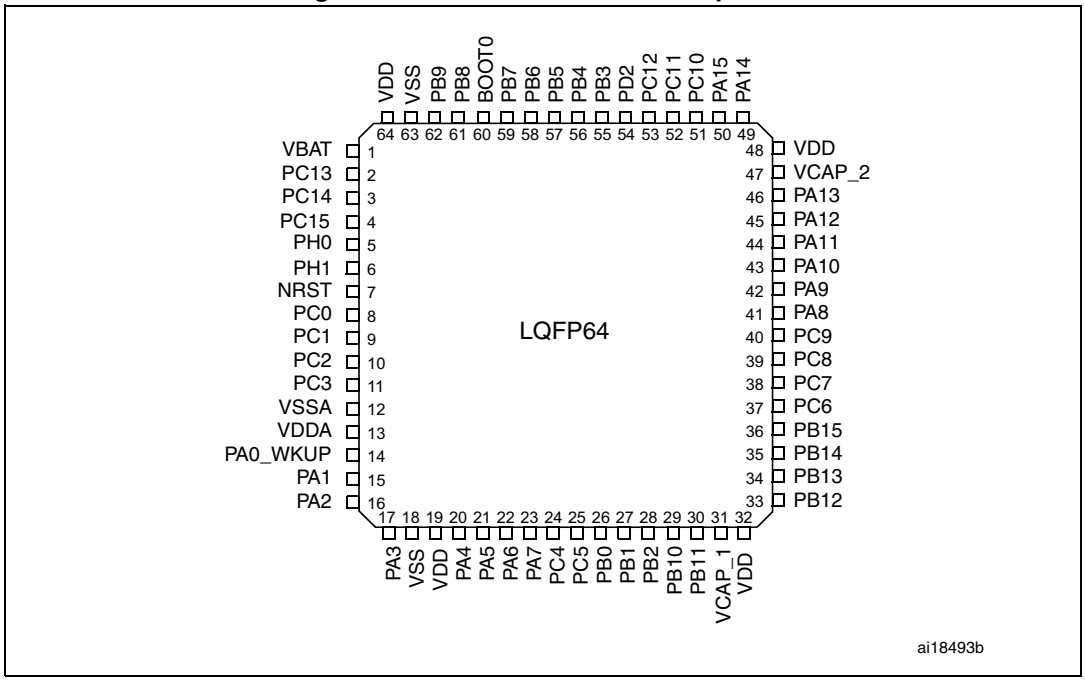
2.2.25 Inter-integrated sound (I^2S)

Two standard I^2S interfaces (multiplexed with SPI2 and SPI3) are available. They can be operated in master or slave mode, in full duplex and half-duplex communication modes, and can be configured to operate with a 16-/32-bit resolution as an input or output channel. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I^2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

All I^2Sx can be served by the DMA controller.

3 Pinouts and pin description

Figure 12. STM32F40xxx LQFP64 pinout



1. The above figure shows the package top view.

Table 7. STM32F40xxx pin and ball definitions (continued)

Pin number						Pin name (function after reset)[1]	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP64	WLCSP90	LQFP100	LQFP144	UFBGA176	LQFP176						
-	-	60	82	M15	101	PD13	I/O	FT	-	FSMC_A18/TIM4_CH2/ EVENTOUT	-
-	-	-	83	-	102	V_{SS}	S		-	-	-
-	-	-	84	J13	103	V_{DD}	S		-	-	-
-	F2	61	85	M14	104	PD14	I/O	FT	-	FSMC_D0/TIM4_CH3/ EVENTOUT/ EVENTOUT	-
-	F1	62	86	L14	105	PD15	I/O	FT	-	FSMC_D1/TIM4_CH4/ EVENTOUT	-
-	-	-	87	L15	106	PG2	I/O	FT	-	FSMC_A12/ EVENTOUT	-
-	-	-	88	K15	107	PG3	I/O	FT	-	FSMC_A13/ EVENTOUT	-
-	-	-	89	K14	108	PG4	I/O	FT	-	FSMC_A14/ EVENTOUT	-
-	-	-	90	K13	109	PG5	I/O	FT	-	FSMC_A15/ EVENTOUT	-
-	-	-	91	J15	110	PG6	I/O	FT	-	FSMC_INT2/ EVENTOUT	-
-	-	-	92	J14	111	PG7	I/O	FT	-	FSMC_INT3 /USART6_CK/ EVENTOUT	-
-	-	-	93	H14	112	PG8	I/O	FT	-	USART6_RTS / ETH_PPS_OUT/ EVENTOUT	-
-	-	-	94	G12	113	V_{SS}	S		-	-	-
-	-	-	95	H13	114	V_{DD}	S		-	-	-
37	F3	63	96	H15	115	PC6	I/O	FT	-	I2S2_MCK / TIM8_CH1/SDIO_D6 / USART6_TX / DCMI_D0/TIM3_CH1/ EVENTOUT	-
38	E1	64	97	G15	116	PC7	I/O	FT	-	I2S3_MCK / TIM8_CH2/SDIO_D7 / USART6_RX / DCMI_D1/TIM3_CH2/ EVENTOUT	-
39	E2	65	98	G14	117	PC8	I/O	FT	-	TIM8_CH3/SDIO_D0 /TIM3_CH3/ USART6_CK / DCMI_D2/ EVENTOUT	-

Table 7. STM32F40xxx pin and ball definitions (continued)

Pin number						Pin name (function after reset)[1]	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP64	WLCSP90	LQFP100	LQFP144	UFBGA176	LQFP176						
-	A4	85	118	D10	146	PD4	I/O	FT	-	FSMC_NOE/ USART2_RTS/ EVENTOUT	-
-	C6	86	119	C11	147	PD5	I/O	FT	-	FSMC_NWE/USART2_TX/ EVENTOUT	-
-	-	-	120	D8	148	V_{SS}	S	-	-	-	-
-	-	-	121	C8	149	V_{DD}	S	-	-	-	-
-	B5	87	122	B11	150	PD6	I/O	FT	-	FSMC_NWAIT/ USART2_RX/ EVENTOUT	-
-	A5	88	123	A11	151	PD7	I/O	FT	-	USART2_CK/FSMC_NE1/ FSMC_NCE2/ EVENTOUT	-
-	-	-	124	C10	152	PG9	I/O	FT	-	USART6_RX / FSMC_NE2/FSMC_NCE3/ EVENTOUT	-
-	-	-	125	B10	153	PG10	I/O	FT	-	FSMC_NCE4_1/ FSMC_NE3/ EVENTOUT	-
-	-	-	126	B9	154	PG11	I/O	FT	-	FSMC_NCE4_2 / ETH_MII_TX_EN/ ETH _RMII_TX_EN/ EVENTOUT	-
-	-	-	127	B8	155	PG12	I/O	FT	-	FSMC_NE4 / USART6_RTS/ EVENTOUT	-
-	-	-	128	A8	156	PG13	I/O	FT	-	FSMC_A24 / USART6_CTS /ETH_MII_TXD0/ ETH_RMII_TXD0/ EVENTOUT	-
-	-	-	129	A7	157	PG14	I/O	FT	-	FSMC_A25 / USART6_TX /ETH_MII_TXD1/ ETH_RMII_TXD1/ EVENTOUT	-
-	E8	-	130	D7	158	V_{SS}	S	-	-	-	-
-	F7	-	131	C7	159	V_{DD}	S	-	-	-	-
-	-	-	132	B7	160	PG15	I/O	FT	-	USART6_CTS / DCMI_D13/ EVENTOUT	-

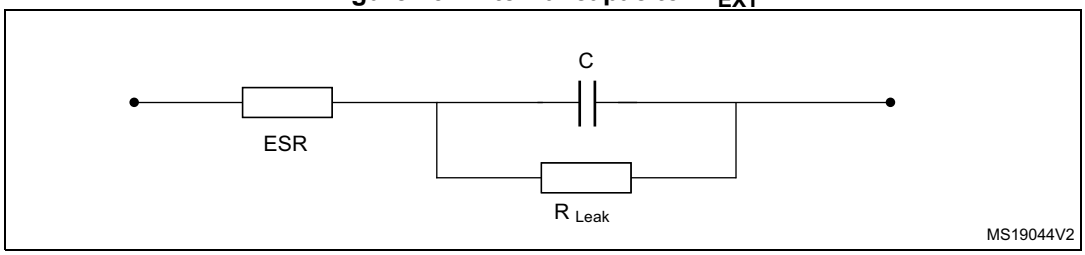
Table 10. register boundary addresses

Bus	Boundary address	Peripheral
	0xE00F FFFF - 0xFFFF FFFF	Reserved
Cortex-M4	0xE000 0000 - 0xE00F FFFF	Cortex-M4 internal peripherals
	0xA000 1000 - 0xDFFF FFFF	Reserved
AHB3	0xA000 0000 - 0xA000 0FFF	FSMC control register
	0x9000 0000 - 0x9FFF FFFF	FSMC bank 4
	0x8000 0000 - 0x8FFF FFFF	FSMC bank 3
	0x7000 0000 - 0x7FFF FFFF	FSMC bank 2
	0x6000 0000 - 0x6FFF FFFF	FSMC bank 1
	0x5006 0C00- 0x5FFF FFFF	Reserved
AHB2	0x5006 0800 - 0x5006 0BFF	RNG
	0x5005 0400 - 0x5006 07FF	Reserved
	0x5005 0000 - 0x5005 03FF	DCMI
	0x5004 0000- 0x5004 FFFF	Reserved
	0x5000 0000 - 0x5003 FFFF	USB OTG FS
	0x4008 0000- 0x4FFF FFFF	Reserved

5.3.2 V_{CAP_1}/V_{CAP_2} external capacitor

Stabilization for the main regulator is achieved by connecting an external capacitor C_{EXT} to the V_{CAP_1}/V_{CAP_2} pins. C_{EXT} is specified in *Table 16*.

Figure 23. External capacitor C_{EXT}



1. Legend: ESR is the equivalent series resistance.

Table 16. V_{CAP_1}/V_{CAP_2} operating conditions(1)

Symbol	Parameter	Conditions
CEXT	Capacitance of external capacitor	2.2 µF
ESR	ESR of external capacitor	< 2 Ω

1. When bypassing the voltage regulator, the two 2.2 µF V_{CAP} capacitors are not required and should be replaced by two 100 nF decoupling capacitors.

5.3.3 Operating conditions at power-up / power-down (regulator ON)

Subject to general operating conditions for T_A.

Table 17. Operating conditions at power-up / power-down (regulator ON)

Symbol	Parameter	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	20	∞	µs/V
	V_{DD} fall time rate	20	∞	

5.3.4 Operating conditions at power-up / power-down (regulator OFF)

Subject to general operating conditions for T_A.

Table 18. Operating conditions at power-up / power-down (regulator OFF)(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	Power-up	20	∞	µs/V
	V_{DD} fall time rate	Power-down	20	∞	
t_{VCAP}	V_{CAP_1} and V_{CAP_2} rise time rate	Power-up	20	∞	
	V_{CAP_1} and V_{CAP_2} fall time rate	Power-down	20	∞	

1. To reset the internal logic at power-down, a reset must be applied on pin PA0 when V_{DD} reach below minimum value of V_{12}.

Table 22. Typical and maximum current consumption in Sleep mode

Symbol	Parameter	Conditions	f_{HCLK}	Typ	Max(1)		Unit
				T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Sleep mode	External clock(2), all peripherals enabled(3)	168 MHz	59	77	84	mA
			144 MHz	46	61	67	
			120 MHz	38	53	60	
			90 MHz	30	44	51	
			60 MHz	20	34	41	
			30 MHz	11	24	31	
			25 MHz	8	21	28	
			16 MHz	6	18	25	
			8 MHz	3	16	23	
			4 MHz	2	15	22	
			2 MHz	2	14	21	
		External clock(2), all peripherals disabled	168 MHz	12	27	35	
			144 MHz	9	22	29	
			120 MHz	8	20	28	
			90 MHz	7	19	26	
			60 MHz	5	17	24	
			30 MHz	3	16	23	
			25 MHz	2	15	22	
			16 MHz	2	14	21	
			8 MHz	1	14	21	
			4 MHz	1	13	21	
			2 MHz	1	13	21	

1. Guaranteed by characterization, tested in production at V_{DD} max and f_{HCLK} max with peripherals enabled.
2. External clock is 4 MHz and PLL is on when f_{HCLK} > 25 MHz.
3. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application, executing EEMBC? code, is running. This emission test is compliant with SAE IEC61967-2 standard which specifies the test board and the pin loading.

Table 44. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{CPU}]	Unit
				25/168 MHz	
S_{EMI}	Peak level	V_{DD} = 3.3 V, T_A = 25 °C, LQFP176 package, conforming to SAE J1752/3 EEMBC, code running from Flash with ART accelerator enabled	0.1 to 30 MHz	32	dBµV
			30 to 130 MHz	25	
			130 MHz to 1GHz	29	
			SAE EMI Level	4	-
		V_{DD} = 3.3 V, T_A = 25 °C, LQFP176 package, conforming to SAE J1752/3 EEMBC, code running from Flash with ART accelerator and PLL spread spectrum enabled	0.1 to 30 MHz	19	dBµV
			30 to 130 MHz	16	
			130 MHz to 1GHz	18	
			SAE EMI level	3.5	-

5.3.14 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 45. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to JESD22-A114	2	2000(2)	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to ANSI/ESD STM5.3.1	II	500	

1. Guaranteed by characterization.
2. On V_{BAT} pin, $V_{ESD(HBM)}$ is limited to 1000 V.

Static latchup

Two complementary static tests are required on six parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latchup standard.

Table 46. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

5.3.15 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibilty to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of 5 µA/+0 µA range), or other functional failure (for example reset, oscillator frequency deviation).

Negative induced leakage current is caused by negative injection and positive induced leakage current by positive injection.

The test results are given in *Table 47*.

Table 61. USB HS clock timing parameters(1)

Parameter		Symbol	Min	Nominal	Max	Unit
Frequency (steady state) ±500 ppm		F_{STEADY}	59.97	60	60.03	MHz
Duty cycle (first transition)	8-bit ±10%	D_{START_8BIT}	40	50	60	%
Duty cycle (steady state) ±500 ppm		D_{STEADY}	49.975	50	50.025	%
Time to reach the steady state frequency and duty cycle after the first transition		T_{STEADY}	-	-	1.4	ms
Clock startup time after the de-assertion of SuspendM	Peripheral	T_{START_DEV}	-	-	5.6	ms
	Host	T_{START_HOST}	-	-	-	
PHY preparation time after the first transition of the input clock		T_{PREP}	-	-	-	µs

1. Guaranteed by design.

Table 62. ULPI timing

Parameter	Symbol	Value(1)		Unit
		Min.	Max.	
Control in (ULPI_DIR) setup time	t_{SC}	-	2.0	ns
Control in (ULPI_NXT) setup time		-	1.5	
Control in (ULPI_DIR, ULPI_NXT) hold time	t_{HC}	0	-	
Data in setup time	t_{SD}	-	2.0	
Data in hold time	t_{HD}	0	-	
Control out (ULPI_STP) setup time and hold time	t_{DC}	-	9.2	
Data out available from clock rising edge	t_{DD}	-	10.7	

1. V_{DD} = 2.7 V to 3.6 V and T_A = –40 to 85 °C.

Figure 45. ULPI timing diagram

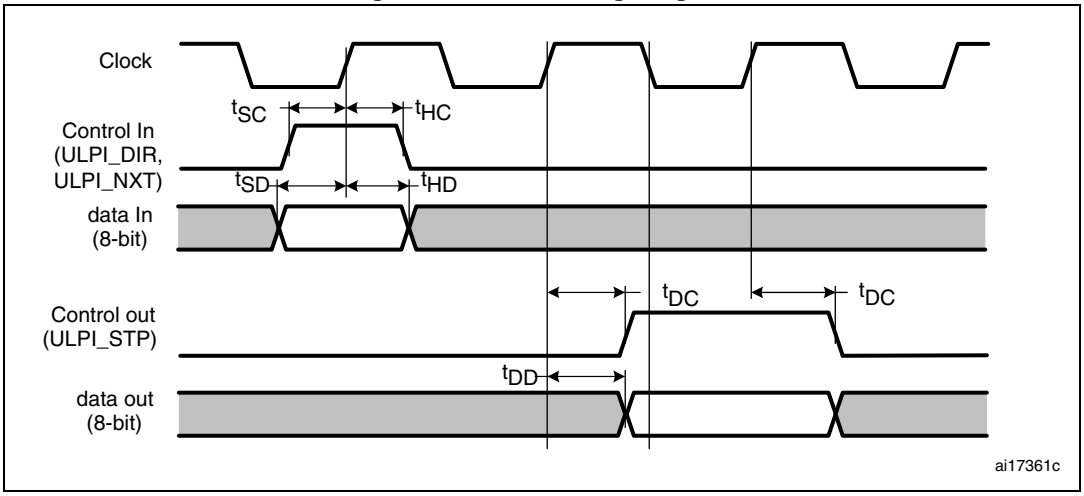
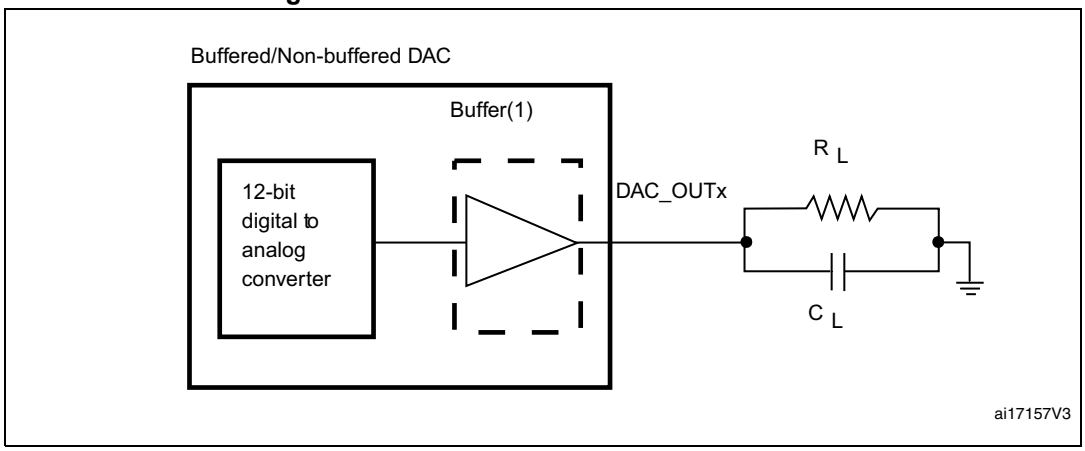


Figure 53. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

5.3.26 FSMC characteristics

Unless otherwise specified, the parameters given in *Table 75* to *Table 86* for the FSMC interface are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage conditions summarized in *Table 14*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to Section *Section 5.3.16: I/O port characteristics* for more details on the input/output characteristics.

Asynchronous waveforms and timings

Figure 54 through *Figure 57* represent asynchronous waveforms and *Table 75* through *Table 78* provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- AddressSetupTime = 1
- AddressHoldTime = 0x1
- DataSetupTime = 0x1
- BusTurnAroundDuration = 0x0

In all timing tables, the T_{HCLK} is the HCLK clock period.

Figure 61. Synchronous non-multiplexed PSRAM write timings

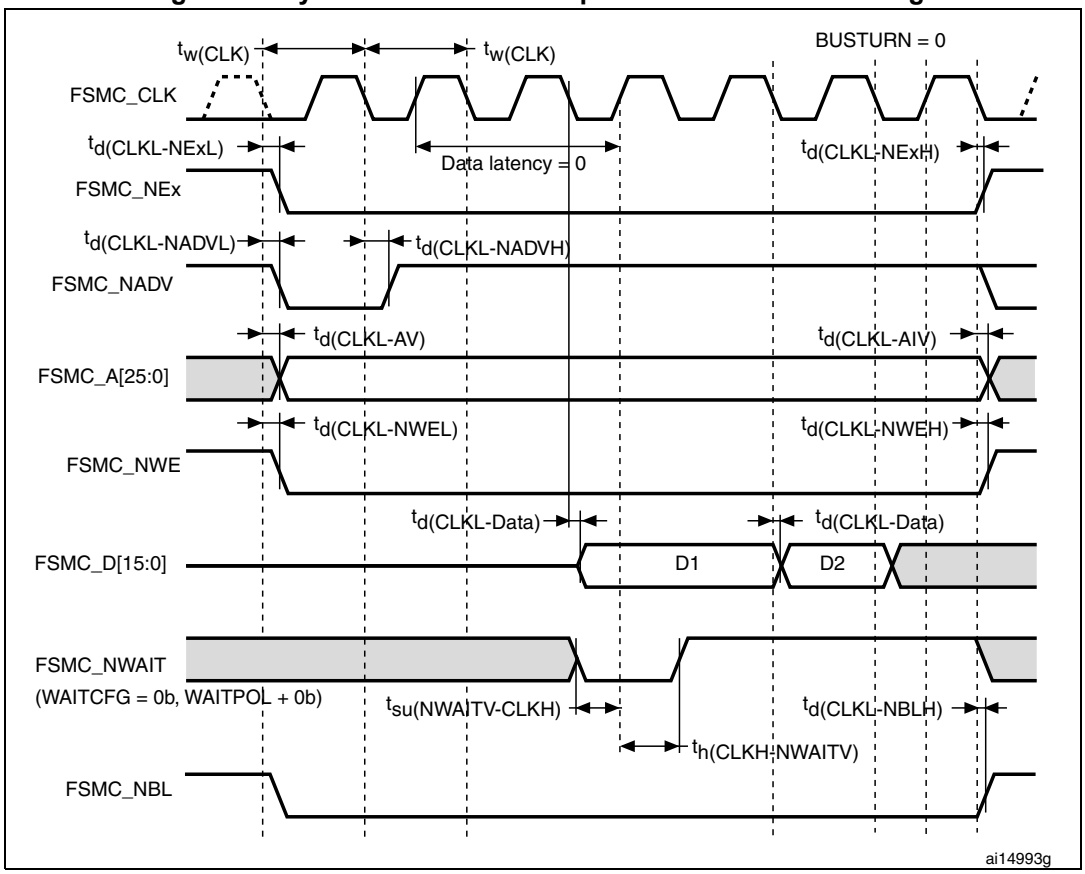


Table 82. Synchronous non-multiplexed PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	$2T_{HCLK}$	-	ns
$t^{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x=0..2)	-	1	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x= 0…2)	1	-	ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	7	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	6	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x=16…25)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x=16…25)	6	-	ns
$t_{d(CLKL-NWEL)}$	FSMC_CLK low to FSMC_NWE low	-	1	ns
$t_{d(CLKL-NWEH)}$	FSMC_CLK low to FSMC_NWE high	2	-	ns
$t_{d(CLKL-Data)}$	FSMC_D[15:0] valid data after FSMC_CLK low	-	3	ns
$t_{d(CLKL-NBLH)}$	FSMC_CLK low to FSMC_NBL high	3	-	ns
$t_{su(NWAIT-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	4	-	ns
$t_{h(CLKH-NWAIT)}$	FSMC_NWAIT valid after FSMC_CLK high	0	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization.

Figure 68. NAND controller waveforms for read access

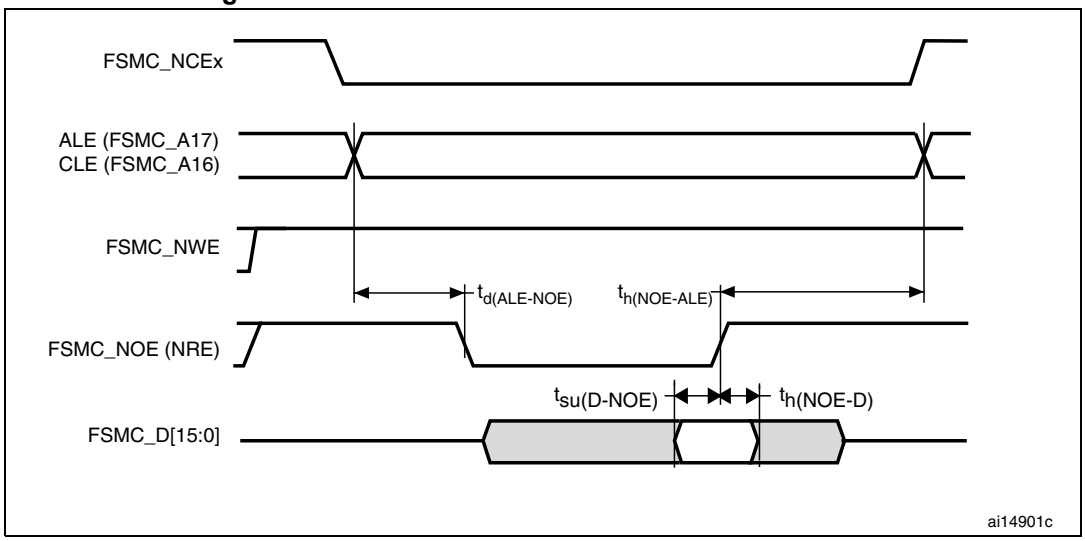


Figure 69. NAND controller waveforms for write access

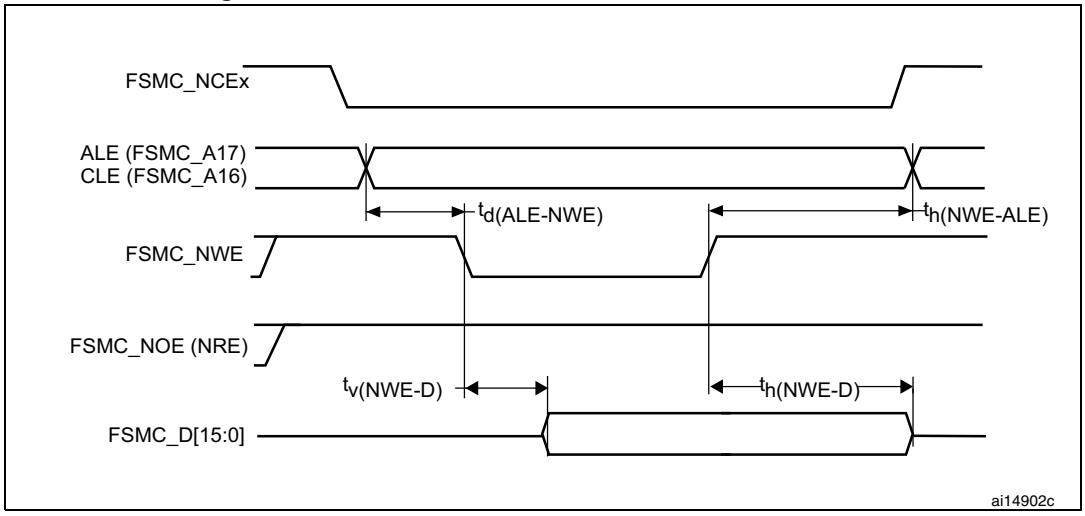


Table 86. Switching characteristics for NAND Flash write cycles(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NWE)}$	FSMC_NWE low width	$4T_{HCLK}-1$	$4T_{HCLK}+3$	ns
$t_{v(NWE-D)}$	FSMC_NWE low to FSMC_D[15-0] valid	-	0	ns
$t_{h(NWE-D)}$	FSMC_NWE high to FSMC_D[15-0] invalid	$3T_{HCLK}-2$	-	ns
$t_{d(D-NWE)}$	FSMC_D[15-0] valid before FSMC_NWE high	$5T_{HCLK}-3$	-	ns
$t_{d(ALE-NWE)}$	FSMC_ALE valid before FSMC_NWE low	-	$3T_{HCLK}$	ns
$t_{h(NWE-ALE)}$	FSMC_NWE high to FSMC_ALE invalid	$3T_{HCLK}-2$	-	ns

1. C_L = 30 pF.

5.3.27 Camera interface (DCMI) timing specifications

Unless otherwise specified, the parameters given in *Table 87* for DCMI are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage summarized in *Table 13*, with the following configuration:

- PCK polarity: falling
- VSYNC and HSYNC polarity: high
- Data format: 14 bits

Figure 72. DCMI timing diagram

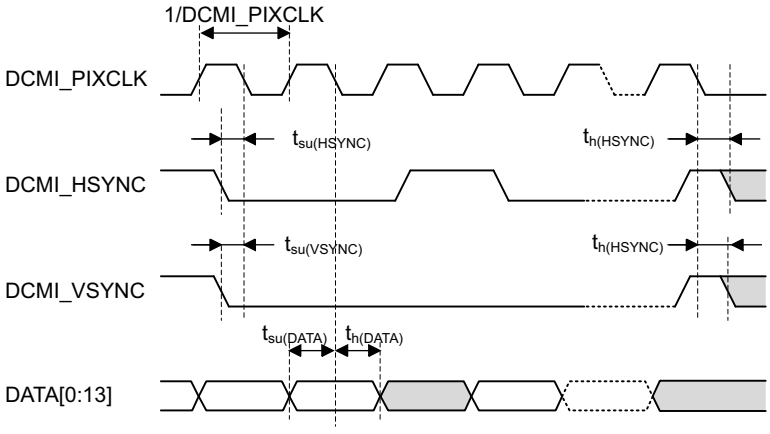


Table 87. DCMI characteristics(1)

Symbol	Parameter	Min	Max	Unit
	Frequency ratio DCMI_PIXCLK/f_{HCLK}	-	0.4	
DCMI_PIXCLK	Pixel clock input	-	54	MHz
D_{pixel}	Pixel clock input duty cycle	30	70	%

Table 91. WLCSP90 recommended PCB design rules

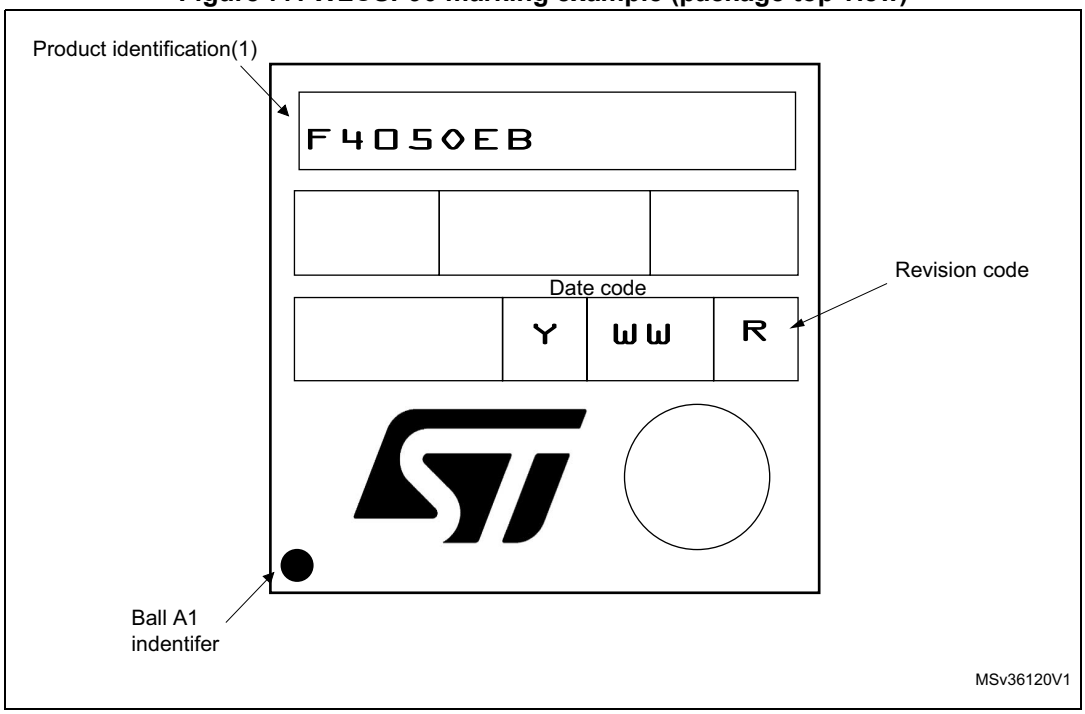
Dimension	Recommended values
Pitch	0.4 mm
Dpad	260 µm max. (circular) 220 µm recommended
Dsm	300 µm min. (for 260 µm diameter pad)
PCB pad design	Non-solder mask defined via underbump allowed

Device marking for WLCSP90

The following figure gives an example of topside marking and ball A1 position identifier location.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 77. WLCSP90 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Table 100. Document revision history (continued)

Date	Revision	Changes
24-Jan-2012	2 (continued)	Added V_{12} in *Table 19: Embedded reset and power control block characteristics*. Updated *Table 21: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled)* and *Table 20: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled) or RAM*. Added *Figure* , *Figure 25*, *Figure 26*, and *Figure 27*. Updated *Table 22: Typical and maximum current consumption in Sleep mode* and removed Note 1. Updated *Table 23: Typical and maximum current consumptions in Stop mode* and *Table 24: Typical and maximum current consumptions in Standby mode*, *Table 25: Typical and maximum current consumptions in VBAT mode*, and *Table 27: Switching output I/O current consumption*. *Section : On-chip peripheral current consumption*: modified conditions, and updated *Table 28: Peripheral current consumption* and *Note 2*. Changed f_{HSE_ext} to 50 MHz and $t_{r(HSE)}/t_{f(HSE)}$ maximum value in *Table 30: High-speed external user clock characteristics*. Added $C_{in(LSE)}$ in *Table 31: Low-speed external user clock characteristics*. Updated maximum PLL input clock frequency, removed related note, and deleted jitter for MCO for RMII Ethernet typical value in *Table 36: Main PLL characteristics*. Updated maximum PLLI2S input clock frequency and removed related note in *Table 37: PLLI2S (audio PLL) characteristics*. Updated *Section : Flash memory* to specify that the devices are shipped to customers with the Flash memory erased. Updated *Table 39: Flash memory characteristics*, and added t_{ME} in *Table 40: Flash memory programming*. Updated *Table 43: EMS characteristics*, and *Table 44: EMI characteristics*. Updated *Table 56: I2S dynamic characteristics* Updated *Figure 45: ULPI timing diagram* and *Table 62: ULPI timing*. Added $t_{COUNTER}$ and t_{MAX_COUNT} in *Table 52: Characteristics of TIMx connected to the APB1 domain* and *Table 53: Characteristics of TIMx connected to the APB2 domain*. Updated *Table 65: Dynamic characteristics: Ethernet MAC signals for RMII*. Removed USB-IF certification in *Section : USB OTG FS characteristics*.

Table 100. Document revision history (continued)

Date	Revision	Changes
24-Jan-2012	2 (continued)	Updated *Table 61: USB HS clock timing parameters* Updated *Table 67: ADC characteristics*. Updated *Table 68: ADC accuracy at fADC = 30 MHz*. Updated *Note 1* in *Table 74: DAC characteristics*. *Section 5.3.26: FSMC characteristics*: updated *Table 75* to *Table 86*, changed C_L value to 30 pF, and modified FSMC configuration for asynchronous timings and waveforms. Updated *Figure 59: Synchronous multiplexed PSRAM write timings*. Updated *Table 98: Package thermal characteristics*. Appendix *A.1: USB OTG full speed (FS) interface solutions*: modified *Figure 93: USB controller configured as peripheral-only and used in Full speed mode* added *Note 2*, updated *Figure 94: USB controller configured as host-only and used in full speed mode* and added *Note 2*, changed *Figure 95: USB controller configured in dual mode and used in full speed mode* and added *Note 3*. Appendix *A.2: USB OTG high speed (HS) interface solutions*: removed figures *USB OTG HS device-only connection in FS mode* and *USB OTG HS host-only connection in FS mode, and updated Figure 96: USB controller configured as peripheral, host, or dual-mode and used in high speed mode* and added *Note 2*. Added Appendix *A.3: Ethernet interface solutions*.

Table 100. Document revision history (continued)

Date	Revision	Changes
31-May-2012	3 (continued)	Removed f_{HSE_ext} typical value in *Table 30: High-speed external user clock characteristics*. Updated *Table 32: HSE 4-26 MHz oscillator characteristics* and *Table 33: LSE oscillator characteristics (fLSE = 32.768 kHz)*. Added f_{PLL48_OUT} maximum value in *Table 36: Main PLL characteristics*. Modified equation 1 and 2 in *Section 5.3.11: PLL spread spectrum clock generation (SSCG) characteristics*. Updated *Table 39: Flash memory characteristics*, *Table 40: Flash memory programming*, and *Table 41: Flash memory programming with VPP*. Updated *Section : Output driving current*. *Table 56: I^2C characteristics*: *Note 4* updated and applied to $t_{h(SDA)}$ in Fast mode, and removed note 4 related to $t_{h(SDA)}$ minimum value. Updated *Table 67: ADC characteristics*. Updated note concerning ADC accuracy vs. negative injection current below *Table 68: ADC accuracy at fADC = 30 MHz*. Added WLCSP90 thermal resistance in *Table 98: Package thermal characteristics*. Updated *Table 90: WLCSP90 - 4.223 x 3.969 mm, 0.400 mm pitch wafer level chip scale package mechanical data*. Updated *Figure 87: UFBGA176+25 ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package outline* and *Table 95: UFBGA176+25 ball, 10 × 10 × 0.65 mm pitch, ultra thin fine pitch ball grid array mechanical data*. Added *Figure 91: LQFP176 - 176-pin, 24 x 24 mm low profile quad flat recommended footprint*. Removed 256 and 768 Kbyte Flash memory density from *Table 99: Ordering information scheme*.