**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 168MHz |
| Connectivity | CANbus, EBI/EMI, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT |
| Number of I/O | 82 |
| Program Memory Size | 1MB (1M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 192K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 16x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-LQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f405vgt7tr |

### 2.2.5 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a software signature during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

### 2.2.6 Embedded SRAM

All STM32F40xxx products embed:

- Up to 192 Kbytes of system SRAM including 64 Kbytes of CCM (core coupled memory) data RAM

  RAM memory is accessed (read/write) at CPU clock speed with 0 wait states.
- 4 Kbytes of backup SRAM

  This area is accessible only from the CPU. Its content is protected against possible unwanted write accesses, and is retained in Standby or $V_{BAT}$ mode.

### 2.2.7 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs, Ethernet, USB HS) and the slaves (Flash memory, RAM, FSMC, AHB and APB peripherals) and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

Two external ceramic capacitors should be connected on $V_{CAP\_1}$ & $V_{CAP\_2}$ pin. Refer to *Figure 21: Power supply scheme* and *Figure 16: VCAP_1/VCAP_2 operating conditions*.

All packages have regulator ON feature.

### Regulator OFF

This feature is available only on packages featuring the BYPASS_REG pin. The regulator is disabled by holding BYPASS_REG high. The regulator OFF mode allows to supply externally a $V_{12}$ voltage source through $V_{CAP\_1}$ and $V_{CAP\_2}$ pins.

Since the internal voltage scaling is not manage internally, the external voltage value must be aligned with the targeted maximum frequency. Refer to *Table 14: General operating conditions*.

The two 2.2 µF ceramic capacitors should be replaced by two 100 nF decoupling capacitors.

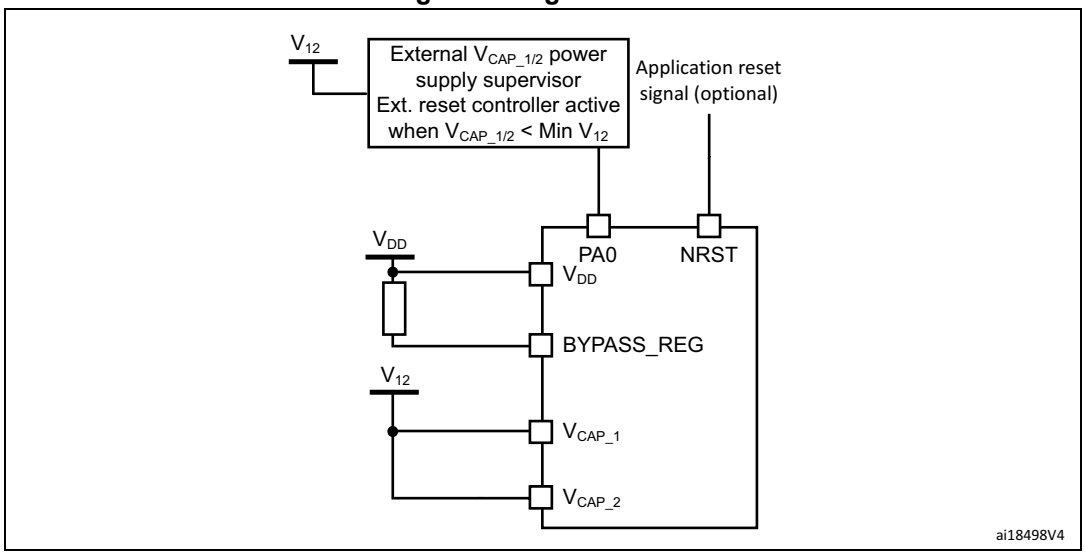
Refer to *Figure 21: Power supply scheme*

When the regulator is OFF, there is no more internal monitoring on $V_{12}$. An external power supply supervisor should be used to monitor the $V_{12}$ of the logic power domain. PA0 pin should be used for this purpose, and act as power-on reset on $V_{12}$ power domain.

In regulator OFF mode the following features are no more supported:

- PA0 cannot be used as a GPIO pin since it allows to reset a part of the $V_{12}$ logic power domain which is not reset by the NRST pin.
- As long as PA0 is kept low, the debug mode cannot be used under power-on reset. As a consequence, PA0 and NRST pins must be managed separately if the debug connection under reset or pre-reset is required.
- The standby mode is not available

**Figure 9. Regulator OFF**



### SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source.

## 2.2.22 Inter-integrated circuit interface (I²C)

Up to three I²C bus interfaces can operate in multimaster and slave modes. They can support the Standard-mode (up to 100 kHz) and Fast-mode (up to 400 kHz). They support the 7/10-bit addressing mode and the 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SMBus 2.0/PMBus.

## 2.2.23 Universal synchronous/asynchronous receiver transmitters (USART)

The STM32F405xx and STM32F407xx embed four universal synchronous/asynchronous receiver transmitters (USART1, USART2, USART3 and USART6) and two universal asynchronous receiver transmitters (UART4 and UART5).

These six interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability. The USART1 and USART6 interfaces are able to communicate at speeds of up to 10.5 Mbit/s. The other available interfaces communicate at up to 5.25 Mbit/s.

USART1, USART2, USART3 and USART6 also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller.

Table 5. USART feature comparison

| USART name | Standard features | Modem (RTS/ CTS) | LIN | SPI master | irDA | Smartcard (ISO 7816) | Max. baud rate in Mbit/s (oversampling by 16) | Max. baud rate in Mbit/s (oversampling by 8) | APB mapping |
|---|---|---|---|---|---|---|---|---|---|
| USART1 | X | X | X | X | X | X | 5.25 | 10.5 | APB2 (max. 84 MHz) |
| USART2 | X | X | X | X | X | X | 2.62 | 5.25 | APB1 (max. 42 MHz) |
| USART3 | X | X | X | X | X | X | 2.62 | 5.25 | APB1 (max. 42 MHz) |
| UART4 | X | - | X | - | X | - | 2.62 | 5.25 | APB1 (max. 42 MHz) |
| UART5 | X | - | X | - | X | - | 2.62 | 5.25 | APB1 (max. 42 MHz) |
| USART6 | X | X | X | X | X | X | 5.25 | 10.5 | APB2 (max. 84 MHz) |

### 2.2.24 Serial peripheral interface (SPI)

The STM32F40xxx feature up to three SPIs in slave and master modes in full-duplex and simplex communication modes. SPI1 can communicate at up to 42 Mbits/s, SPI2 and SPI3 can communicate at up to 21 Mbit/s. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes. All SPIs can be served by the DMA controller.

The SPI interface can be configured to operate in TI mode for communications in master mode and slave mode.

### 2.2.25 Inter-integrated sound ($I^2S$)

Two standard $I^2S$ interfaces (multiplexed with SPI2 and SPI3) are available. They can be operated in master or slave mode, in full duplex and half-duplex communication modes, and can be configured to operate with a 16-/32-bit resolution as an input or output channel. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the $I^2S$ interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

All $I^2Sx$ can be served by the DMA controller.

alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

The I/O configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

Fast I/O handling allowing maximum I/O toggling up to 84 MHz.

### 2.2.35 Analog-to-digital converters (ADCs)

Three 12-bit analog-to-digital converters are embedded and each ADC shares up to 16 external channels, performing conversions in the single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold

The ADC can be served by the DMA controller. An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

To synchronize A/D conversion and timers, the ADCs could be triggered by any of TIM1, TIM2, TIM3, TIM4, TIM5, or TIM8 timer.

### 2.2.36 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 1.8 V and 3.6 V. The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

As the offset of the temperature sensor varies from chip to chip due to process variation, the internal temperature sensor is mainly suitable for applications that detect temperature changes instead of absolute temperatures. If an accurate temperature reading is needed, then an external temperature sensor part should be used.

### 2.2.37 Digital-to-analog converter (DAC)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- external triggers for conversion
- input voltage reference $V_{REF+}$

Eight DAC trigger inputs are used in the device. The DAC channels are triggered through the timer update outputs that are also connected to different DMA streams.

### 2.2.38 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

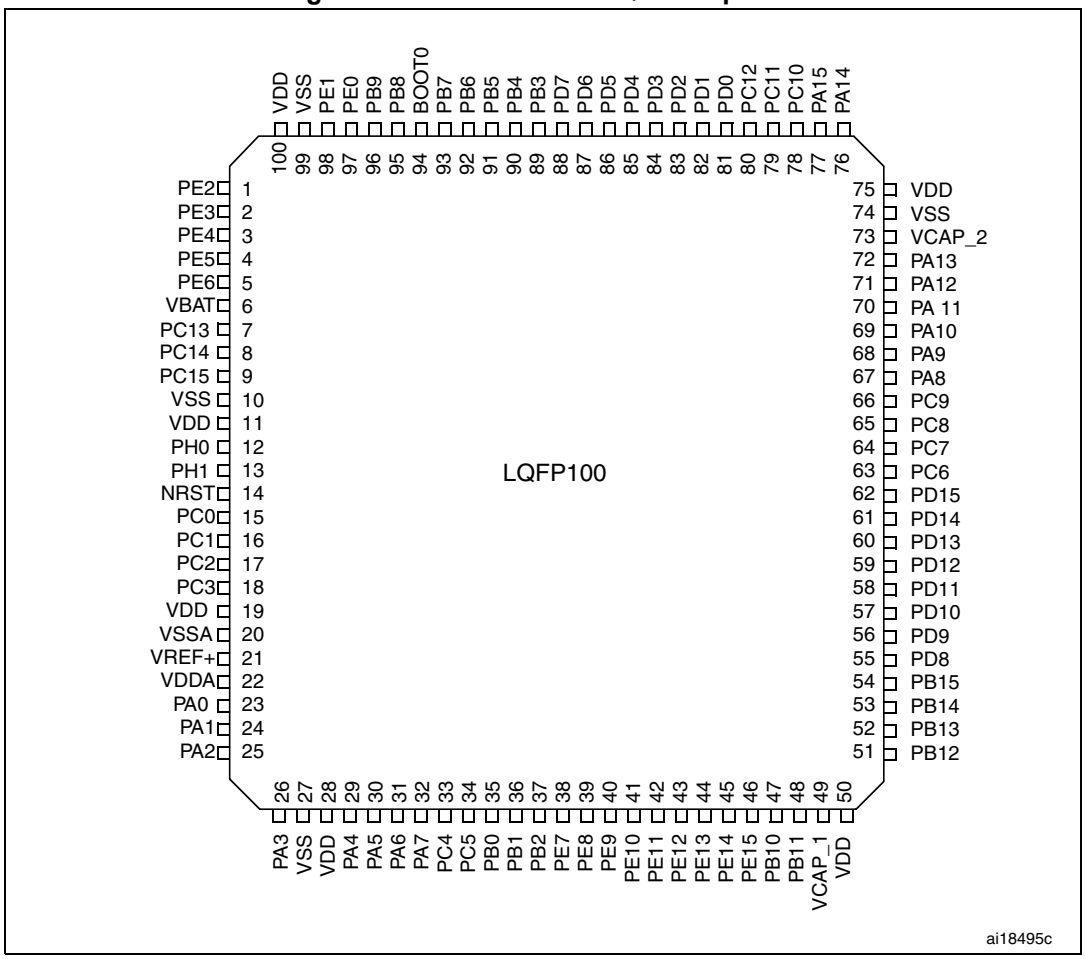
Debug is performed using 2 pins only instead of 5 required by the JTAG (JTAG pins could be re-use as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

### 2.2.39 Embedded Trace Macrocell™

The ARM Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F40xxx through a small number of ETM pins to an external hardware trace port analyser (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

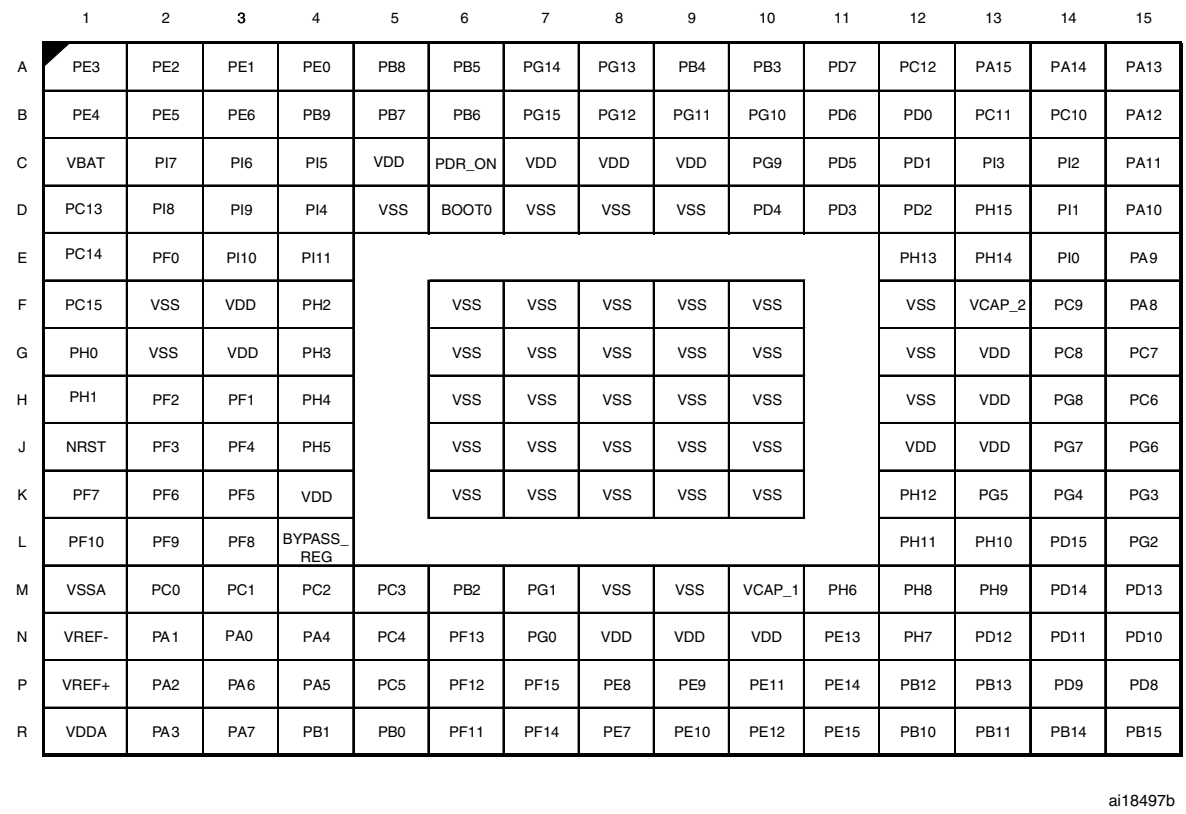
The Embedded Trace Macrocell operates with third party debugger software tools.

**Figure 13. STM32F40xxx LQFP100 pinout**




1. The above figure shows the package top view.

**Figure 16. STM32F40xxx UFBGA176 ballout**




1. This figure shows the package top view.

## Table 9. Alternate function mapping (continued)

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2 | TIM3/4/5 | TIM8/9/10/11 | I2C1/2/3 | SPI1/SPI2/I2S2/I2S2ext | SPI3/I2Sext/I2S3 | USART1/2/3/I2S3ext | UART4/5/USART6 | CAN1/2 TIM12/13/14 | OTG_FS/OTG_HS | ETH | FSMC/SDIO/OTG_FS | DCMI | | |
| Port E | PE0 | - | - | TIM4_ETR | - | - | - | - | - | - | - | - | - | FSMC_NBL0 | DCMI_D2 | - | EVENTOUT |
| | PE1 | - | - | - | - | - | - | - | - | - | - | - | - | FSMC_NBL1 | DCMI_D3 | - | EVENTOUT |
| | PE2 | TRACECLK | - | - | - | - | - | - | - | - | - | - | ETH _MII_TXD3 | FSMC_A23 | - | - | EVENTOUT |
| | PE3 | TRACED0 | - | - | - | - | - | - | - | - | - | - | - | FSMC_A19 | - | - | EVENTOUT |
| | PE4 | TRACED1 | - | - | - | - | - | - | - | - | - | - | - | FSMC_A20 | DCMI_D4 | - | EVENTOUT |
| | PE5 | TRACED2 | - | - | TIM9_CH1 | - | - | - | - | - | - | - | - | FSMC_A21 | DCMI_D6 | - | EVENTOUT |
| | PE6 | TRACED3 | - | - | TIM9_CH2 | - | - | - | - | - | - | - | - | FSMC_A22 | DCMI_D7 | - | EVENTOUT |
| | PE7 | - | TIM1_ETR | - | - | - | - | - | - | - | - | - | - | FSMC_D4 | - | - | EVENTOUT |
| | PE8 | - | TIM1_CH1N | - | - | - | - | - | - | - | - | - | - | FSMC_D5 | - | - | EVENTOUT |
| | PE9 | - | TIM1_CH1 | - | - | - | - | - | - | - | - | - | - | FSMC_D6 | - | - | EVENTOUT |
| | PE10 | - | TIM1_CH2N | - | - | - | - | - | - | - | - | - | - | FSMC_D7 | - | - | EVENTOUT |
| | PE11 | - | TIM1_CH2 | - | - | - | - | - | - | - | - | - | - | FSMC_D8 | - | - | EVENTOUT |
| | PE12 | - | TIM1_CH3N | - | - | - | - | - | - | - | - | - | - | FSMC_D9 | - | - | EVENTOUT |
| | PE13 | - | TIM1_CH3 | - | - | - | - | - | - | - | - | - | - | FSMC_D10 | - | - | EVENTOUT |
| | PE14 | - | TIM1_CH4 | - | - | - | - | - | - | - | - | - | - | FSMC_D11 | - | - | EVENTOUT |
| | PE15 | - | TIM1_BKIN | - | - | - | - | - | - | - | - | - | - | FSMC_D12 | - | - | EVENTOUT |

**Table 14. General operating conditions (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{12}$ | Regulator ON: 1.2 V internal voltage on $V_{CAP\_1}/V_{CAP\_2}$ pins | VOS bit in PWR_CR register = 0(1) Max frequency 144MHz | 1.08 | 1.14 | 1.20 | V |
| | | VOS bit in PWR_CR register= 1 Max frequency 168MHz | 1.20 | 1.26 | 1.32 | V |
| | Regulator OFF: 1.2 V external voltage must be supplied from external regulator on $V_{CAP\_1}/V_{CAP\_2}$ pins | Max frequency 144MHz | 1.10 | 1.14 | 1.20 | V |
| | | Max frequency 168MHz | 1.20 | 1.26 | 1.30 | V |
| $V_{IN}$ | Input voltage on RST and FT pins(6) | 2 V ≤ $V_{DD}$ ≤ 3.6 V | –0.3 | - | 5.5 | V |
| | | $V_{DD}$ ≤ 2 V | –0.3 | - | 5.2 | |
| | Input voltage on TTa pins | - | –0.3 | - | $V_{DDA}$+ 0.3 | |
| | Input voltage on B pin | - | - | - | 5.5 | |
| $P_D$ | Power dissipation at $T_A$ = 85 °C for suffix 6 or $T_A$ = 105 °C for suffix 7(7) | LQFP64 | - | - | 435 | mW |
| | | LQFP100 | - | - | 465 | |
| | | LQFP144 | - | - | 500 | |
| | | LQFP176 | - | - | 526 | |
| | | UFBGA176 | - | - | 513 | |
| | | WLCSP90 | - | - | 543 | |
| $T_A$ | Ambient temperature for 6 suffix version | Maximum power dissipation | –40 | - | 85 | °C |
| | | Low-power dissipation(8) | –40 | - | 105 | |
| | Ambient temperature for 7 suffix version | Maximum power dissipation | –40 | - | 105 | °C |
| | | Low-power dissipation(8) | –40 | - | 125 | |
| $T_J$ | Junction temperature range | 6 suffix version | –40 | - | 105 | °C |
| | | 7 suffix version | –40 | - | 125 | |

1. The average expected gain in power consumption when VOS = 0 compared to VOS = 1 is around 10% for the whole temperature range, when the system clock frequency is between 30 and 144 MHz.
2. $V_{DD}/V_{DDA}$ minimum value of 1.7 V is obtained when the device operates in reduced temperature range, and with the use of an external power supply supervisor (refer to *Section : Internal reset OFF*).
3. When the ADC is used, refer to *Table 67: ADC characteristics*.
4. If $V_{REF+}$ pin is present, it must respect the following condition: $V_{DDA}$-$V_{REF+}$ < 1.2 V.
5. It is recommended to power $V_{DD}$ and $V_{DDA}$ from the same source. A maximum difference of 300 mV between $V_{DD}$ and $V_{DDA}$ can be tolerated during power-up and power-down operation.
6. To sustain a voltage higher than $V_{DD}$+0.3, the internal pull-up and pull-down resistors must be disabled.
7. If $T_A$ is lower, higher $P_D$ values are allowed as long as $T_J$ does not exceed $T_{Jmax}$.
8. In low-power dissipation state, $T_A$ can be extended to this range as long as $T_J$ does not exceed $T_{Jmax}$.

### 5.3.5 Embedded reset and power control block characteristics

The parameters given in *Table 19* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 14*.

**Table 19. Embedded reset and power control block characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{PVD}$ | Programmable voltage detector level selection | PLS[2:0]=000 (rising edge) | 2.09 | 2.14 | 2.19 | V |
| | | PLS[2:0]=000 (falling edge) | 1.98 | 2.04 | 2.08 | V |
| | | PLS[2:0]=001 (rising edge) | 2.23 | 2.30 | 2.37 | V |
| | | PLS[2:0]=001 (falling edge) | 2.13 | 2.19 | 2.25 | V |
| | | PLS[2:0]=010 (rising edge) | 2.39 | 2.45 | 2.51 | V |
| | | PLS[2:0]=010 (falling edge) | 2.29 | 2.35 | 2.39 | V |
| | | PLS[2:0]=011 (rising edge) | 2.54 | 2.60 | 2.65 | V |
| | | PLS[2:0]=011 (falling edge) | 2.44 | 2.51 | 2.56 | V |
| | | PLS[2:0]=100 (rising edge) | 2.70 | 2.76 | 2.82 | V |
| | | PLS[2:0]=100 (falling edge) | 2.59 | 2.66 | 2.71 | V |
| | | PLS[2:0]=101 (rising edge) | 2.86 | 2.93 | 2.99 | V |
| | | PLS[2:0]=101 (falling edge) | 2.65 | 2.84 | 2.92 | V |
| | | PLS[2:0]=110 (rising edge) | 2.96 | 3.03 | 3.10 | V |
| | | PLS[2:0]=110 (falling edge) | 2.85 | 2.93 | 2.99 | V |
| | | PLS[2:0]=111 (rising edge) | 3.07 | 3.14 | 3.21 | V |
| | | PLS[2:0]=111 (falling edge) | 2.95 | 3.03 | 3.09 | V |
| $V_{PVDhyst}$(1) | PVD hysteresis | - | - | 100 | - | mV |
| $V_{POR/PDR}$ | Power-on/power-down reset threshold | Falling edge | 1.60 | 1.68 | 1.76 | V |
| | | Rising edge | 1.64 | 1.72 | 1.80 | V |
| $V_{PDRhyst}$(1) | PDR hysteresis | - | - | 40 | - | mV |
| $V_{BOR1}$ | Brownout level 1 threshold | Falling edge | 2.13 | 2.19 | 2.24 | V |
| | | Rising edge | 2.23 | 2.29 | 2.33 | V |

**Figure 26. Typical current consumption versus temperature, Run mode, code with data processing running from Flash (ART accelerator OFF) or RAM, and peripherals OFF**

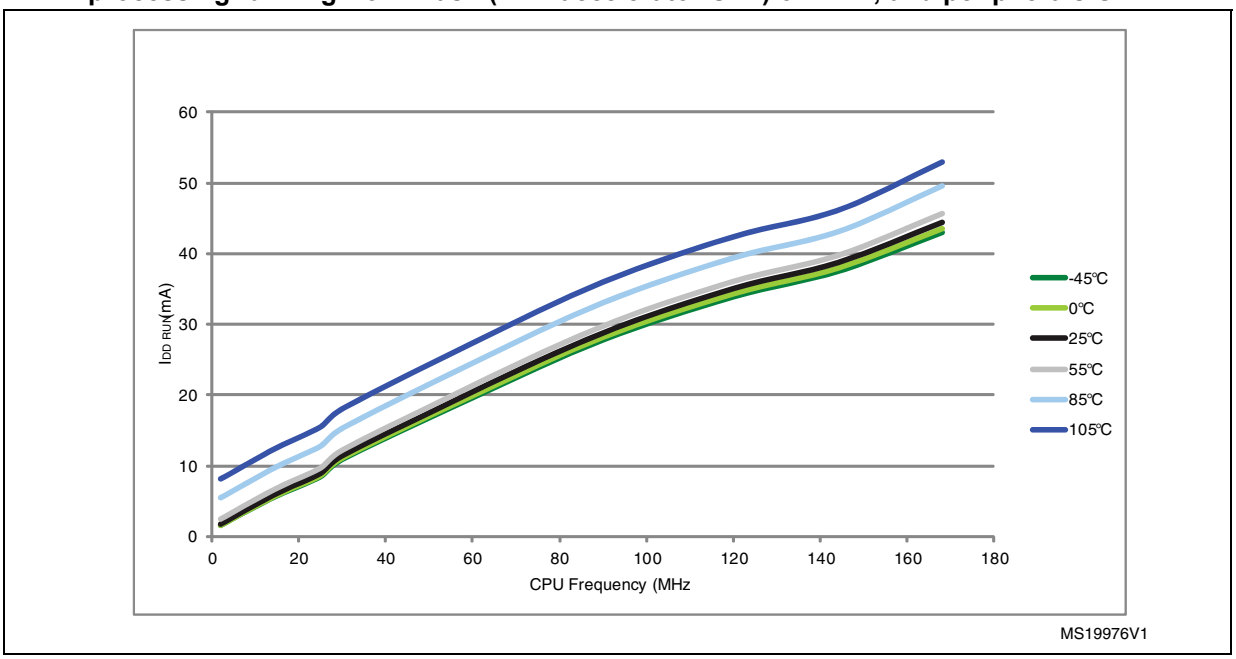



**Figure 27. Typical current consumption versus temperature, Run mode, code with data processing running from Flash (ART accelerator OFF) or RAM, and peripherals ON**

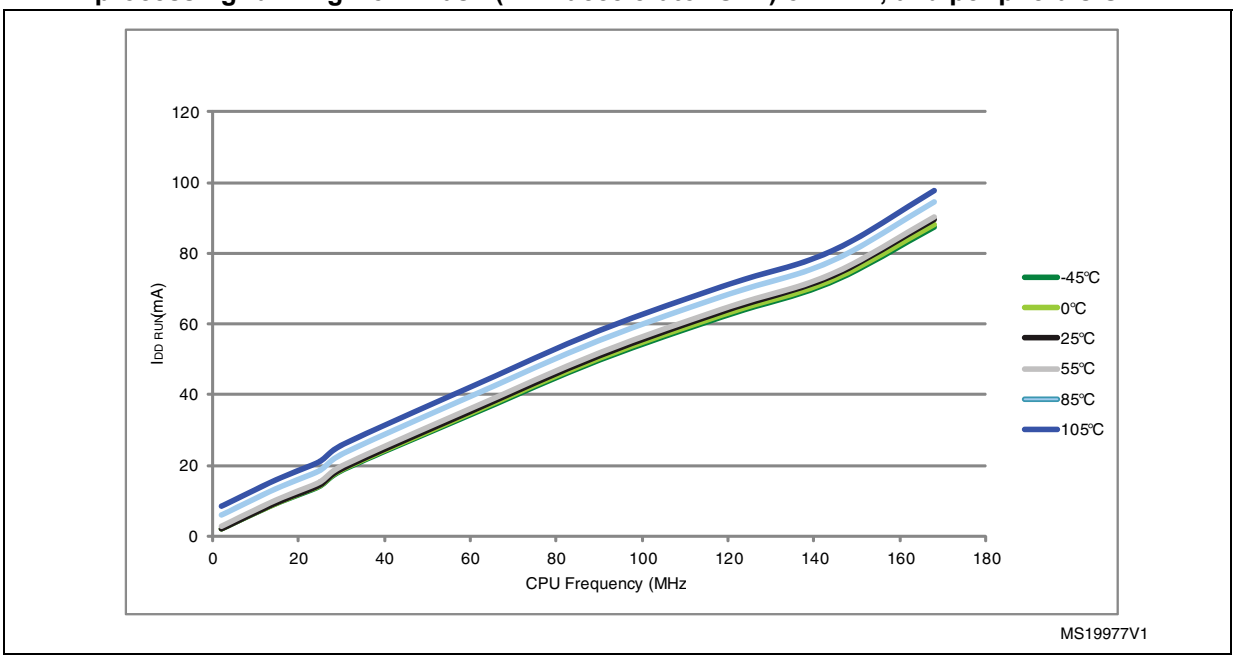
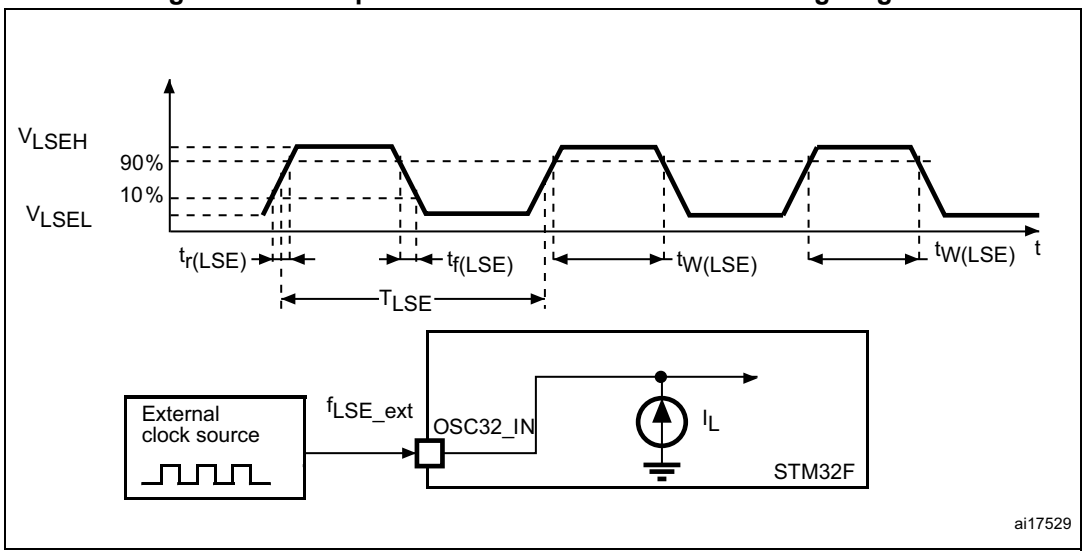


**Table 28. Peripheral current consumption (continued)**

| Peripheral | | $I_{DD}$(Typ)(1) | | Unit |
|---|---|---|---|---|
| | | Scale1 (up t 168 MHz) | Scale2 (up to 144 MHz) | |
| AHB2 (up to 168 MHz) | OTG_FS | 26.45 | 26.67 | µA/MHz |
| | DCMI | 5.87 | 5.35 | |
| | RNG | 1.50 | 1.67 | |
| AHB3 (up to 168 MHz) | FSMC | 12.46 | 11.31 | µA/MHz |
| Bus matrix(2) | | 13.10 | 11.81 | µA/MHz |
| APB1 (up to 42 MHz) | TIM2 | 16.71 | 16.50 | µA/MHz |
| | TIM3 | 12.33 | 11.94 | |
| | TIM4 | 13.45 | 12.92 | |
| | TIM5 | 17.14 | 16.58 | |
| | TIM6 | 2.43 | 3.06 | |
| | TIM7 | 2.43 | 2.22 | |
| | TIM12 | 6.62 | 6.83 | |
| | TIM13 | 5.05 | 5.47 | |
| | TIM14 | 5.26 | 5.61 | |
| | PWR | 1.00 | 0.56 | |
| | USART2 | 2.69 | 2.78 | |
| | USART3 | 2.74 | 2.78 | |
| | UART4 | 3.24 | 3.33 | |
| | UART5 | 2.69 | 2.78 | |
| | I2C1 | 2.67 | 2.50 | |
| | I2C2 | 2.83 | 2.78 | |
| | I2C3 | 2.81 | 2.78 | |
| | SPI2 | 2.43 | 2.22 | |
| | SPI3 | 2.43 | 2.22 | |
| | I2S2(3) | 2.43 | 2.22 | |
| | I2S3(3) | 2.26 | 2.22 | |
| | CAN1 | 5.12 | 5.56 | |
| | CAN2 | 4.81 | 5.28 | |
| | DAC(4) | 1.67 | 1.67 | |
| | WWDG | 1.00 | 0.83 | |

**Figure 31. Low-speed external clock source AC timing diagram**




## High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 26 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 32*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

**Table 32. HSE 4-26 MHz oscillator characteristics (1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{OSC\_IN}$ | Oscillator frequency | - | 4 | - | 26 | MHz |
| $R_F$ | Feedback resistor | - | - | 200 | - | kΩ |
| $G_m$ | Oscillator transconductance | Startup | 5 | - | - | mA/V |
| $G_{mcritmax}$ | Maximum critical crystal $G_m$ | | - | - | 1 | |
| $t_{SU(HSE)}$ (2) | Startup time | $V_{DD}$ is stabilized | - | 2 | - | ms |

1. Guaranteed by design.
2. Guaranteed by characterization. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and can vary significantly with the crystal manufacturer

For $C_{L1}$ and $C_{L2}$, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 32*). $C_{L1}$ and $C_{L2}$ are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of $C_{L1}$ and $C_{L2}$. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing $C_{L1}$ and $C_{L2}$.

### Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 37* and *Table 50*, respectively.

Unless otherwise specified, the parameters given in *Table 50* are derived from tests performed under the ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 14*.

**Table 50. I/O AC characteristics(1)(2)**

| OSPEEDRy [1:0] bit value(1) | Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| 00 | $f_{max(IO)out}$ | Maximum frequency(3) | $C_L$ = 50 pF, $V_{DD}$ > 2.70 V | - | - | 4 | MHz |
| | | | $C_L$ = 50 pF, $V_{DD}$ > 1.8 V | - | - | 2 | |
| | | | $C_L$ = 10 pF, $V_{DD}$ > 2.70 V | - | - | 8 | |
| | | | $C_L$ = 10 pF, $V_{DD}$ > 1.8 V | - | - | 4 | |
| | $t_{f(IO)out}$/ $t_{r(IO)out}$ | Output high to low level fall time and output low to high level rise time | $C_L$ = 50 pF, $V_{DD}$ = 1.8 V to 3.6 V | - | - | 100 | ns |
| 01 | $f_{max(IO)out}$ | Maximum frequency(3) | $C_L$ = 50 pF, $V_{DD}$ > 2.70 V | - | - | 25 | MHz |
| | | | $C_L$ = 50 pF, $V_{DD}$ > 1.8 V | - | - | 12.5 | |
| | | | $C_L$ = 10 pF, $V_{DD}$ > 2.70 V | - | - | 50(4) | |
| | | | $C_L$ = 10 pF, $V_{DD}$ > 1.8 V | - | - | 20 | |
| | $t_{f(IO)out}$/ $t_{r(IO)out}$ | Output high to low level fall time and output low to high level rise time | $C_L$ = 50 pF, $V_{DD}$ >2.7 V | - | - | 10 | ns |
| | | | $C_L$ = 50 pF, $V_{DD}$ > 1.8 V | - | - | 20 | |
| | | | $C_L$ = 10 pF, $V_{DD}$ > 2.70 V | - | - | 6 | |
| | | | $C_L$ = 10 pF, $V_{DD}$ > 1.8 V | - | - | 10 | |
| 10 | $f_{max(IO)out}$ | Maximum frequency(3) | $C_L$ = 40 pF, $V_{DD}$ > 2.70 V | - | - | 50(4) | MHz |
| | | | $C_L$ = 40 pF, $V_{DD}$ > 1.8 V | - | - | 25 | |
| | | | $C_L$ = 10 pF, $V_{DD}$ > 2.70 V | - | - | 100(4) | |
| | | | $C_L$ = 10 pF, $V_{DD}$ > 1.8 V | - | - | 50(4) | |
| | $t_{f(IO)out}$/ $t_{r(IO)out}$ | Output high to low level fall time and output low to high level rise time | $C_L$ = 40 pF, $V_{DD}$ > 2.70 V | - | - | 6 | ns |
| | | | $C_L$ = 40 pF, $V_{DD}$ > 1.8 V | - | - | 10 | |
| | | | $C_L$ = 10 pF, $V_{DD}$ > 2.70 V | - | - | 4 | |
| | | | $C_L$ = 10 pF, $V_{DD}$ > 1.8 V | - | - | 6 | |

**Figure 39. SPI timing diagram - slave mode and CPHA = 0**

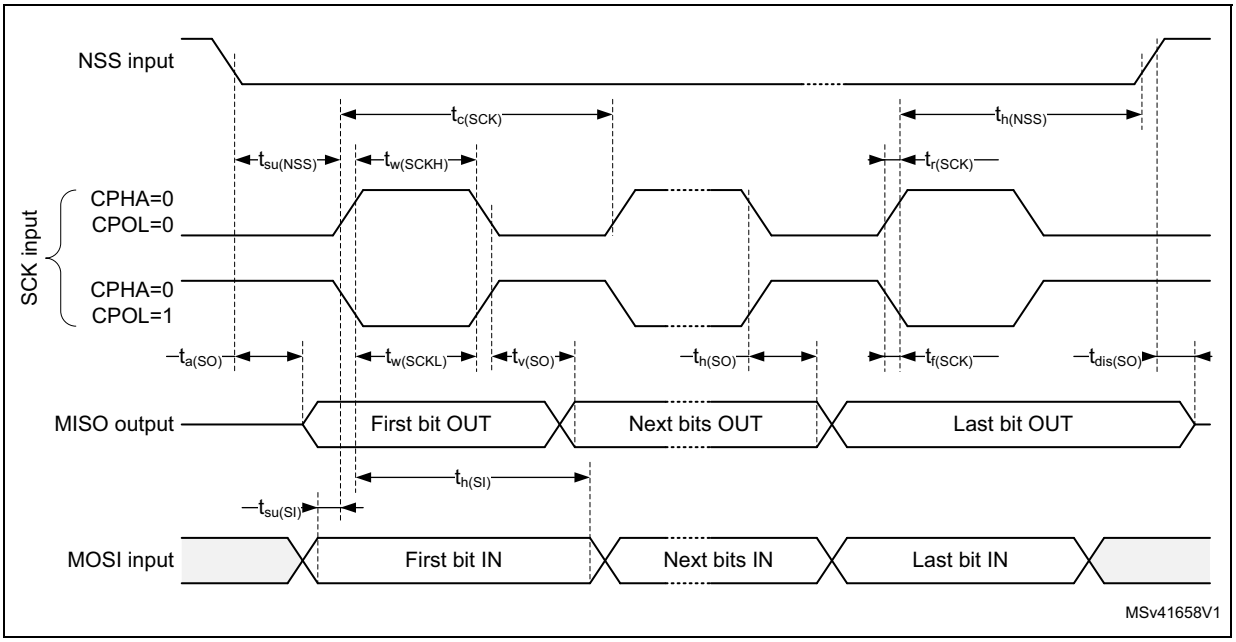



**Figure 40. SPI timing diagram - slave mode and CPHA = 1**

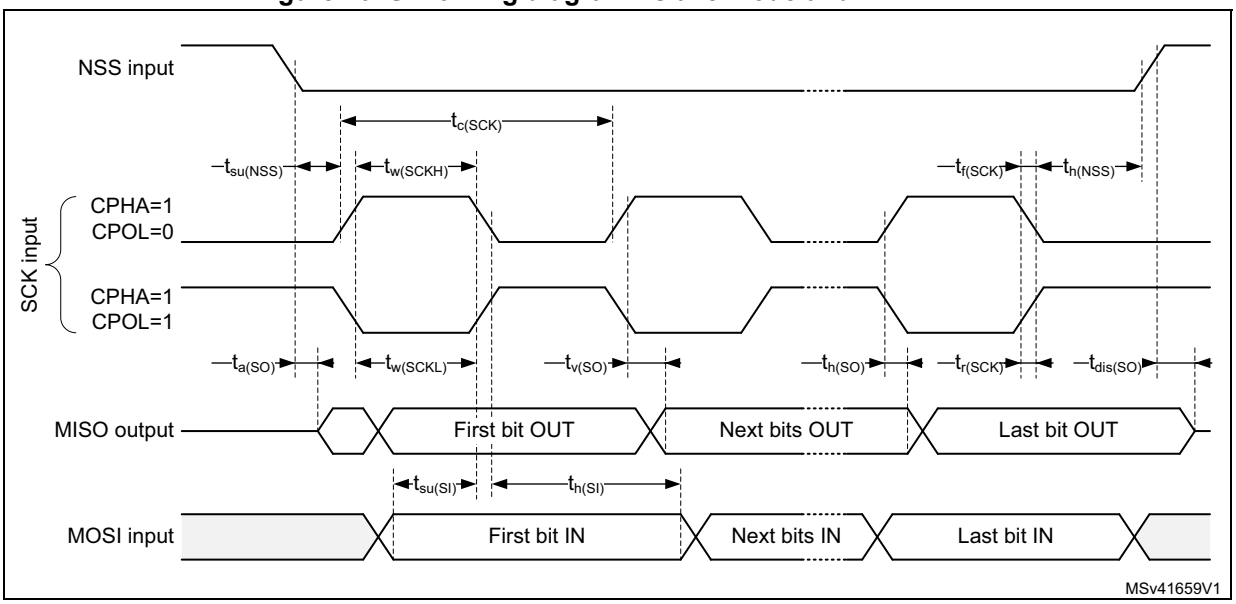


**Figure 57. Asynchronous multiplexed PSRAM/NOR write waveforms**

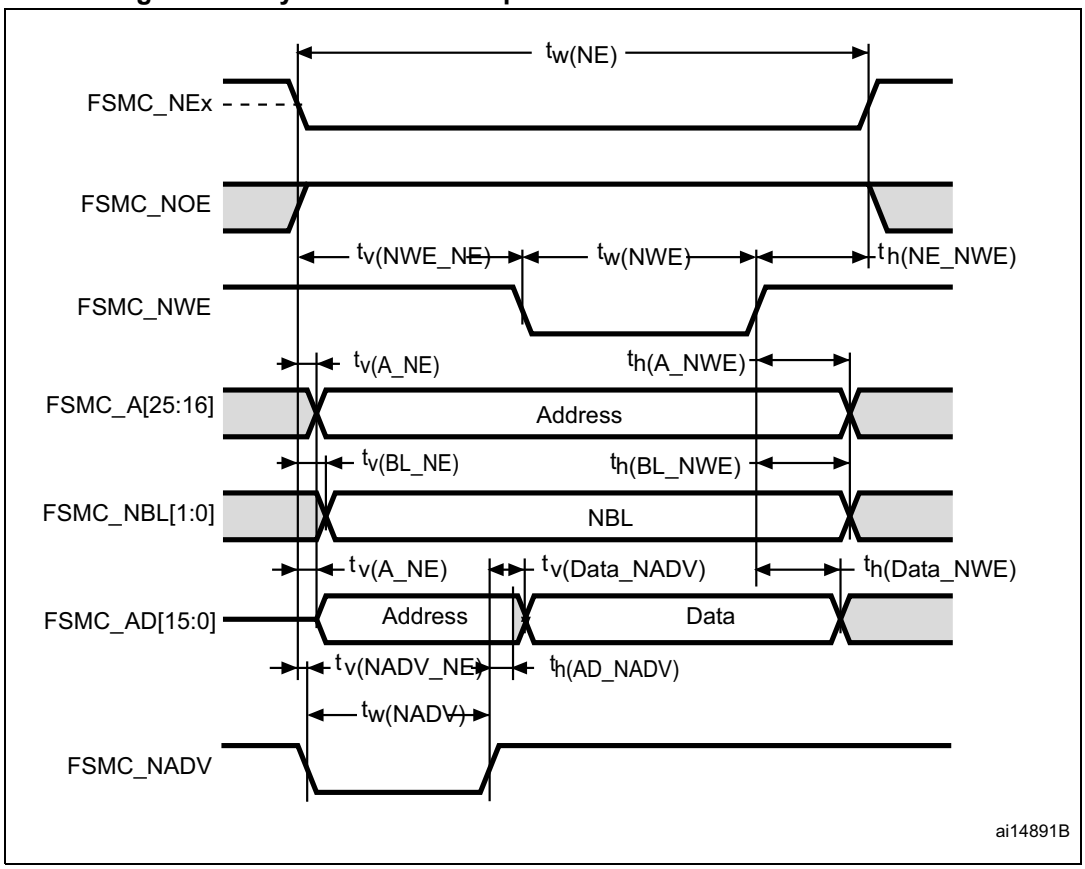



**Table 78. Asynchronous multiplexed PSRAM/NOR write timings(1)(2)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FSMC_NE low time | $4T_{HCLK}$–0.5 | $4T_{HCLK}$+3 | ns |
| $t_{v(NWE\_NE)}$ | FSMC_NEx low to FSMC_NWE low | $T_{HCLK}$–0.5 | $T_{HCLK}$ -0.5 | ns |
| $t_{w(NWE)}$ | FSMC_NWE low tim e | $2T_{HCLK}$–0.5 | $2T_{HCLK}$+3 | ns |
| $t_{h(NE\_NWE)}$ | FSMC_NWE high to FSMC_NE high hold time | $T_{HCLK}$ | - | ns |
| $t_{v(A\_NE)}$ | FSMC_NEx low to FSMC_A valid | - | 0 | ns |
| $t_{v(NADV\_NE)}$ | FSMC_NEx low to FSMC_NADV low | 1 | 2 | ns |
| $t_{w(NADV)}$ | FSMC_NADV low time | $T_{HCLK}$– 2 | $T_{HCLK}$+ 1 | ns |
| $t_{h(AD\_NADV)}$ | FSMC_AD(address) valid hold time after FSMC_NADV high) | $T_{HCLK}$–2 | - | ns |
| $t_{h(A\_NWE)}$ | Address hold time after FSMC_NWE high | $T_{HCLK}$ | - | ns |
| $t_{h(BL\_NWE)}$ | FSMC_BL hold time after FSMC_NWE high | $T_{HCLK}$–2 | - | ns |
| $t_{v(BL\_NE)}$ | FSMC_NEx low to FSMC_BL valid | - | 1.5 | ns |
| $t_{v(Data\_NADV)}$ | FSMC_NADV high to Data valid | - | $T_{HCLK}$–0.5 | ns |
| $t_{h(Data\_NWE)}$ | Data hold time after FSMC_NWE high | $T_{HCLK}$ | - | ns |

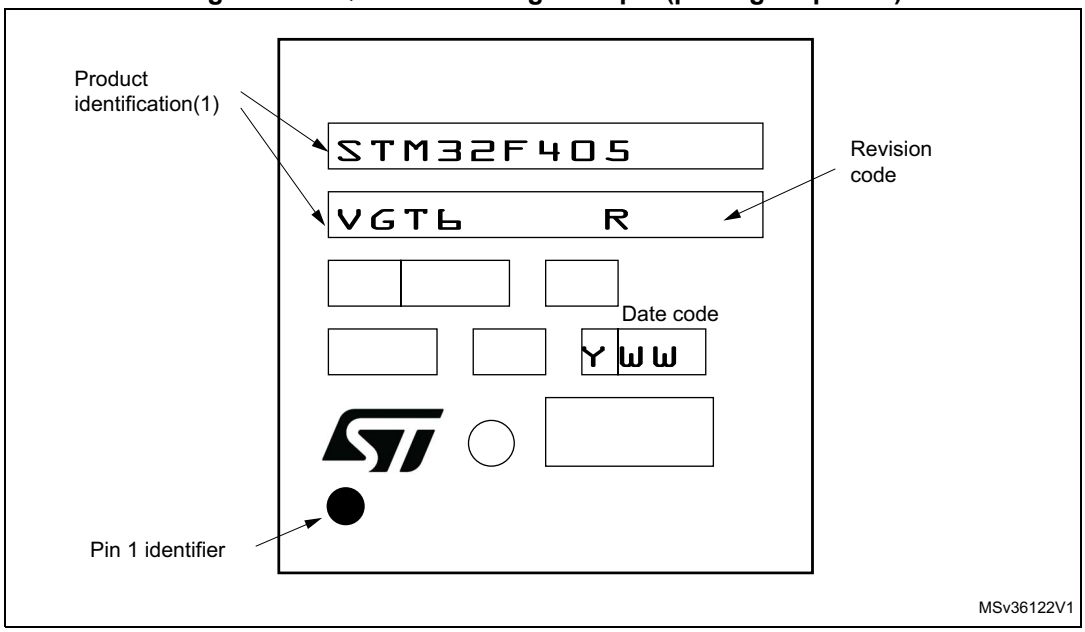
1. $C_L$ = 30 pF.

### Device marking for LFP100

The following figure gives an example of topside marking and pin 1 position identifier location.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

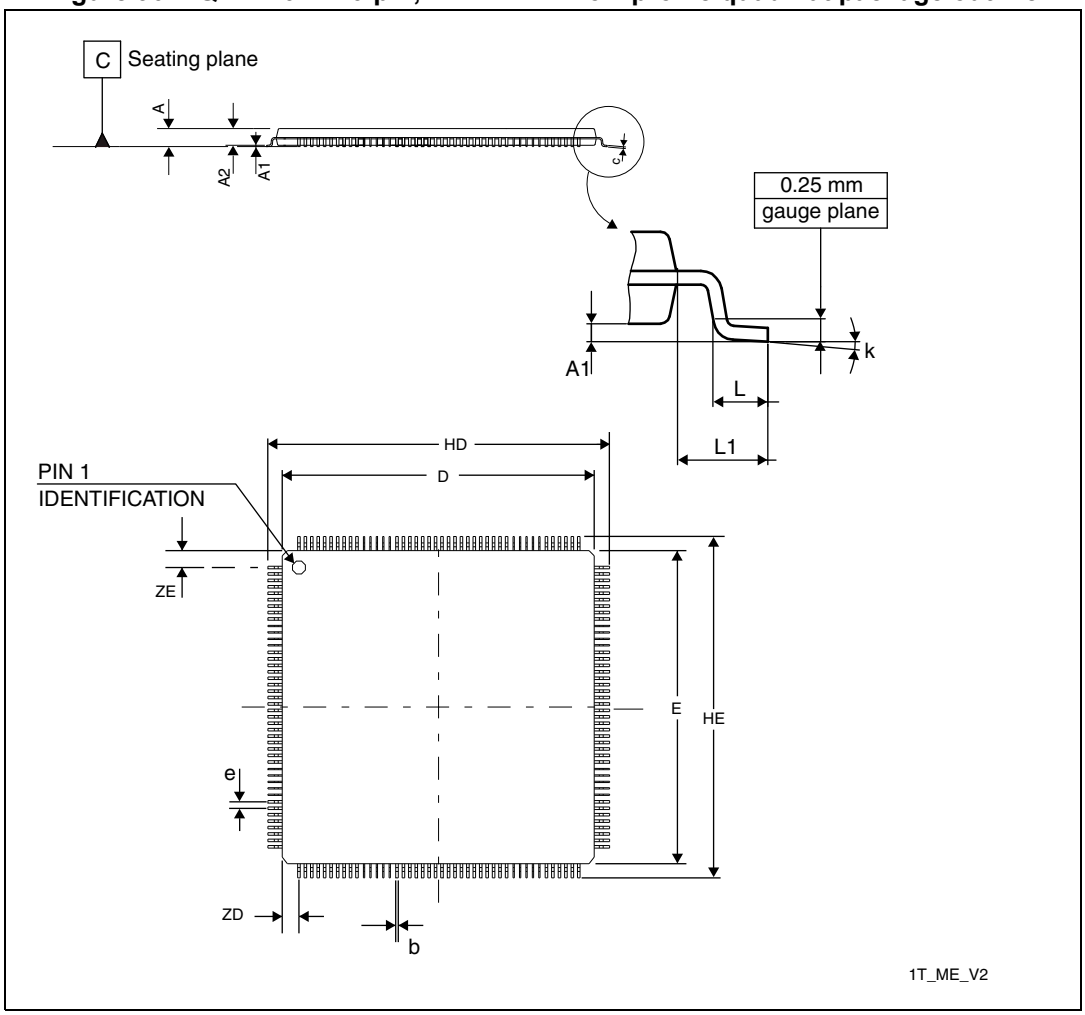
**Figure 83. LQFP100 marking example (package top view)**




1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

## 6.6 LQFP176 package information

**Figure 90. LQFP176 - 176-pin, 24 x 24 mm low profile quad flat package outline**

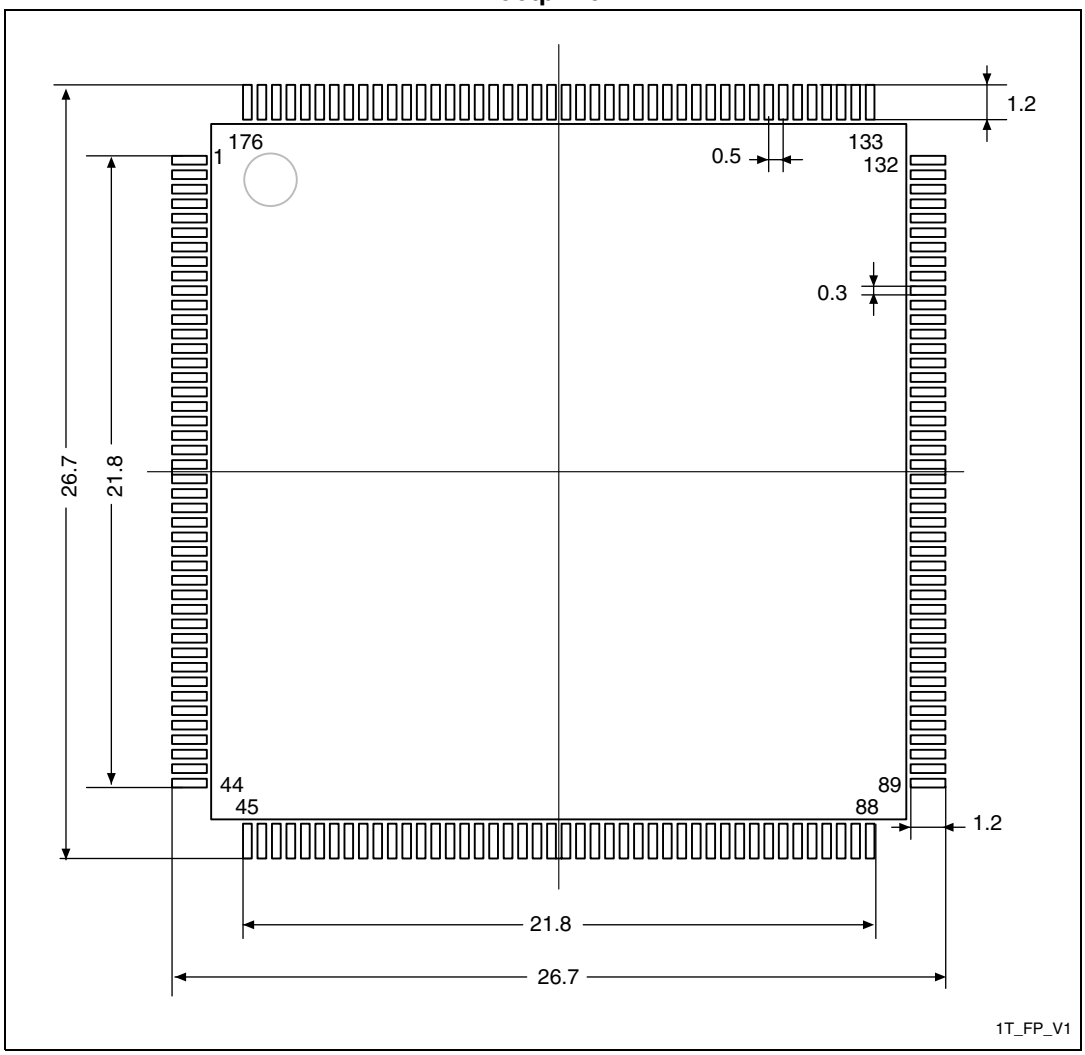



1. Drawing is not to scale.

**Table 97. LQFP176 - 176-pin, 24 x 24 mm low profile quad flat package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | - | 1.450 | 0.0531 | - | 0.0571 |
| b | 0.170 | - | 0.270 | 0.0067 | - | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | 23.900 | - | 24.100 | 0.9409 | - | 0.9488 |
| HD | 25.900 | - | 26.100 | 1.0197 | - | 1.0276 |

**Figure 91. LQFP176 - 176-pin, 24 x 24 mm low profile quad flat recommended footprint**




1. Dimensions are expressed in millimeters.