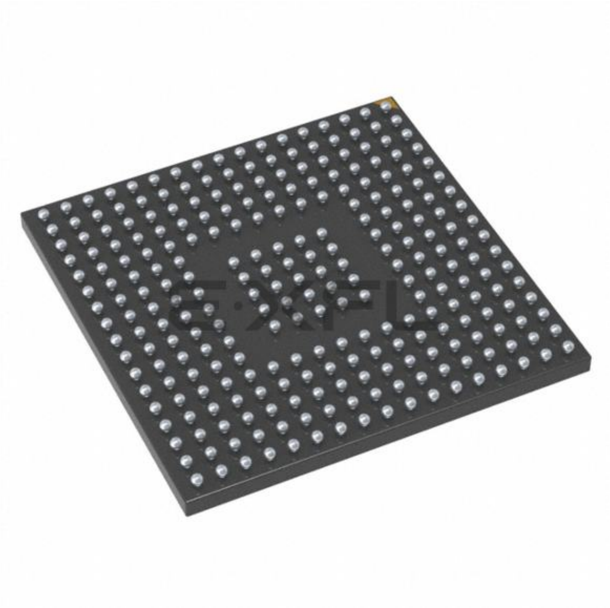

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	168MHz
Connectivity	CANbus, DCMI, EBI/EMI, Ethernet, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	140
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	201-UFBGA
Supplier Device Package	176+25UFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f407igh6tr

Contents

2.2.1 ARM® Cortex®-M4 core with FPU and embedded Flash and SRAM

The ARM Cortex-M4 processor with FPU is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM Cortex-M4 32-bit RISC processor with FPU features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU (floating point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

The STM32F405xx and STM32F407xx family is compatible with all ARM tools and software.

Figure 5 shows the general block diagram of the STM32F40xxx family.

Note: Cortex-M4 with FPU is binary compatible with Cortex-M3.

2.2.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard ARM® Cortex®-M4 with FPU processors. It balances the inherent performance advantage of the ARM Cortex-M4 with FPU over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor full 210 DMIPS performance at this frequency, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 128-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 168 MHz.

2.2.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

2.2.4 Embedded Flash memory

The STM32F40xxx devices embed a Flash memory of 512 Kbytes or 1 Mbytes available for storing programs and data.

2.2.5 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a software signature during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

2.2.6 Embedded SRAM

All STM32F40xxx products embed:

- Up to 192 Kbytes of system SRAM including 64 Kbytes of CCM (core coupled memory) data RAM

  RAM memory is accessed (read/write) at CPU clock speed with 0 wait states.
- 4 Kbytes of backup SRAM

  This area is accessible only from the CPU. Its content is protected against possible unwanted write accesses, and is retained in Standby or V_{BAT} mode.

2.2.7 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs, Ethernet, USB HS) and the slaves (Flash memory, RAM, FSMC, AHB and APB peripherals) and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

Eight DAC trigger inputs are used in the device. The DAC channels are triggered through the timer update outputs that are also connected to different DMA streams.

2.2.38 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using 2 pins only instead of 5 required by the JTAG (JTAG pins could be re-use as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

2.2.39 Embedded Trace Macrocell™

The ARM Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F40xxx through a small number of ETM pins to an external hardware trace port analyser (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell operates with third party debugger software tools.

Table 7. STM32F40xxx pin and ball definitions (continued)

Pin number						Pin name (function after reset)(1)	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP64	WLCSP90	LQFP100	LQFP144	UFBGA176	LQFP176						
-	-	-	49	R6	59	PF11	I/O	FT	-	DCMI_D12/ EVENTOUT	-
-	-	-	50	P6	60	PF12	I/O	FT	-	FSMC_A6/ EVENTOUT	-
-	-	-	51	M8	61	V_{SS}	S	-	-	-	-
-	-	-	52	N8	62	V_{DD}	S	-	-	-	-
-	-	-	53	N6	63	PF13	I/O	FT	-	FSMC_A7/ EVENTOUT	-
-	-	-	54	R7	64	PF14	I/O	FT	-	FSMC_A8/ EVENTOUT	-
-	-	-	55	P7	65	PF15	I/O	FT	-	FSMC_A9/ EVENTOUT	-
-	-	-	56	N7	66	PG0	I/O	FT	-	FSMC_A10/ EVENTOUT	-
-	-	-	57	M7	67	PG1	I/O	FT	-	FSMC_A11/ EVENTOUT	-
-	G6	38	58	R8	68	PE7	I/O	FT	-	FSMC_D4/TIM1_ETR/ EVENTOUT	-
-	H6	39	59	P8	69	PE8	I/O	FT	-	FSMC_D5/ TIM1_CH1N/ EVENTOUT	-
-	J6	40	60	P9	70	PE9	I/O	FT	-	FSMC_D6/TIM1_CH1/ EVENTOUT	-
-	-	-	61	M9	71	V_{SS}	S	-	-	-	-
-	-	-	62	N9	72	V_{DD}	S	-	-	-	-
-	F6	41	63	R9	73	PE10	I/O	FT	-	FSMC_D7/TIM1_CH2N/ EVENTOUT	-
-	J5	42	64	P10	74	PE11	I/O	FT	-	FSMC_D8/TIM1_CH2/ EVENTOUT	-
-	H5	43	65	R10	75	PE12	I/O	FT	-	FSMC_D9/TIM1_CH3N/ EVENTOUT	-
-	G5	44	66	N11	76	PE13	I/O	FT	-	FSMC_D10/TIM1_CH3/ EVENTOUT	-
-	F5	45	67	P11	77	PE14	I/O	FT	-	FSMC_D11/TIM1_CH4/ EVENTOUT	-
-	G4	46	68	R11	78	PE15	I/O	FT	-	FSMC_D12/TIM1_BKIN/ EVENTOUT	-

Table 7. STM32F40xxx pin and ball definitions (continued)

Pin number						Pin name (function after reset)[1]	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP64	WLCSP90	LQFP100	LQFP144	UFBGA176	LQFP176						
55	B6	89	133	A10	161	PB3 (JTDO/ TRACESWO)	I/O	FT	-	JTDO/ TRACESWO/ SPI3_SCK / I2S3_CK / TIM2_CH2 / SPI1_SCK/ EVENTOUT	-
56	A6	90	134	A9	162	PB4 (NJTRST)	I/O	FT	-	NJTRST/ SPI3_MISO / TIM3_CH1 / SPI1_MISO / I2S3ext_SD/ EVENTOUT	-
57	D7	91	135	A6	163	PB5	I/O	FT	-	I2C1_SMBA/ CAN2_RX / OTG_HS_ULPI_D7 / ETH_PPS_OUT/TIM3_CH2 / SPI1_MOSI/ SPI3_MOSI / DCMI_D10 / I2S3_SD/ EVENTOUT	-
58	C7	92	136	B6	164	PB6	I/O	FT	-	I2C1_SCL/ TIM4_CH1 / CAN2_TX / DCMI_D5/USART1_TX/ EVENTOUT	-
59	B7	93	137	B5	165	PB7	I/O	FT	-	I2C1_SDA / FSMC_NL / DCMI_VSYNC / USART1_RX/ TIM4_CH2/ EVENTOUT	-
60	A7	94	138	D6	166	BOOT0	I	B	-	-	V_{PP}
61	D8	95	139	A5	167	PB8	I/O	FT	-	TIM4_CH3/SDIO_D4/ TIM10_CH1 / DCMI_D6 / ETH_MII_TXD3 / I2C1_SCL/ CAN1_RX/ EVENTOUT	-
62	C8	96	140	B4	168	PB9	I/O	FT	-	SPI2_NSS/ I2S2_WS / TIM4_CH4/ TIM11_CH1/ SDIO_D5 / DCMI_D7 / I2C1_SDA / CAN1_TX/ EVENTOUT	-
-	-	97	141	A4	169	PE0	I/O	FT	-	TIM4_ETR / FSMC_NBL0 / DCMI_D2/ EVENTOUT	-
-	-	98	142	A3	170	PE1	I/O	FT	-	FSMC_NBL1 / DCMI_D3/ EVENTOUT	-
63	-	99	-	D5	-	V_{SS}	S	-	-	-	-

Table 10. register boundary addresses (continued)

Bus	Boundary address	Peripheral
APB2	0x4001 4C00 - 0x4001 57FF	Reserved
	0x4001 4800 - 0x4001 4BFF	TIM11
	0x4001 4400 - 0x4001 47FF	TIM10
	0x4001 4000 - 0x4001 43FF	TIM9
	0x4001 3C00 - 0x4001 3FFF	EXTI
	0x4001 3800 - 0x4001 3BFF	SYSCFG
	0x4001 3400 - 0x4001 37FF	Reserved
	0x4001 3000 - 0x4001 33FF	SPI1
	0x4001 2C00 - 0x4001 2FFF	SDIO
	0x4001 2400 - 0x4001 2BFF	Reserved
	0x4001 2000 - 0x4001 23FF	ADC1 - ADC2 - ADC3
	0x4001 1800 - 0x4001 1FFF	Reserved
	0x4001 1400 - 0x4001 17FF	USART6
	0x4001 1000 - 0x4001 13FF	USART1
	0x4001 0800 - 0x4001 0FFF	Reserved
	0x4001 0400 - 0x4001 07FF	TIM8
	0x4001 0000 - 0x4001 03FF	TIM1
	0x4000 7800- 0x4000 FFFF	Reserved

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V (for the 1.8 V ≤V_{DD} ≤3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 19*.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 20*.

Figure 19. Pin loading conditions

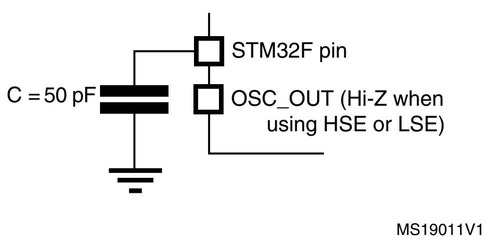
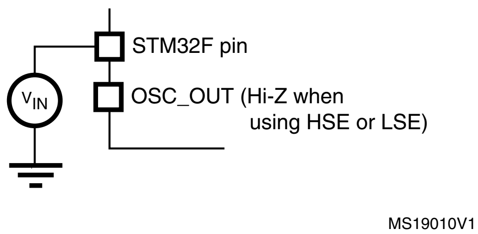
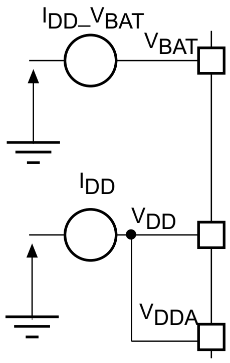


Figure 20. Pin input voltage



5.1.7 Current consumption measurement

Figure 22. Current consumption measurement scheme



5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 11: Voltage characteristics*, *Table 12: Current characteristics*, and *Table 13: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Device mission profile (application conditions) is compliant with JEDEC JESD47 Qualification Standard, extended mission profiles are available on demand.

Table 11. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
$V_{DD}–V_{SS}$	External main supply voltage (including V_{DDA}, V_{DD})(1)	–0.3	4.0	V
V_{IN}	Input voltage on five-volt tolerant pin(2)	V_{SS}–0.3	V_{DD}+4	
	Input voltage on any other pin	V_{SS}–0.3	4.0	
$\|\Delta V_{DDx}\|$	Variations between different V_{DD} power pins	-	50	mV
$\|V_{SSX} - V_{SS}\|$	Variations between all the different ground pins including V_{REF-}	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 5.3.14: Absolute maximum ratings (electrical sensitivity)*		

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum value must always be respected. Refer to *Table 12* for the values of the maximum allowed injected current.

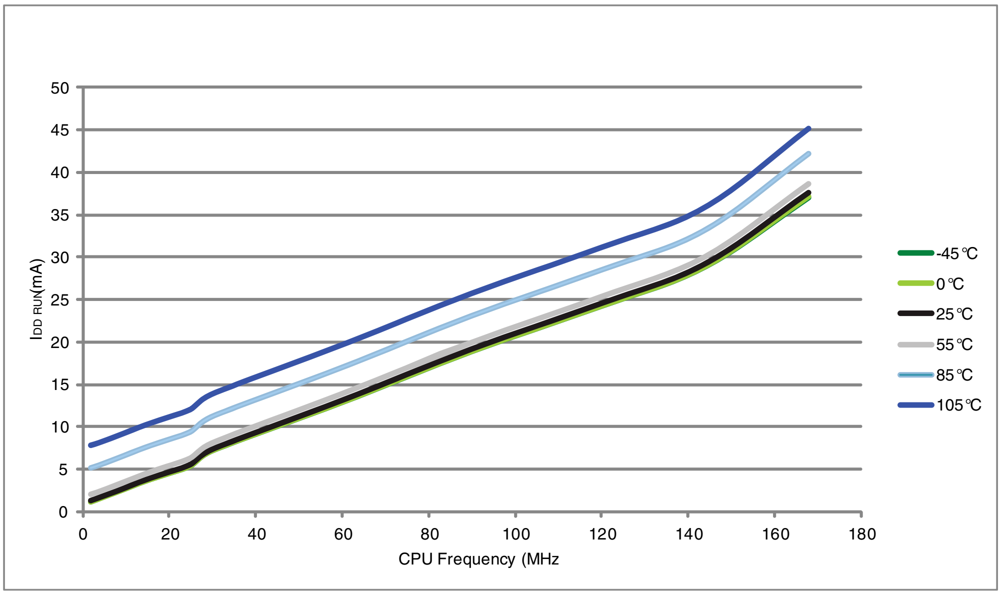
5.3.5 Embedded reset and power control block characteristics

The parameters given in *Table 19* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Table 19. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.09	2.14	2.19	V
		PLS[2:0]=000 (falling edge)	1.98	2.04	2.08	V
		PLS[2:0]=001 (rising edge)	2.23	2.30	2.37	V
		PLS[2:0]=001 (falling edge)	2.13	2.19	2.25	V
		PLS[2:0]=010 (rising edge)	2.39	2.45	2.51	V
		PLS[2:0]=010 (falling edge)	2.29	2.35	2.39	V
		PLS[2:0]=011 (rising edge)	2.54	2.60	2.65	V
		PLS[2:0]=011 (falling edge)	2.44	2.51	2.56	V
		PLS[2:0]=100 (rising edge)	2.70	2.76	2.82	V
		PLS[2:0]=100 (falling edge)	2.59	2.66	2.71	V
		PLS[2:0]=101 (rising edge)	2.86	2.93	2.99	V
		PLS[2:0]=101 (falling edge)	2.65	2.84	2.92	V
		PLS[2:0]=110 (rising edge)	2.96	3.03	3.10	V
		PLS[2:0]=110 (falling edge)	2.85	2.93	2.99	V
		PLS[2:0]=111 (rising edge)	3.07	3.14	3.21	V
		PLS[2:0]=111 (falling edge)	2.95	3.03	3.09	V
$V_{PVDhyst}$(1)	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power-on/power-down reset threshold	Falling edge	1.60	1.68	1.76	V
		Rising edge	1.64	1.72	1.80	V
$V_{PDRhyst}$(1)	PDR hysteresis	-	-	40	-	mV
V_{BOR1}	Brownout level 1 threshold	Falling edge	2.13	2.19	2.24	V
		Rising edge	2.23	2.29	2.33	V

Figure 24. Typical current consumption versus temperature, Run mode, code with data processing running from Flash (ART accelerator ON) or RAM, and peripherals OFF



MS19974V1

Figure 25. Typical current consumption versus temperature, Run mode, code with data processing running from Flash (ART accelerator ON) or RAM, and peripherals ON

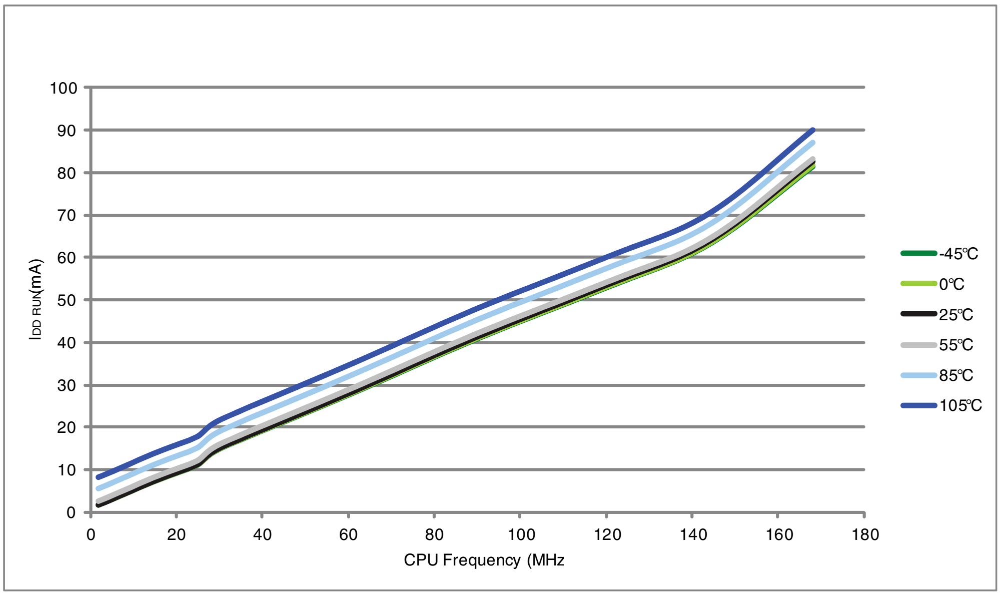


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Table 25. Typical and maximum current consumptions in V_{BAT} mode

Symbol	Parameter	Conditions	Typ			Max(1)		Unit
			T_A = 25 °C			T_A = 85 °C	T_A = 105 °C	
			V_{BAT} = 1.8 V	V_{BAT}= 2.4 V	V_{BAT} = 3.3 V	V_{BAT} = 3.6 V		
I_{DD_VBAT}	Backup domain supply current	Backup SRAM ON, low-speed oscillator and RTC ON	1.29	1.42	1.68	6	11	µA
		Backup SRAM OFF, low-speed oscillator and RTC ON	0.62	0.73	0.96	3	5	
		Backup SRAM ON, RTC OFF	0.79	0.81	0.86	5	10	
		Backup SRAM OFF, RTC OFF	0.10	0.10	0.10	2	4	

1. Guaranteed by characterization.

Figure 28. Typical V_{BAT} current consumption (LSE and RTC ON/backup RAM OFF)

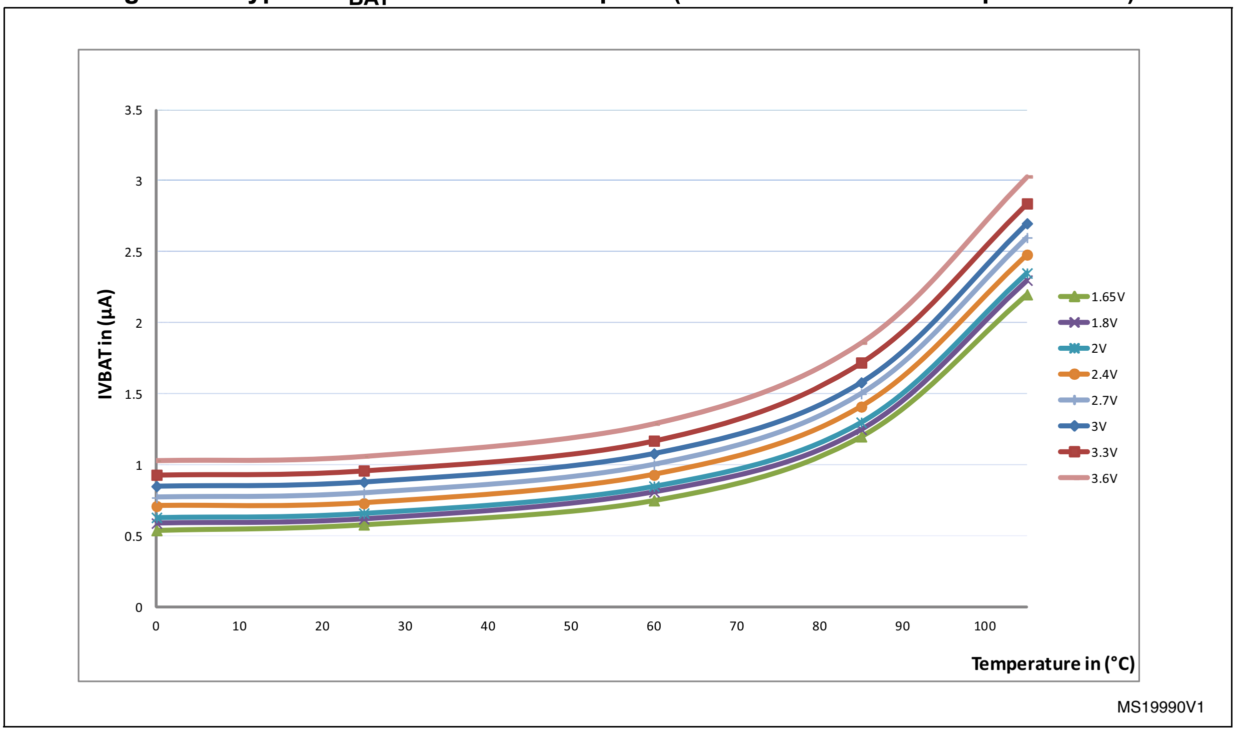


Table 28. Peripheral current consumption (continued)

Peripheral		I_{DD}(Typ)[1]		Unit
		Scale1 (up t 168 MHz)	Scale2 (up to 144 MHz)	
AHB2 (up to 168 MHz)	OTG_FS	26.45	26.67	µA/MHz
	DCMI	5.87	5.35	
	RNG	1.50	1.67	
AHB3 (up to 168 MHz)	FSMC	12.46	11.31	µA/MHz
Bus matrix[2]		13.10	11.81	µA/MHz
APB1 (up to 42 MHz)	TIM2	16.71	16.50	µA/MHz
	TIM3	12.33	11.94	
	TIM4	13.45	12.92	
	TIM5	17.14	16.58	
	TIM6	2.43	3.06	
	TIM7	2.43	2.22	
	TIM12	6.62	6.83	
	TIM13	5.05	5.47	
	TIM14	5.26	5.61	
	PWR	1.00	0.56	
	USART2	2.69	2.78	
	USART3	2.74	2.78	
	UART4	3.24	3.33	
	UART5	2.69	2.78	
	I2C1	2.67	2.50	
	I2C2	2.83	2.78	
	I2C3	2.81	2.78	
	SPI2	2.43	2.22	
	SPI3	2.43	2.22	
	I2S2[3]	2.43	2.22	
	I2S3[3]	2.26	2.22	
	CAN1	5.12	5.56	
	CAN2	4.81	5.28	
	DAC[4]	1.67	1.67	
	WWDG	1.00	0.83	

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application, executing EEMBC? code, is running. This emission test is compliant with SAE IEC61967-2 standard which specifies the test board and the pin loading.

Table 44. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{CPU}] 25/168 MHz	Unit
S_{EMI}	Peak level	V_{DD} = 3.3 V, T_A = 25 °C, LQFP176 package, conforming to SAE J1752/3 EEMBC, code running from Flash with ART accelerator enabled	0.1 to 30 MHz	32	dBµV
			30 to 130 MHz	25	
			130 MHz to 1GHz	29	
			SAE EMI Level	4	-
		V_{DD} = 3.3 V, T_A = 25 °C, LQFP176 package, conforming to SAE J1752/3 EEMBC, code running from Flash with ART accelerator and PLL spread spectrum enabled	0.1 to 30 MHz	19	dBµV
			30 to 130 MHz	16	
			130 MHz to 1GHz	18	
			SAE EMI level	3.5	-

5.3.14 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 45. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to JESD22-A114	2	2000(2)	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to ANSI/ESD STM5.3.1	II	500	

1. Guaranteed by characterization.
2. On V_{BAT} pin, $V_{ESD(HBM)}$ is limited to 1000 V.

Figure 41. SPI timing diagram - master mode

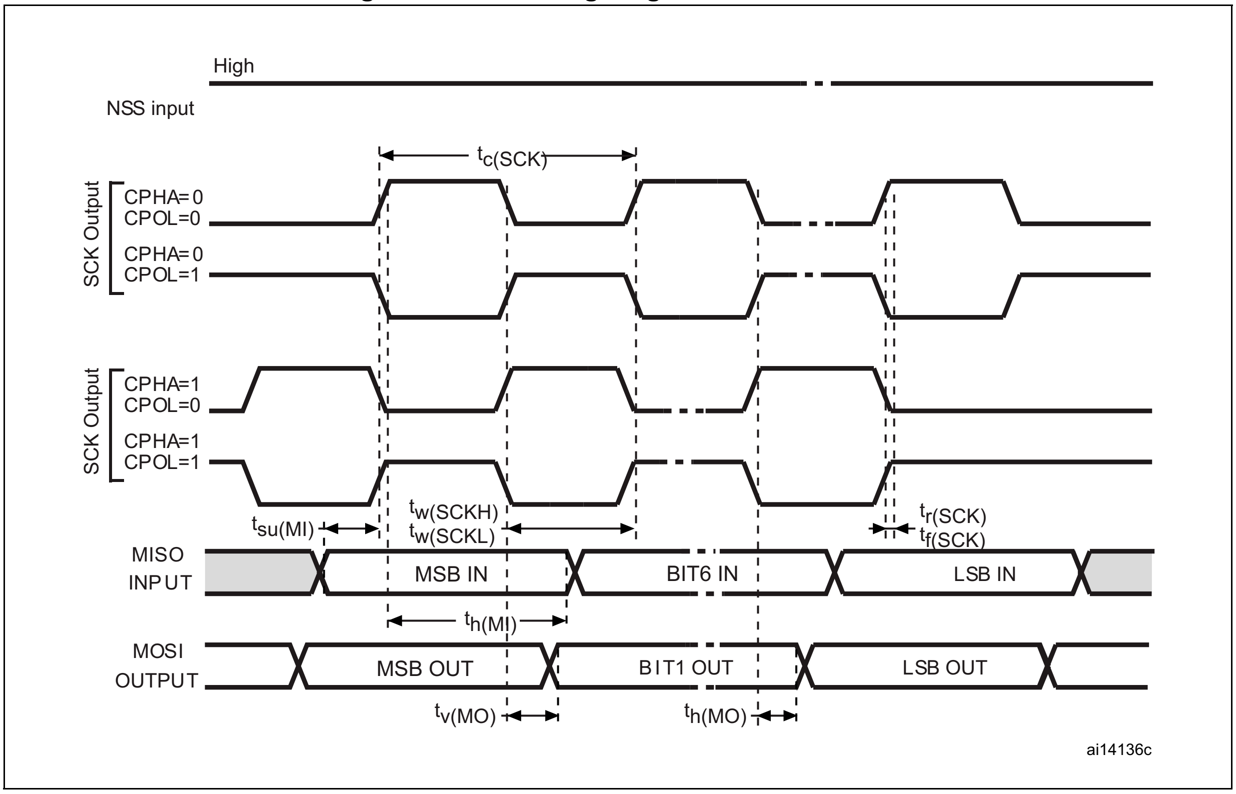
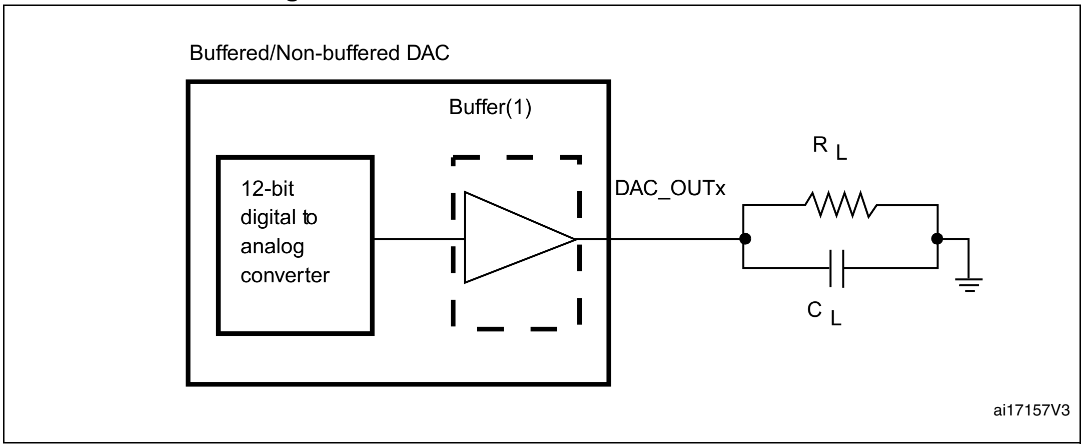


Figure 53. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

5.3.26 FSMC characteristics

Unless otherwise specified, the parameters given in *Table 75* to *Table 86* for the FSMC interface are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage conditions summarized in *Table 14*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to Section *Section 5.3.16: I/O port characteristics* for more details on the input/output characteristics.

Asynchronous waveforms and timings

Figure 54 through *Figure 57* represent asynchronous waveforms and *Table 75* through *Table 78* provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- AddressSetupTime = 1
- AddressHoldTime = 0x1
- DataSetupTime = 0x1
- BusTurnAroundDuration = 0x0

In all timing tables, the T_{HCLK} is the HCLK clock period.

Table 84. Switching characteristics for PC Card/CF read and write cycles in I/O space(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NIOWR)}$	FSMC_NIOWR low width	$8T_{HCLK} -1$	-	ns
$t_{v(NIOWR-D)}$	FSMC_NIOWR low to FSMC_D[15:0] valid	-	$5T_{HCLK}- 1$	ns
$t_{h(NIOWR-D)}$	FSMC_NIOWR high to FSMC_D[15:0] invalid	$8T_{HCLK}- 2$	-	ns
$t_{d(NCE4\_1-NIOWR)}$	FSMC_NCE4_1 low to FSMC_NIOWR valid	-	$5T_{HCLK}+ 2.5$	ns
$t_{h(NCEx-NIOWR)}$	FSMC_NCEx high to FSMC_NIOWR invalid	$5T_{HCLK}-1.5$	-	ns
$t_{d(NIORD-NCEx)}$	FSMC_NCEx low to FSMC_NIORD valid	-	$5T_{HCLK}+ 2$	ns
$t_{h(NCEx-NIORD)}$	FSMC_NCEx high to FSMC_NIORD) valid	$5T_{HCLK}- 1.5$	-	ns
$t_{w(NIORD)}$	FSMC_NIORD low width	$8T_{HCLK}-0.5$	-	ns
$t_{su(D-NIORD)}$	FSMC_D[15:0] valid before FSMC_NIORD high	9	-	ns
$t_{d(NIORD-D)}$	FSMC_D[15:0] valid after FSMC_NIORD high	0	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization.

NAND controller waveforms and timings

Figure 68 through *Figure 71* represent synchronous waveforms, and *Table 85* and *Table 86* provide the corresponding timings. The results shown in this table are obtained with the following FSMC configuration:

- COM.FSMC_SetupTime = 0x01;
- COM.FSMC_WaitSetupTime = 0x03;
- COM.FSMC_HoldSetupTime = 0x02;
- COM.FSMC_HiZSetupTime = 0x01;
- ATT.FSMC_SetupTime = 0x01;
- ATT.FSMC_WaitSetupTime = 0x03;
- ATT.FSMC_HoldSetupTime = 0x02;
- ATT.FSMC_HiZSetupTime = 0x01;
- Bank = FSMC_Bank_NAND;
- MemoryDataWidth = FSMC_MemoryDataWidth_16b;
- ECC = FSMC_ECC_Enable;
- ECCPageSize = FSMC_ECCPageSize_512Bytes;
- TCLRSetupTime = 0;
- TARSetupTime = 0.

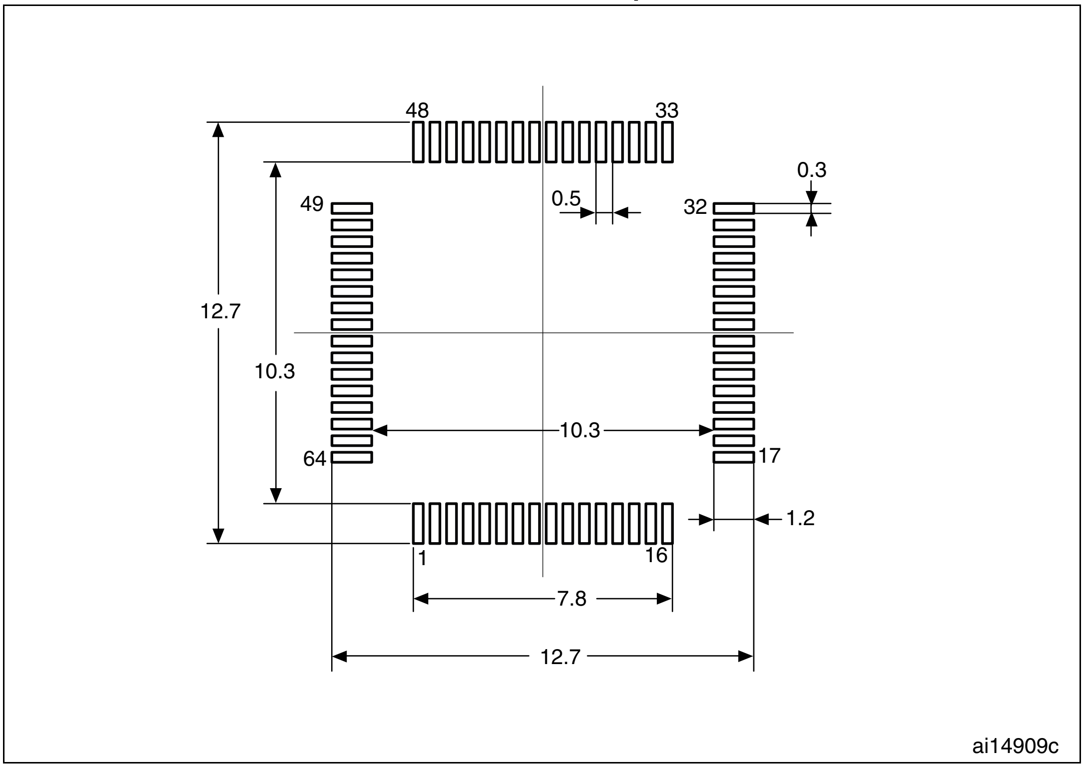
In all timing tables, the T_{HCLK} is the HCLK clock period.

Table 92. LQFP64 – 64-pin 10 x 10 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 79. LQFP64 – 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint



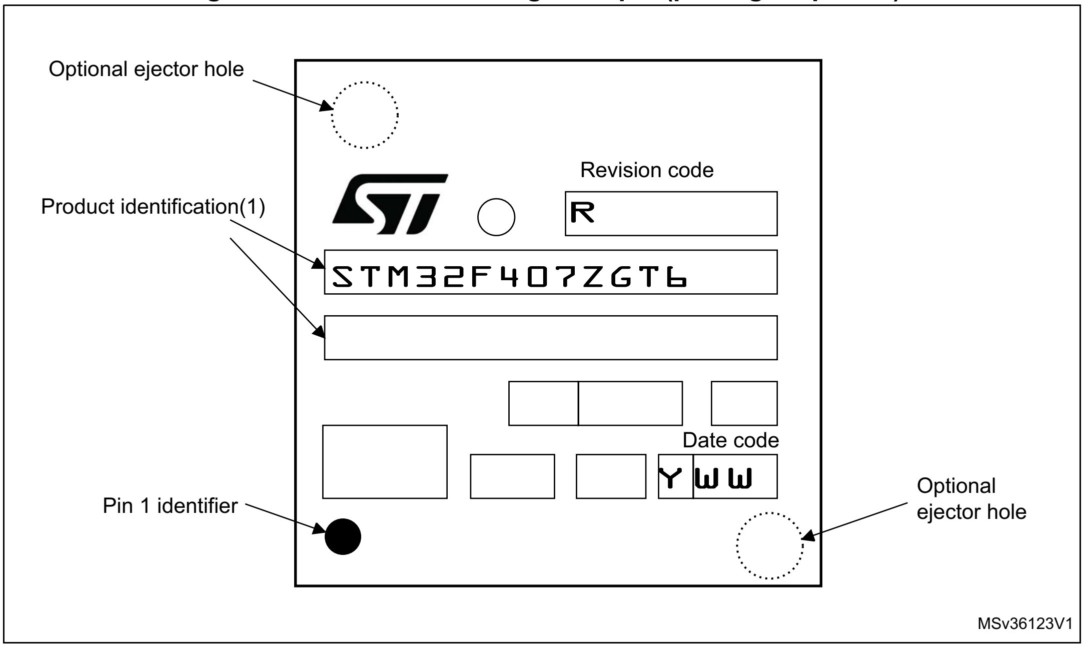
1. Dimensions are in millimeters.

Device marking for LQPF144

The following figure gives an example of topside marking and pin 1 position identifier location.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 86. LQFP144 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Table 100. Document revision history (continued)

Date	Revision	Changes
04-Jun-2013	4	Modified *Note 1* below *Table 2: STM32F405xx and STM32F407xx: features and peripheral counts*. Updated *Figure 4* title. Updated *Note 3* below *Figure 21: Power supply scheme*. Changed simplex mode into half-duplex mode in *Section 2.2.25: Inter-integrated sound (I2S)*. Replaced DAC1_OUT and DAC2_OUT by DAC_OUT1 and DAC_OUT2, respectively. Updated pin 36 signal in *Figure 15: STM32F40xxx LQFP176 pinout*. Changed pin number from F8 to D4 for PA13 pin in *Table 7: STM32F40xxx pin and ball definitions*. Replaced TIM2_CH1/TIM2_ETR by TIM2_CH1_ETR for PA0 and PA5 pins in *Table 9: Alternate function mapping*. Changed system memory into System memory + OTP in *Figure 18: STM32F40xxx memory map*. Added *Note 1* below *Table 16: VCAP_1/VCAP_2 operating conditions*. Updated I_{DDA} description in *Table 74: DAC characteristics*. Removed PA9/PB13 connection to VBUS in *Figure 93: USB controller configured as peripheral-only and used in Full speed mode* and *Figure 94: USB controller configured as host-only and used in full speed mode*. Updated SPI throughput on front page and *Section 2.2.24: Serial peripheral interface (SPI)* Updated operating voltages in *Table 2: STM32F405xx and STM32F407xx: features and peripheral counts* Updated note in *Section 2.2.14: Power supply schemes* Updated *Section 2.2.15: Power supply supervisor* Updated “Regulator ON” paragraph in *Section 2.2.16: Voltage regulator* Removed note in *Section 2.2.19: Low-power modes* Corrected wrong reference manual in *Section 2.2.28: Ethernet MAC interface with dedicated DMA and IEEE 1588 support* Updated *Table 15: Limitations depending on the operating power supply range* Updated *Table 24: Typical and maximum current consumptions in Standby mode* Updated *Table 25: Typical and maximum current consumptions in VBAT mode* Updated *Table 37: PLLI2S (audio PLL) characteristics* Updated *Table 44: EMI characteristics* Updated *Table 49: Output voltage characteristics* Updated *Table 51: NRST pin characteristics* Updated *Table 55: SPI dynamic characteristics* Updated *Table 56: I2S dynamic characteristics* Deleted Table 59 Updated *Table 62: ULPI timing* Updated *Figure 46: Ethernet SMI timing diagram*