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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	168MHz
Connectivity	CANbus, DCMI, EBI/EMI, Ethernet, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f407vet6

2   Description

The STM32F405xx and STM32F407xx family is based on the high-performance ARM®
Cortex®-M4 32-bit RISC core operating at a frequency of up to 168 MHz. The Cortex-M4
core features a Floating point unit (FPU) single precision which supports all ARM single-
precision data-processing instructions and data types. It also implements a full set of DSP
instructions and a memory protection unit (MPU) which enhances application security.

The STM32F405xx and STM32F407xx family incorporates high-speed embedded
memories (Flash memory up to 1 Mbyte, up to 192 Kbytes of SRAM), up to 4 Kbytes of
backup SRAM, and an extensive range of enhanced I/Os and peripherals connected to two
APB buses, three AHB buses and a 32-bit multi-AHB bus matrix.

All devices offer three 12-bit ADCs, two DACs, a low-power RTC, twelve general-purpose
16-bit timers including two PWM timers for motor control, two general-purpose 32-bit timers.
a true random number generator (RNG). They also feature standard and advanced
communication interfaces.

- Up to three I^{2}Cs
- Three SPIs, two I^{2}Ss full duplex. To achieve audio class accuracy, the I2S peripherals
  can be clocked via a dedicated internal audio PLL or via an external clock to allow
  synchronization.
- Four USARTs plus two UARTs
- An USB OTG full-speed and a USB OTG high-speed with full-speed capability (with the
  ULPI),
- Two CANs
- An SDIO/MMC interface
- Ethernet and the camera interface available on STM32F407xx devices only.

New advanced peripherals include an SDIO, an enhanced flexible static memory control
(FSMC) interface (for devices offered in packages of 100 pins and more), a camera
interface for CMOS sensors. Refer to *Table 2: STM32F405xx and STM32F407xx: features
and peripheral counts* for the list of peripherals available on each part number.

The STM32F405xx and STM32F407xx family operates in the –40 to +105 °C temperature
range from a 1.8 to 3.6 V power supply. The supply voltage can drop to 1.7 V when the
device operates in the 0 to 70 °C temperature range using an external power supply
supervisor: refer to *Section : Internal reset OFF*. A comprehensive set of power-saving
mode allows the design of low-power applications.

The STM32F405xx and STM32F407xx family offers devices in various packages ranging
from 64 pins to 176 pins. The set of included peripherals changes with the device chosen.

These features make the STM32F405xx and STM32F407xx microcontroller family suitable
for a wide range of applications:

- Motor drive and application control
- Medical equipment
- Industrial applications: PLC, inverters, circuit breakers
- Printers, and scanners
- Alarm systems, video intercom, and HVAC
- Home audio appliances

Figure 5 shows the general block diagram of the device family.

Table 2. STM32F405xx and STM32F407xx: features and peripheral counts

Peripherals		STM32F405RG	STM32F405OG	STM32F405VG	STM32F405ZG	STM32F405OE	STM32F407Vx		STM32F407Zx		STM32F407Ix	
Flash memory in Kbytes		1024				512	512	1024	512	1024	512	1024
SRAM in Kbytes	System	192(112+16+64)										
	Backup	4										
FSMC memory controller		No	Yes[1]									
Ethernet		No						Yes				
Timers	General-purpose	10										
	Advanced-control	2										
	Basic	2										
	IWDG	Yes										
	WWDG	Yes										
	RTC	Yes										
Random number generator		Yes										

**Figure 4. Compatible board design between STM32F2 and STM32F40xxx
for LQFP176 and BGA176 packages**
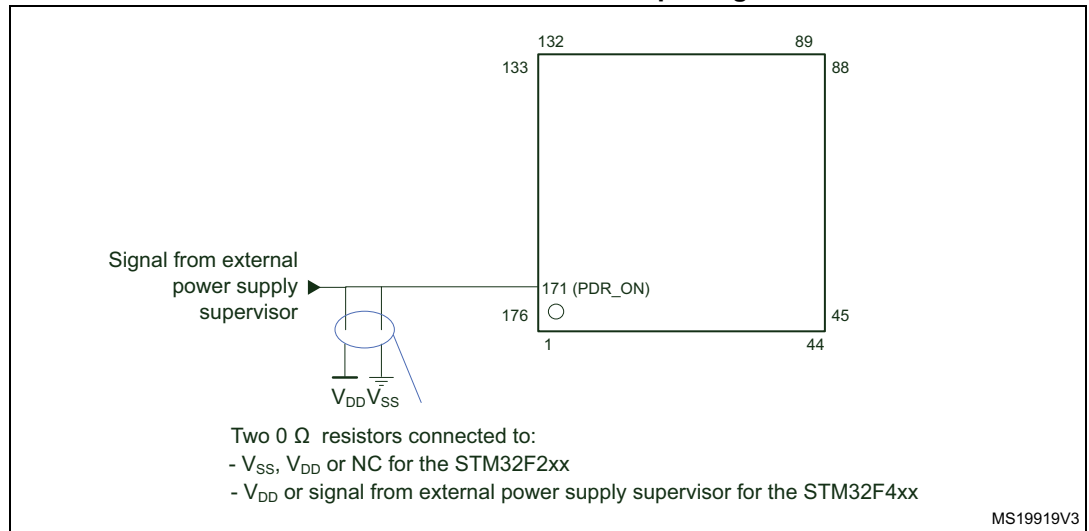
clock entry is available when necessary (for example if an indirectly used external oscillator fails).

Several prescalers allow the configuration of the three AHB buses, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the three AHB buses is 168 MHz while the maximum frequency of the high-speed APB domains is 84 MHz. The maximum allowed frequency of the low-speed APB domain is 42 MHz.

The devices embed a dedicated PLL (PLLI2S) which allows to achieve audio class performance. In this case, the I^{2}S master clock can generate all standard sampling frequencies from 8 kHz to 192 kHz.

2.2.13 Boot modes

At startup, boot pins are used to select one out of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART1 (PA9/PA10), USART3 (PC10/PC11 or PB10/PB11), CAN2 (PB5/PB13), USB OTG FS in Device mode (PA11/PA12) through DFU (device firmware upgrade).

2.2.14 Power supply schemes

- V_{DD} = 1.8 to 3.6 V: external power supply for I/Os and the internal regulator (when enabled), provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 1.8 to 3.6 V: external analog power supplies for ADC, DAC, Reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

Refer to *Figure 21: Power supply scheme* for more details.

Note: *V_{DD}/V_{DDA} minimum value of 1.7 V is obtained when the device operates in reduced temperature range, and with the use of an external power supply supervisor (refer to Section : Internal reset OFF).*

Refer to Table 2 in order to identify the packages supporting this option.

2.2.15 Power supply supervisor

Internal reset ON

On packages embedding the PDR_ON pin, the power supply supervisor is enabled by holding PDR_ON high. On all other packages, the power supply supervisor is always enabled.

The device has an integrated power-on reset (POR) / power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry. At power-on, POR/PDR is always active and ensures proper operation starting from 1.8 V. After the 1.8 V POR threshold level is reached, the option byte loading process starts, either to confirm or modify default BOR threshold levels, or to disable BOR permanently. Three BOR thresholds are available through option bytes. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for an external reset circuit.

The device also features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

Internal reset OFF

This feature is available only on packages featuring the PDR_ON pin. The internal power-on reset (POR) / power-down reset (PDR) circuitry is disabled with the PDR_ON pin.

An external power supply supervisor should monitor V_{DD} and should maintain the device in reset mode as long as V_{DD} is below a specified threshold. PDR_ON should be connected to this external power supply supervisor. Refer to *Figure 7: Power supply supervisor interconnection with internal reset OFF*.

Figure 7. Power supply supervisor interconnection with internal reset OFF
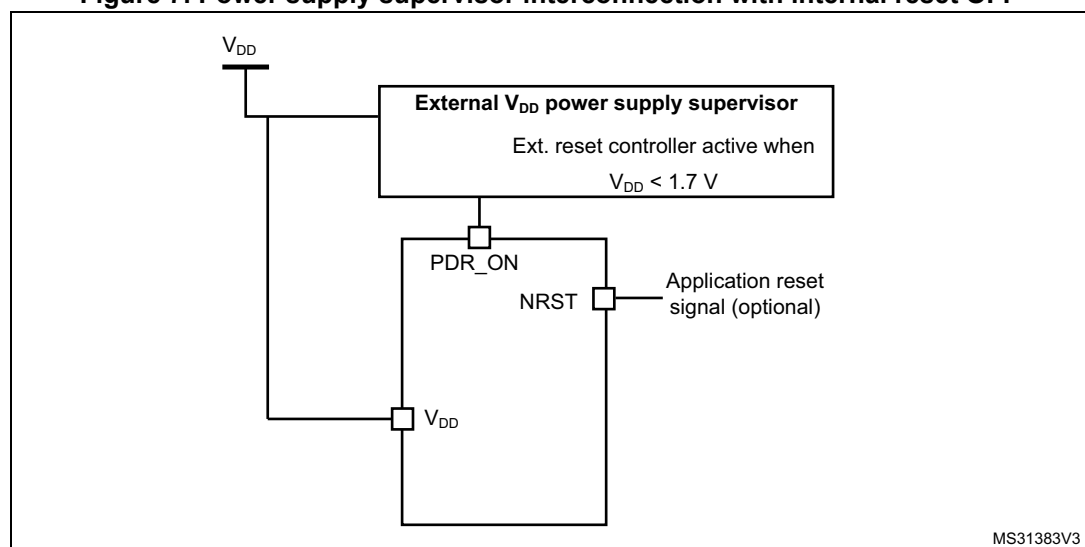
1. PDR = 1.7 V for reduce temperature range; PDR = 1.8 V for all temperature range.

The V_{DD} specified threshold, below which the device must be maintained under reset, is 1.8 V (see *Figure 7*). This supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range.

A comprehensive set of power-saving mode allows to design low-power applications.

When the internal reset is OFF, the following integrated features are no more supported:

- The integrated power-on reset (POR) / power-down reset (PDR) circuitry is disabled
- The brownout reset (BOR) circuitry is disabled
- The embedded programmable voltage detector (PVD) is disabled
- V_{BAT} functionality is no more available and V_{BAT} pin should be connected to V_{DD}

All packages, except for the LQFP64 and LQFP100, allow to disable the internal reset through the PDR_ON signal.

Table 8. FSMC pin definition (continued)

Pins[1]	FSMC				LQFP100[2]	WLCSP90 [2]
	CF	NOR/PSRAM/ SRAM	NOR/PSRAM Mux	NAND 16 bit		
PF1	A1	A1	-	-	-	-
PF2	A2	A2	-	-	-	-
PF3	A3	A3	-	-	-	-
PF4	A4	A4	-	-	-	-
PF5	A5	A5	-	-	-	-
PF6	NIORD	-	-	-	-	-
PF7	NREG	-	-	-	-	-
PF8	NIOWR	-	-	-	-	-
PF9	CD	-	-	-	-	-
PF10	INTR	-	-	-	-	-
PF12	A6	A6	-	-	-	-
PF13	A7	A7	-	-	-	-
PF14	A8	A8	-	-	-	-
PF15	A9	A9	-	-	-	-
PG0	A10	A10	-	-	-	-
PG1		A11	-	-	-	-
PE7	D4	D4	DA4	D4	Yes	Yes
PE8	D5	D5	DA5	D5	Yes	Yes
PE9	D6	D6	DA6	D6	Yes	Yes
PE10	D7	D7	DA7	D7	Yes	Yes
PE11	D8	D8	DA8	D8	Yes	Yes
PE12	D9	D9	DA9	D9	Yes	Yes
PE13	D10	D10	DA10	D10	Yes	Yes
PE14	D11	D11	DA11	D11	Yes	Yes
PE15	D12	D12	DA12	D12	Yes	Yes
PD8	D13	D13	DA13	D13	Yes	Yes
PD9	D14	D14	DA14	D14	Yes	Yes
PD10	D15	D15	DA15	D15	Yes	Yes
PD11	-	A16	A16	CLE	Yes	Yes
PD12	-	A17	A17	ALE	Yes	Yes
PD13	-	A18	A18	-	Yes	-
PD14	D0	D0	DA0	D0	Yes	Yes
PD15	D1	D1	DA1	D1	Yes	Yes

Table 25. Typical and maximum current consumptions in V$_{BAT}$ mode

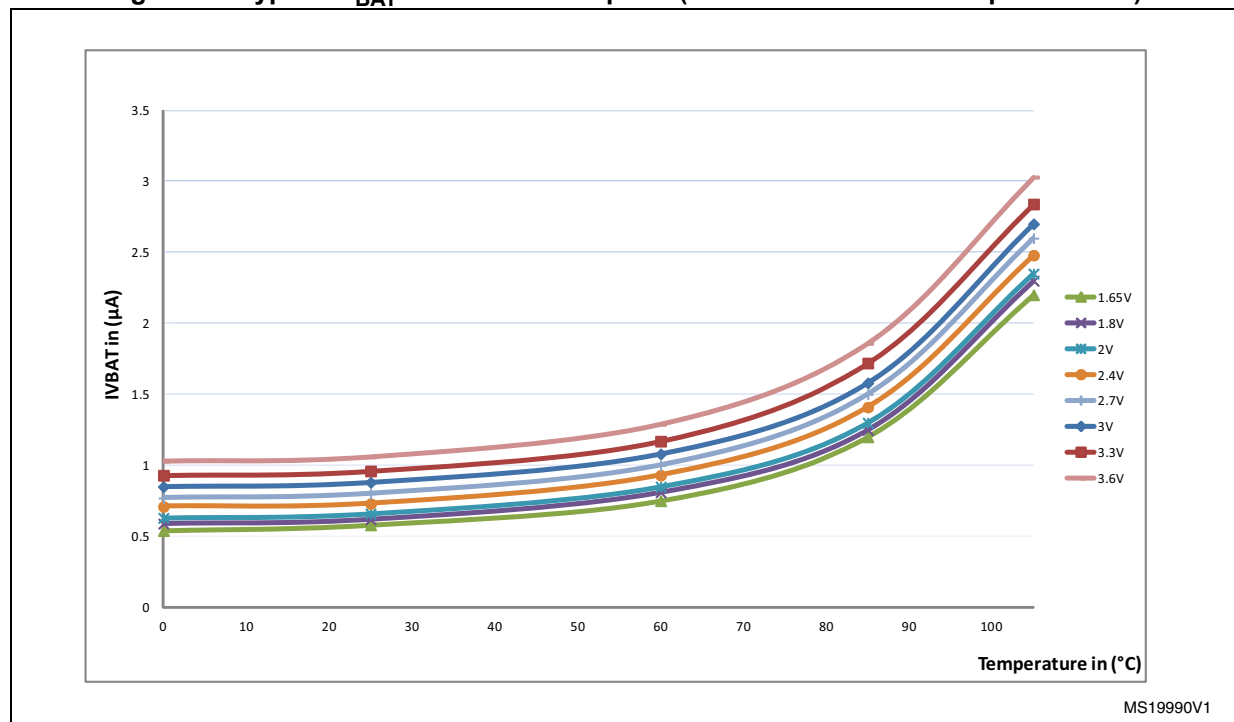| Symbol	Parameter	Conditions	Typ			Max[1]		Unit
			T$_A$ = 25 °C			T$_A$ = 85 °C	T$_A$ = 105 °C	
			V$_{BAT}$ = 1.8 V	V$_{BAT}$= 2.4 V	V$_{BAT}$ = 3.3 V	V$_{BAT}$ = 3.6 V		
I$_{DD\_VBAT}$	Backup domain supply current	Backup SRAM ON, low-speed oscillator and RTC ON	1.29	1.42	1.68	6	11	μA
		Backup SRAM OFF, low-speed oscillator and RTC ON	0.62	0.73	0.96	3	5	
		Backup SRAM ON, RTC OFF	0.79	0.81	0.86	5	10	
		Backup SRAM OFF, RTC OFF	0.10	0.10	0.10	2	4	

1. Guaranteed by characterization.

Figure 28. Typical V$_{BAT}$ current consumption (LSE and RTC ON/backup RAM OFF)

Table 27. Switching output I/O current consumption

Symbol	Parameter	Conditions[1]	I/O toggling frequency (f_{SW})	Typ	Unit
I_{DDIO}	I/O switching current	V_{DD} = 3.3 V[2] $C = C_{INT}$	2 MHz	0.02	mA
			8 MHz	0.14	
			25 MHz	0.51	
			50 MHz	0.86	
			60 MHz	1.30	
		V_{DD} = 3.3 V C_{EXT} = 0 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	0.10	
			8 MHz	0.38	
			25 MHz	1.18	
			50 MHz	2.47	
			60 MHz	2.86	
		V_{DD} = 3.3 V C_{EXT} = 10 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	0.17	
			8 MHz	0.66	
			25 MHz	1.70	
			50 MHz	2.65	
			60 MHz	3.48	
		V_{DD} = 3.3 V C_{EXT} = 22 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	0.23	
			8 MHz	0.95	
			25 MHz	3.20	
			50 MHz	4.69	
			60 MHz	8.06	
		V_{DD} = 3.3 V C_{EXT} = 33 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	0.30	
			8 MHz	1.22	
			25 MHz	3.90	
			50 MHz	8.82	
			60 MHz	-[3]	

1. C_S is the PCB board capacitance including the pad pin. C_S = 7 pF (estimated value).
2. This test is performed by cutting the LQFP package pin (pad removal).
3. At 60 MHz, C maximum load is specified 30 pF.

Figure 34. ACC$_{LSI}$ versus temperature

MS19013V1
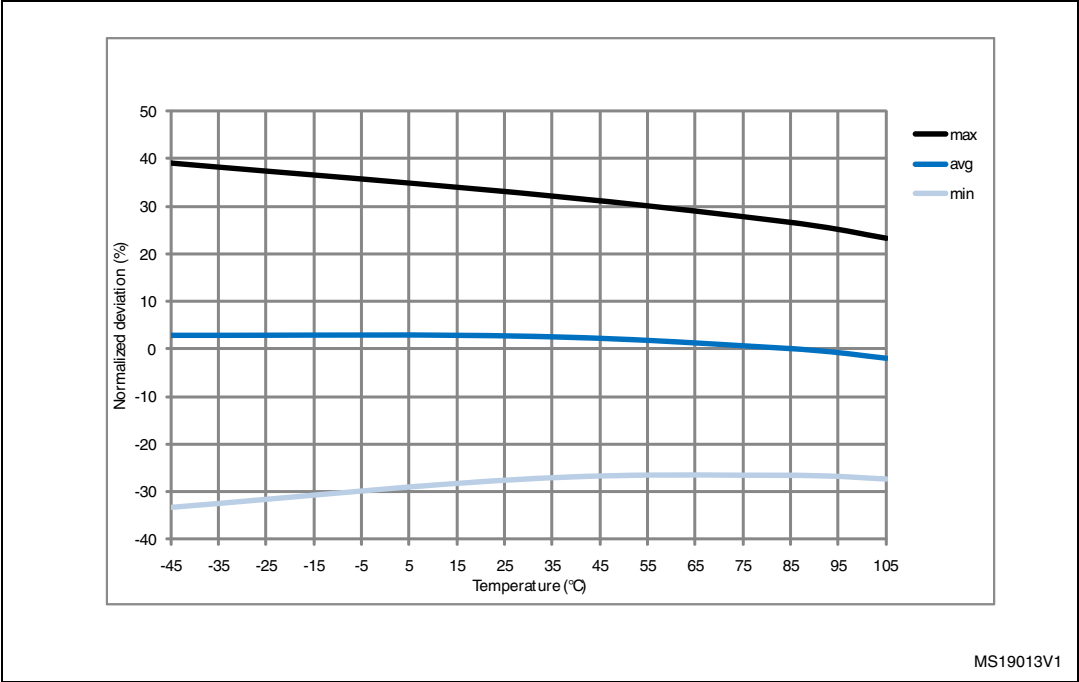
5.3.10 PLL characteristics

The parameters given in *Table 36* and *Table 37* are derived from tests performed under temperature and V$_{DD}$ supply voltage conditions summarized in *Table 14*.

Table 36. Main PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f$_{PLL\_IN}$	PLL input clock[1]	-	0.95[2]	1	2.10	MHz
f$_{PLL\_OUT}$	PLL multiplier output clock	-	24	-	168	MHz
f$_{PLL48\_OUT}$	48 MHz PLL multiplier output clock	-	-	48	75	MHz
f$_{VCO\_OUT}$	PLL VCO output	-	100	-	432	MHz
t$_{LOCK}$	PLL lock time	VCO freq = 100 MHz	75	-	200	μs
		VCO freq = 432 MHz	100	-	300	

Figure 36. PLL output clock waveforms in down spread mode
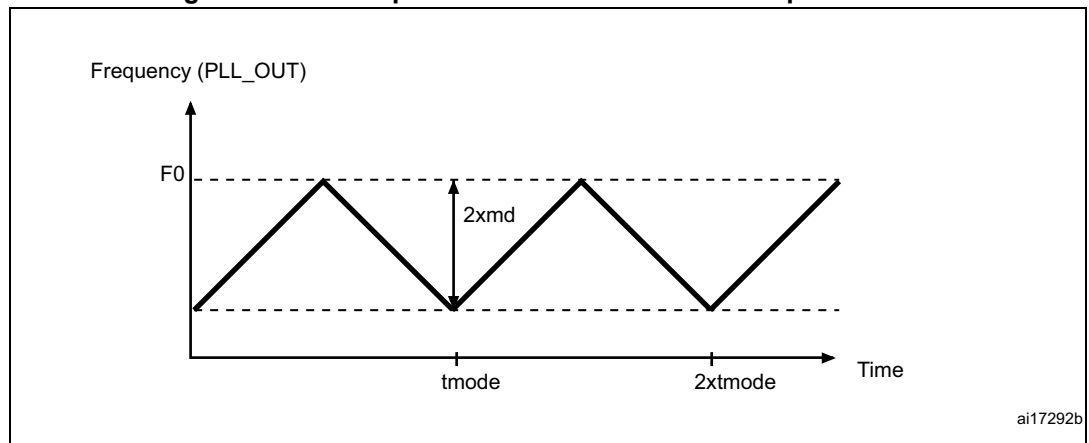
5.3.12 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 105 °C unless otherwise specified.

The devices are shipped to customers with the Flash memory erased.

Table 39. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current	Write / Erase 8-bit mode, V_{DD} = 1.8 V	-	5	-	mA
		Write / Erase 16-bit mode, V_{DD} = 2.1 V	-	8	-	
		Write / Erase 32-bit mode, V_{DD} = 3.3 V	-	12	-	

Table 40. Flash memory programming

Symbol	Parameter	Conditions	Min[1]	Typ	Max[1]	Unit
t_{prog}	Word programming time	Program/erase parallelism (PSIZE) = x 8/16/32	-	16	100[2]	µs
$t_{ERASE16KB}$	Sector (16 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	400	800	ms
		Program/erase parallelism (PSIZE) = x 16	-	300	600	
		Program/erase parallelism (PSIZE) = x 32	-	250	500	
$t_{ERASE64KB}$	Sector (64 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	1200	2400	ms
		Program/erase parallelism (PSIZE) = x 16	-	700	1400	
		Program/erase parallelism (PSIZE) = x 32	-	550	1100	

Table 50. I/O AC characteristics[1][2] (continued)

OSPEEDRy [1:0] bit value[1]	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
11	$F_{max(IO)out}$	Maximum frequency[3]	C_L = 30 pF, V_{DD} > 2.70 V	-	-	100[4]	MHz
			C_L = 30 pF, V_{DD} > 1.8 V	-	-	50[4]	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	180[4]	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	100[4]	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 30 pF, V_{DD} > 2.70 V	-	-	4	ns
			C_L = 30 pF, V_{DD} > 1.8 V	-	-	6	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	2.5	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	4	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller		10	-	-	ns

1. Guaranteed by characterization.

2. The I/O speed is configured using the OSPEEDRy[1:0] bits. Refer to the STM32F4xx reference manual for a description of the GPIOx_SPEEDR GPIO port output speed register.

3. The maximum frequency is defined in *Figure 37*.

4. For maximum frequencies above 50 MHz, the compensation cell should be used.

Figure 37. I/O AC characteristics definition

Maximum frequency is achieved if $(t_r + t_f) \leq (2/3)T$ and if the duty cycle is (45-55%) when loaded by CL specified in the table " *I/O AC characteristics*".

ai14131d
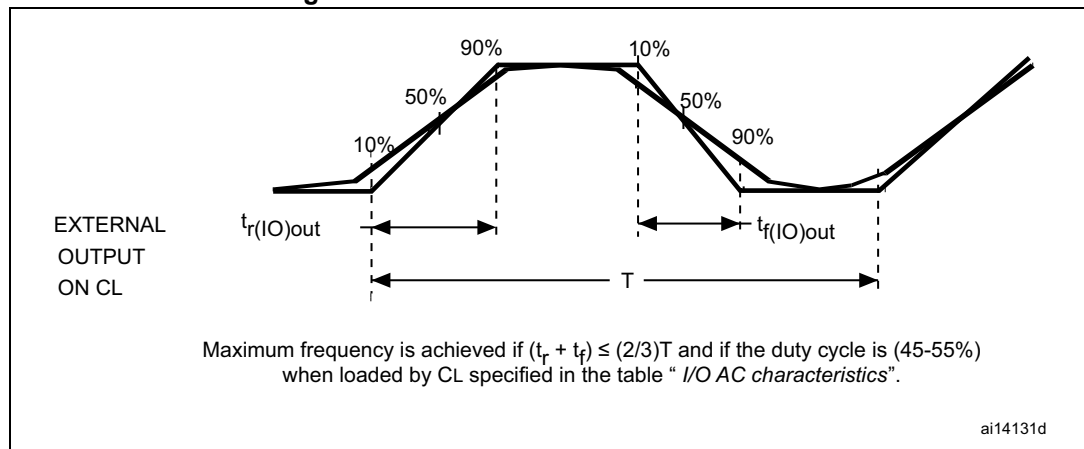
5.3.17 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 48*).

Unless otherwise specified, the parameters given in *Table 51* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Table 51. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$[1]	NRST Input low level voltage	TTL ports 2.7 V $\leq V_{DD} \leq$ 3.6 V	-	-	0.8	V
$V_{IH(NRST)}$[1]	NRST Input high level voltage		2	-	-	
$V_{IL(NRST)}$[1]	NRST Input low level voltage	CMOS ports 1.8 V $\leq V_{DD} \leq$ 3.6 V	-	-	$0.3V_{DD}$	
$V_{IH(NRST)}$[1]	NRST Input high level voltage		$0.7V_{DD}$	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor[2]	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$[1]	NRST Input filtered pulse		-	-	100	ns
$V_{NF(NRST)}$[1]	NRST Input not filtered pulse	$V_{DD} > 2.7$ V	300	-	-	ns
T_{NRST_OUT}	Generated reset pulse duration	Internal Reset source	20	-	-	µs

1. Guaranteed by design.

2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

Figure 38. Recommended NRST pin protection
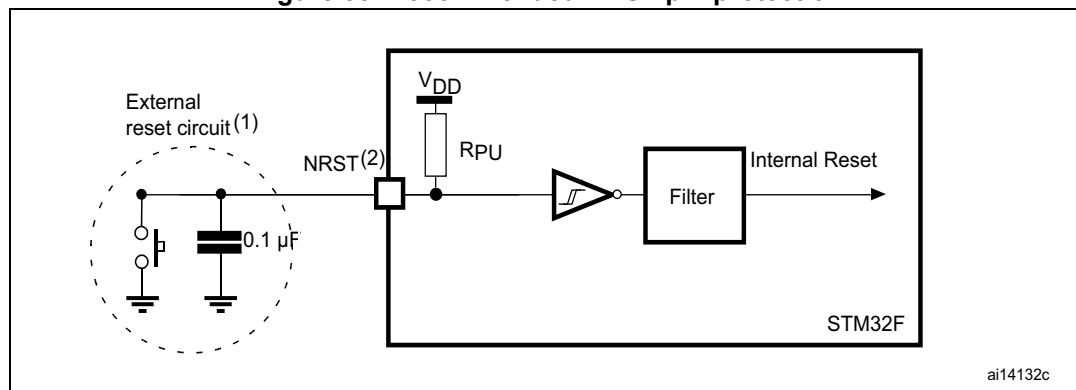
1. The reset network protects the device against parasitic resets.

2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 51*. Otherwise the reset is not taken into account by the device.

5.3.18 TIM timer characteristics

The parameters given in *Table 52* and *Table 53* are guaranteed by design.

Refer to *Section 5.3.16: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 52. Characteristics of TIMx connected to the APB1 domain[(1)]

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	AHB/APB1 prescaler distinct from 1, $f_{TIMxCLK}$ = 84 MHz	1	-	$t_{TIMxCLK}$
			11.9	-	ns
		AHB/APB1 prescaler = 1, $f_{TIMxCLK}$ = 42 MHz	1	-	$t_{TIMxCLK}$
			23.8	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	$f_{TIMxCLK}$ = 84 MHz APB1= 42 MHz	0	$f_{TIMxCLK}$/2	MHz
			0	42	MHz
Res_{TIM}	Timer resolution		-	16/32	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected		1	65536	$t_{TIMxCLK}$
			0.0119	780	µs
	32-bit counter clock period when internal clock is selected		1	-	$t_{TIMxCLK}$
			0.0119	51130563	µs
t_{MAX_COUNT}	Maximum possible count		-	65536 × 65536	$t_{TIMxCLK}$
			-	51.1	s

1. TIMx is used as a general term to refer to the TIM2, TIM3, TIM4, TIM5, TIM6, TIM7, and TIM12 timers.
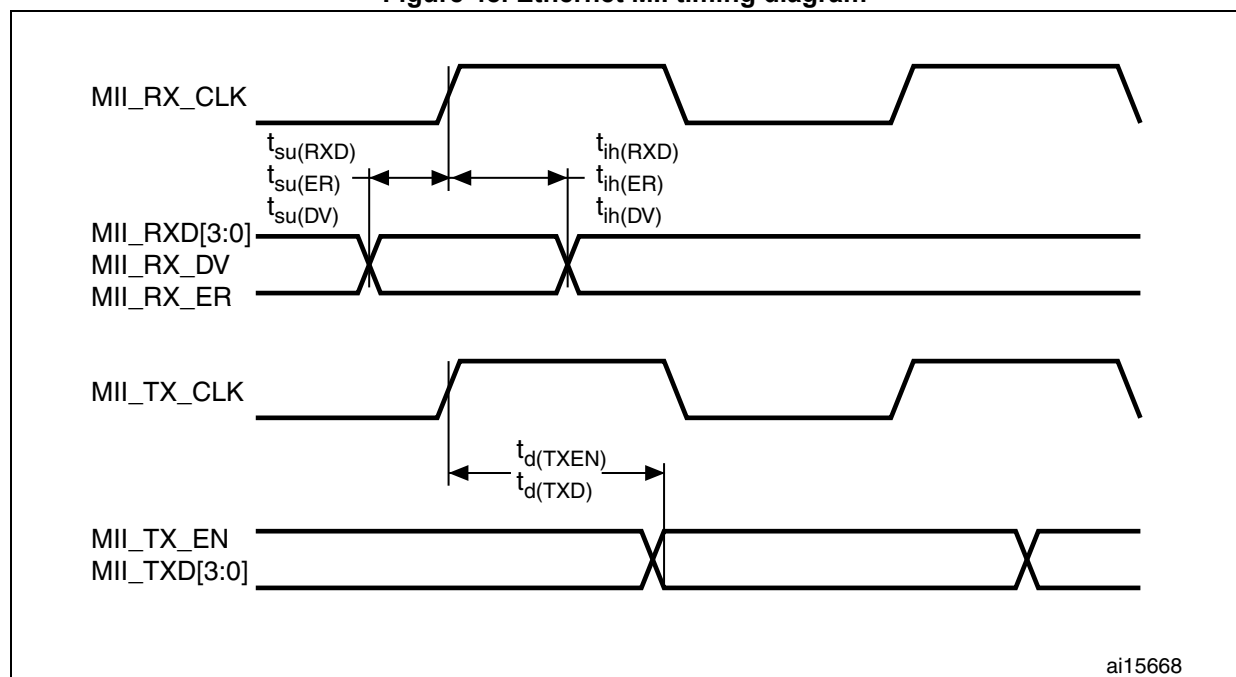
Figure 47. Ethernet RMII timing diagram
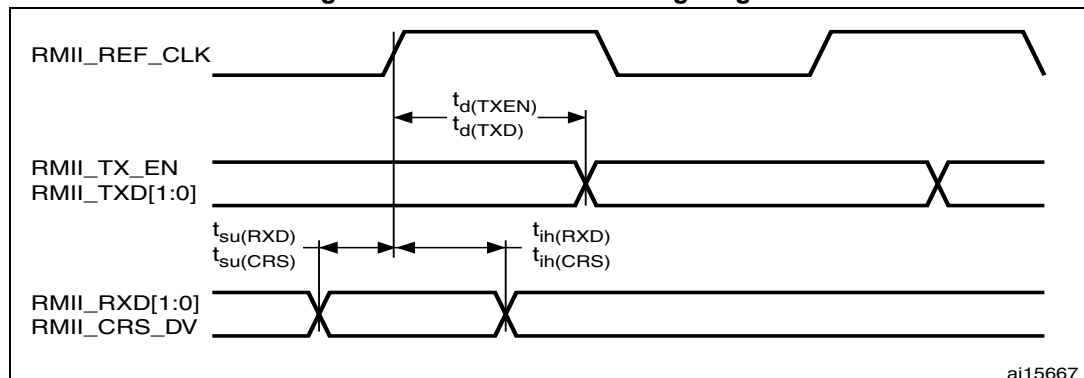
Table 65. Dynamic characteristics: Ethernet MAC signals for RMII

Symbol	Rating	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	2	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	1	-	-	ns
$t_{su(CRS)}$	Carrier sense set-up time	0.5	-	-	ns
$t_{ih(CRS)}$	Carrier sense hold time	2	-	-	ns
$t_{d(TXEN)}$	Transmit enable valid delay time	8	9.5	11	ns
$t_{d(TXD)}$	Transmit data valid delay time	8.5	10	11.5	ns

Table 66 gives the list of Ethernet MAC signals for MII and *Figure 47* shows the corresponding timing diagram.

Figure 48. Ethernet MII timing diagram

Table 74. DAC characteristics (continued)

Symbol	Parameter	Min	Typ	Max	Unit	Comments
R_{LOAD}[2]	Resistive load with buffer ON	5	-	-	kΩ	
R_O[2]	Impedance output with buffer OFF	-	-	15	kΩ	When the buffer is OFF, the Minimum resistive load between DAC_OUT and V_{SS} to have a 1% accuracy is 1.5 MΩ
C_{LOAD}[2]	Capacitive load	-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
DAC_OUT min[2]	Lower DAC_OUT voltage with buffer ON	0.2	-	-	V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at V_{REF+} = 3.6 V and (0x1C7) to (0xE38) at V_{REF+} = 1.8 V
DAC_OUT max[2]	Higher DAC_OUT voltage with buffer ON	-	-	$V_{DDA} - 0.2$	V	
DAC_OUT min[2]	Lower DAC_OUT voltage with buffer OFF	-	0.5	-	mV	It gives the maximum output excursion of the DAC.
DAC_OUT max[2]	Higher DAC_OUT voltage with buffer OFF	-	-	$V_{REF+} - 1LSB$	V	
I_{VREF+}[4]	DAC DC V_{REF} current consumption in quiescent mode (Standby mode)	-	170	240	µA	With no load, worst code (0x800) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs
		-	50	75		With no load, worst code (0xF1C) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs
I_{DDA}[4]	DAC DC VDDA current consumption in quiescent mode[3]	-	280	380	µA	With no load, middle code (0x800) on the inputs
		-	475	625	µA	With no load, worst code (0xF1C) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs
DNL[4]	Differential non linearity Difference between two consecutive code-1LSB)	-	-	±0.5	LSB	Given for the DAC in 10-bit configuration.
		-	-	±2	LSB	Given for the DAC in 12-bit configuration.
INL[4]	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)	-	-	±1	LSB	Given for the DAC in 10-bit configuration.
		-	-	±4	LSB	Given for the DAC in 12-bit configuration.

**Table 90. WLCSP90 - 4.223 x 3.969 mm, 0.400 mm pitch wafer level chip scale package mechanical data**

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.540	0.570	0.600	0.0213	0.0224	0.0236
A1	-	0.190	-	-	0.0075	-
A2	-	0.380	-	-	0.0150	-
A3[2]	-	0.025	-	-	0.0010	-
b[3]	0.240	0.270	0.300	0.0094	0.0106	0.0118
D	4.188	4.223	4.258	0.1649	0.1663	0.1676
E	3.934	3.969	4.004	0.1549	0.1563	0.1576
e	-	0.400	-	-	0.0157	-
e1	-	3.600	-	-	0.1417	-
e2	-	3.200	-	-	0.1260	-
F	-	0.3115	-	-	0.0123	-
G	-	0.3845	-	-	0.0151	-
aaa	-	0.100	-	-	0.0039	-
bbb	-	0.100	-	-	0.0039	-
ccc	-	0.100	-	-	0.0039	-
ddd	-	0.050	-	-	0.0020	-
eee	-	0.050	-	-	0.0020	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.
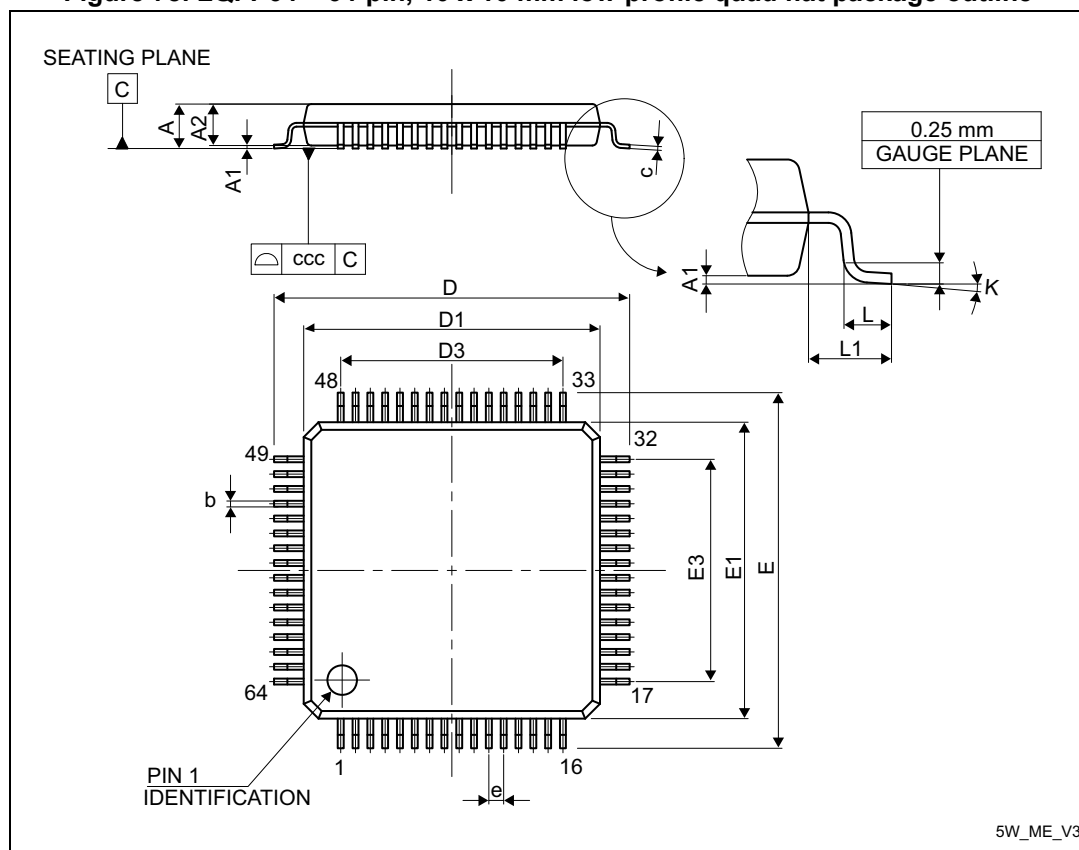
2. Back side coating.

3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Figure 76. WLCSP90 - 4.223 x 3.969 mm, 0.400 mm pitch wafer level chip scale recommended footprint

MS18965V2
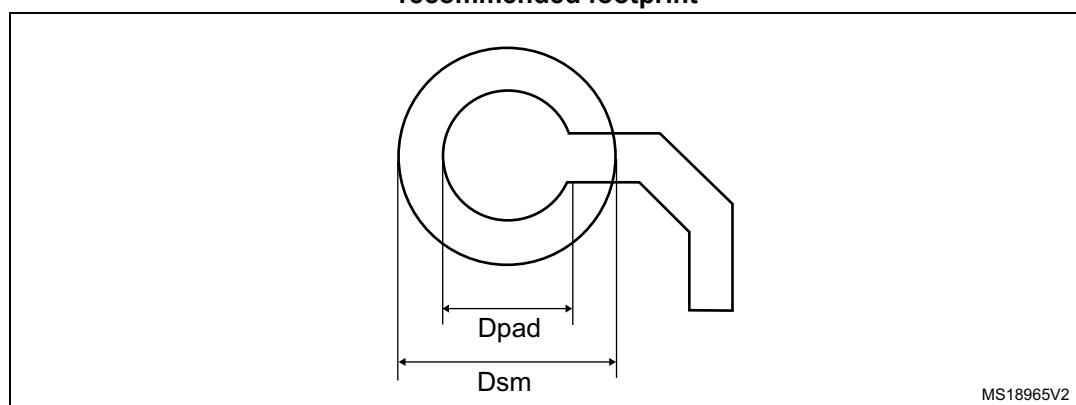
6.2 LQFP64 package information

Figure 78. LQFP64 – 64-pin, 10 x 10 mm low-profile quad flat package outline


5W_ME_V3

1. Drawing is not to scale.

Table 92. LQFP64 – 64-pin 10 x 10 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-

# Appendix A Application block diagrams

A.1 USB OTG full speed (FS) interface solutions

Figure 93. USB controller configured as peripheral-only and used in Full speed mode
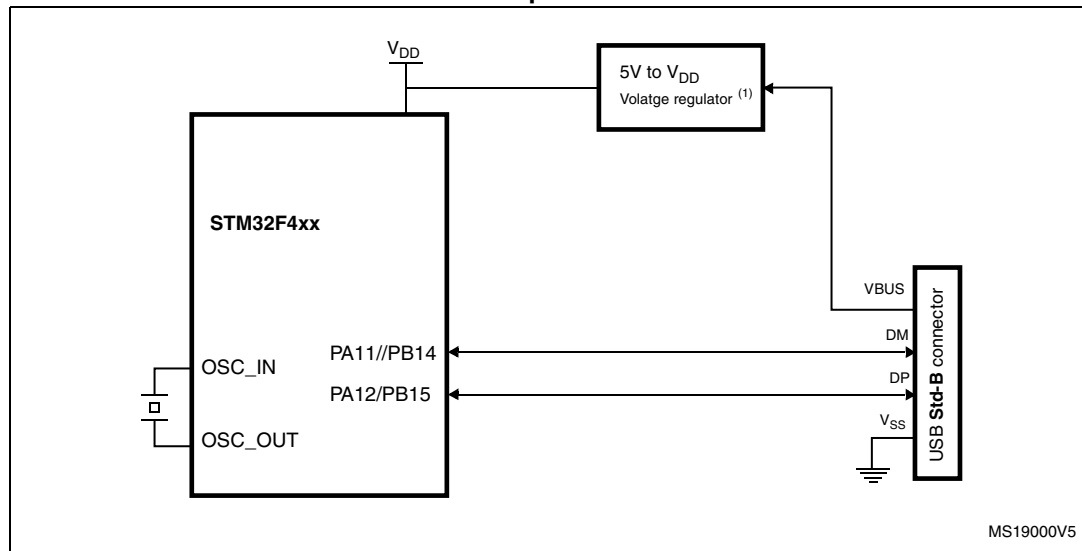
1. External voltage regulator only needed when building a V_{BUS} powered device.

2. The same application can be developed using the OTG HS in FS mode to achieve enhanced performance thanks to the large Rx/Tx FIFO and to a dedicated DMA controller.

Figure 94. USB controller configured as host-only and used in full speed mode
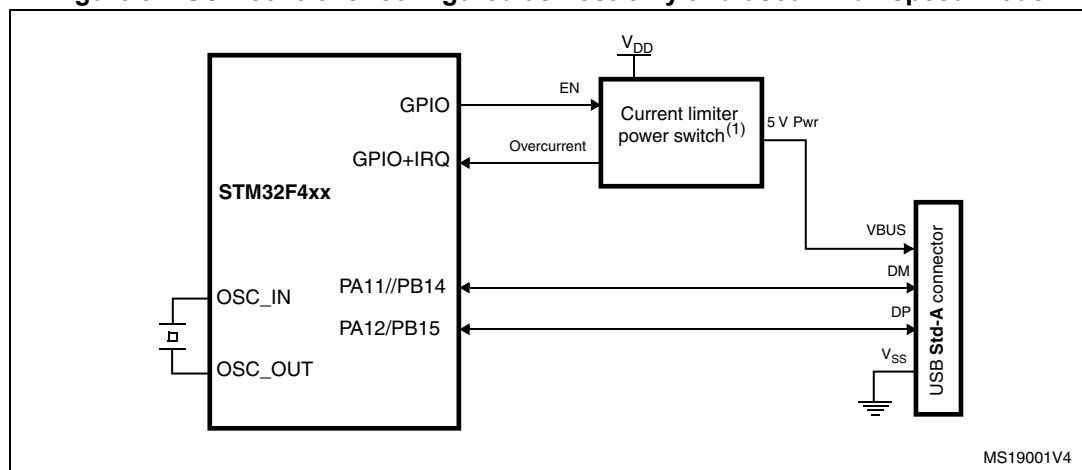
1. The current limiter is required only if the application has to support a V_{BUS} powered device. A basic power switch can be used if 5 V are available on the application board.

2. The same application can be developed using the OTG HS in FS mode to achieve enhanced performance thanks to the large Rx/Tx FIFO and to a dedicated DMA controller.

Table 100. Document revision history (continued)

Date	Revision	Changes
31-May-2012	3	Updated *Figure 5: STM32F40xxx block diagram* and *Figure 7: Power supply supervisor interconnection with internal reset OFF* Added SDIO, added notes related to FSMC and SPI/I2S in *Table 2: STM32F405xx and STM32F407xx: features and peripheral counts*. Starting from Silicon revision Z, USB OTG full-speed interface is now available for all STM32F405xx devices. Added full information on WLCSP90 package together with corresponding part numbers. Changed number of AHB buses to 3. Modified available Flash memory sizes in *Section 2.2.4: Embedded Flash memory*. Modified number of maskable interrupt channels in *Section 2.2.10: Nested vectored interrupt controller (NVIC)*. Updated case of Regulator ON/internal reset ON, Regulator ON/internal reset OFF, and Regulator OFF/internal reset ON in *Section 2.2.16: Voltage regulator*. Updated standby mode description in *Section 2.2.19: Low-power modes*. Added *Note 1* below *Figure 16: STM32F40xxx UFBGA176 ballout*. Added *Note 1* below *Figure 17: STM32F40xxx WLCSP90 ballout*. Updated *Table 7: STM32F40xxx pin and ball definitions*. Added *Table 8: FSMC pin definition*. Removed OTG_HS_INTN alternate function in *Table 7: STM32F40xxx pin and ball definitions* and *Table 9: Alternate function mapping*. Removed I2S2_WS on PB6/AF5 in *Table 9: Alternate function mapping*. Replaced JTRST by NJTRST, removed ETH_RMII _TX_CLK, and modified I2S3ext_SD on PC11 in *Table 9: Alternate function mapping*. Added *Table 10: register boundary addresses*. Updated *Figure 18: STM32F40xxx memory map*. Updated V_{DDA} and V_{REF+} decoupling capacitor in *Figure 21: Power supply scheme*. Added power dissipation maximum value for WLCSP90 in *Table 14: General operating conditions*. Updated $V_{POR/PDR}$ in *Table 19: Embedded reset and power control block characteristics*. Updated notes in *Table 21: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled)*, *Table 20: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled) or RAM*, and *Table 22: Typical and maximum current consumption in Sleep mode*. Updated maximum current consumption at T_A = 25 °n *Table 23: Typical and maximum current consumptions in Stop mode*.