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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	168MHz
Connectivity	CANbus, DCMI, EBI/EMI, Ethernet, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f407vgt6tr

- 8- to 14-bit parallel camera interface up to 54 Mbytes/s
- True random number generator
- CRC calculation unit
- 96-bit unique ID
- RTC: subsecond accuracy, hardware calendar

Table 1. Device summary

Reference	Part number
STM32F405xx	STM32F405RG, STM32F405VG, STM32F405ZG, STM32F405OG, STM32F405OE
STM32F407xx	STM32F407VG, STM32F407IG, STM32F407ZG, STM32F407VE, STM32F407ZE, STM32F407IE

General-purpose timers (TIMx)

There are ten synchronizable general-purpose timers embedded in the STM32F40xxx devices (see *Table 4* for differences).

- **TIM2, TIM3, TIM4, TIM5**

  The STM32F40xxx include 4 full-featured general-purpose timers: TIM2, TIM5, TIM3, and TIM4.The TIM2 and TIM5 timers are based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. The TIM3 and TIM4 timers are based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They all feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input capture/output compare/PWMs on the largest packages.

  The TIM2, TIM3, TIM4, TIM5 general-purpose timers can work together, or with the other general-purpose timers and the advanced-control timers TIM1 and TIM8 via the Timer Link feature for synchronization or event chaining.

  Any of these general-purpose timers can be used to generate PWM outputs.

  TIM2, TIM3, TIM4, TIM5 all have independent DMA request generation. They are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 4 hall-effect sensors.

- **TIM9, TIM10, TIM11, TIM12, TIM13, and TIM14**

  These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM10, TIM11, TIM13, and TIM14 feature one independent channel, whereas TIM9 and TIM12 have two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers. They can also be used as simple time bases.

Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger and waveform generation. They can also be used as a generic 16-bit time base.

TIM6 and TIM7 support independent DMA request generation.

Independent watchdog

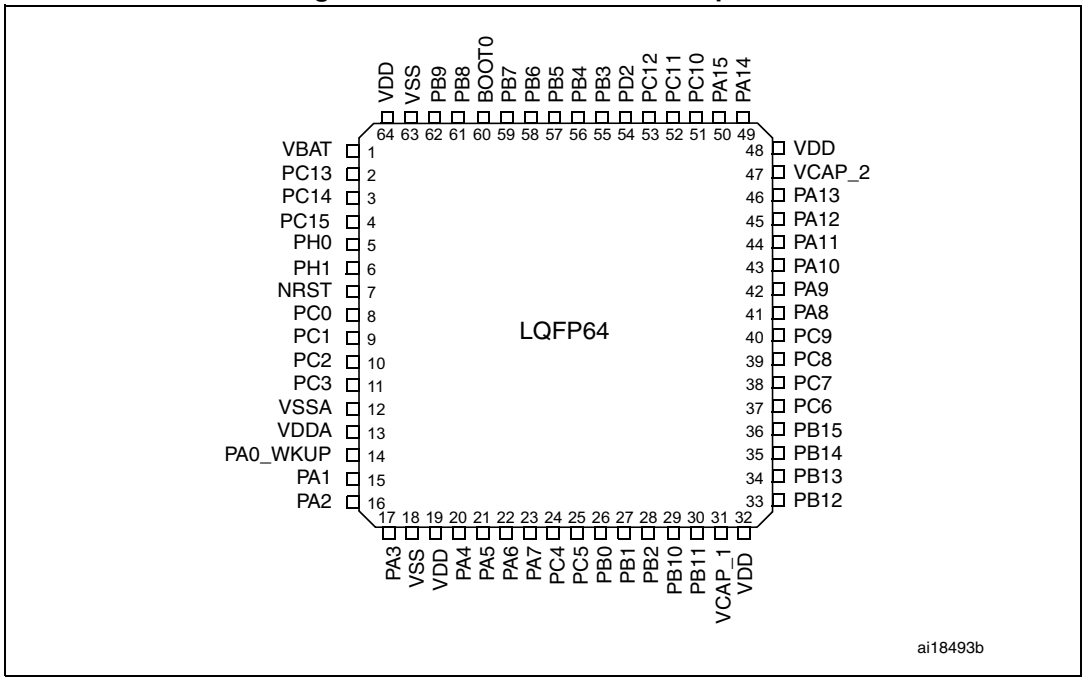
The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes.

Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

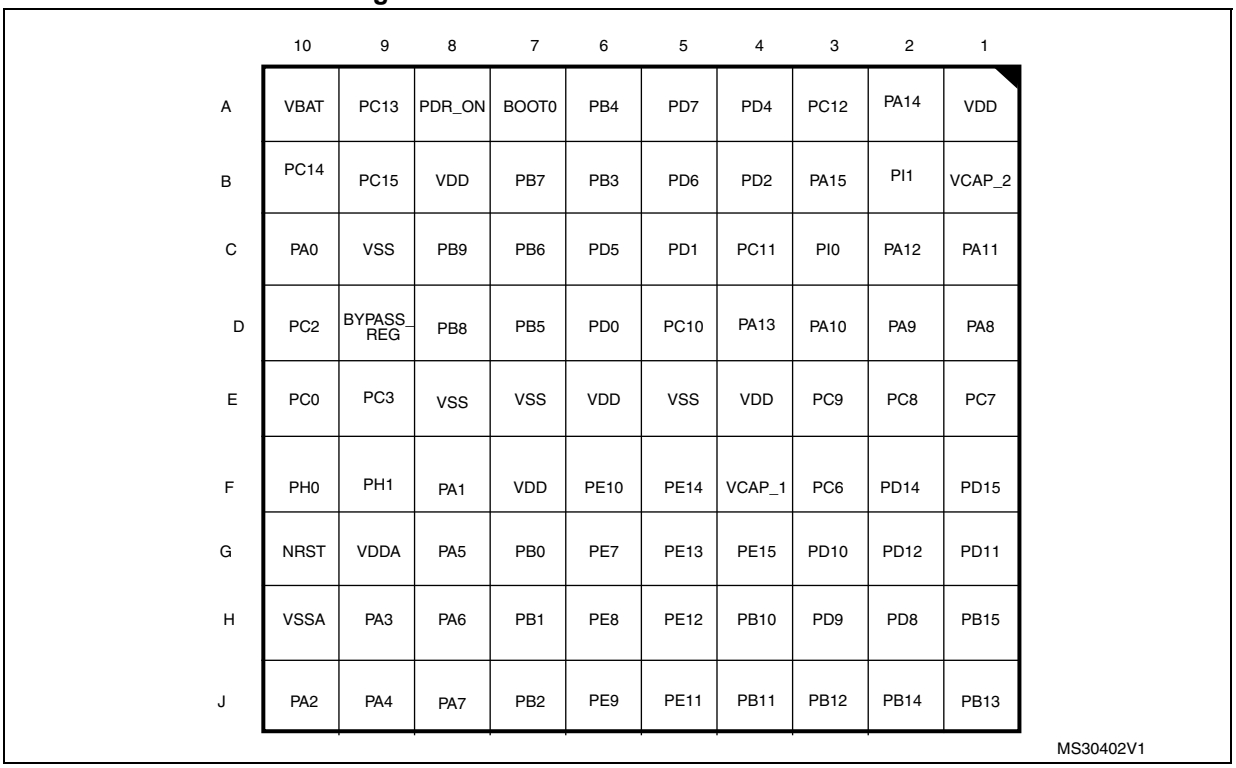
3 Pinouts and pin description

Figure 12. STM32F40xxx LQFP64 pinout



1. The above figure shows the package top view.

Figure 17. STM32F40xxx WLCSP90 ballout



1. This figure shows the package bump view.

Table 6. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
I/O structure	FT	5 V tolerant I/O
	TTa	3.3 V tolerant I/O directly connected to ADC
	B	Dedicated BOOT0 pin
	RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Alternate functions	Functions selected through GPIOx_AFR registers	
Additional functions	Functions directly selected/enabled through peripheral registers	

Table 8. FSMC pin definition (continued)

Pins[1]	FSMC				LQFP100[2]	WLCSP90 (2)
	CF	NOR/PSRAM/ SRAM	NOR/PSRAM Mux	NAND 16 bit		
PG2	-	A12	-	-	-	-
PG3	-	A13	-	-	-	-
PG4	-	A14	-	-	-	-
PG5	-	A15	-	-	-	-
PG6	-	-	-	INT2	-	-
PG7	-	-	-	INT3	-	-
PD0	D2	D2	DA2	D2	Yes	Yes
PD1	D3	D3	DA3	D3	Yes	Yes
PD3	-	CLK	CLK	-	Yes	-
PD4	NOE	NOE	NOE	NOE	Yes	Yes
PD5	NWE	NWE	NWE	NWE	Yes	Yes
PD6	NWAIT	NWAIT	NWAIT	NWAIT	Yes	Yes
PD7	-	NE1	NE1	NCE2	Yes	Yes
PG9	-	NE2	NE2	NCE3	-	-
PG10	NCE4_1	NE3	NE3	-	-	-
PG11	NCE4_2	-	-	-	-	-
PG12	-	NE4	NE4	-	-	-
PG13	-	A24	A24	-	-	-
PG14	-	A25	A25	-	-	-
PB7	-	NADV	NADV	-	Yes	Yes
PE0	-	NBL0	NBL0	-	Yes	-
PE1	-	NBL1	NBL1	-	Yes	-

1. Full FSMC features are available on LQFP144, LQFP176, and UFBGA176. The features available on smaller packages are given in the dedicated package column.
2. Ports F and G are not available in devices delivered in 100-pin packages.

Table 9. Alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/SPI2/I2S2/I2S2ext	SPI3/I2Sext/I2S3	USART1/2/3/I2S3ext	UART4/5/USART6	CAN1/2 TIM12/13/14	OTG_FS/OTG_HS	ETH	FSMC/SDIO/OTG_FS	DCMI		
Port F	PF0	-	-	-	-	I2C2_SDA	-	-	-	-	-	-	-	FSMC_A0	-	-	EVENTOUT
	PF1	-	-	-	-	I2C2_SCL	-	-	-	-	-	-	-	FSMC_A1	-	-	EVENTOUT
	PF2	-	-	-	-	I2C2_SMBA	-	-	-	-	-	-	-	FSMC_A2	-	-	EVENTOUT
	PF3	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A3	-	-	EVENTOUT
	PF4	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A4	-	-	EVENTOUT
	PF5	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A5	-	-	EVENTOUT
	PF6	-	-	-	TIM10_CH1	-	-	-	-	-	-	-	-	FSMC_NIORD	-	-	EVENTOUT
	PF7	-	-	-	TIM11_CH1	-	-	-	-	-	-	-	-	FSMC_NREG	-	-	EVENTOUT
	PF8	-	-	-	-	-	-	-	-	-	TIM13_CH1	-	-	FSMC_NIOWR	-	-	EVENTOUT
	PF9	-	-	-	-	-	-	-	-	-	TIM14_CH1	-	-	FSMC_CD	-	-	EVENTOUT
	PF10	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_INTR	-	-	EVENTOUT
	PF11	-	-	-	-	-	-	-	-	-	-	-	-		DCMI_D12	-	EVENTOUT
	PF12	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A6	-	-	EVENTOUT
	PF13	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A7	-	-	EVENTOUT
	PF14	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A8	-	-	EVENTOUT
	PF15	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A9	-	-	EVENTOUT

Table 9. Alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10 /11	I2C1/2/3	SPI1/SPI2/ I2S2/I2S2ext	SPI3/I2Sext /I2S3	USART1/2/3/ I2S3ext	UART4/5/ USART6	CAN1/2 TIM12/13/ 14	OTG_FS/ OTG_HS	ETH	FSMC/SDIO /OTG_FS	DCMI		
Port G	PG0	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A10	-	-	EVENTOUT
	PG1	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A11	-	-	EVENTOUT
	PG2	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A12	-	-	EVENTOUT
	PG3	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A13	-	-	EVENTOUT
	PG4	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A14	-	-	EVENTOUT
	PG5	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A15	-	-	EVENTOUT
	PG6	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_INT2	-	-	EVENTOUT
	PG7	-	-	-	-	-	-	-	-	USART6_CK	-	-	-	FSMC_INT3	-	-	EVENTOUT
	PG8	-	-	-	-	-	-	-	-	USART6_ RTS	-	-	ETH _PPS_OUT	-	-	-	EVENTOUT
	PG9	-	-	-	-	-	-	-	-	USART6_RX	-	-	-	FSMC_NE2/ FSMC_NCE3	-	-	EVENTOUT
	PG10	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_ NCE4_1/ FSMC_NE3	-	-	EVENTOUT
	PG11	-	-	-	-	-	-	-	-	-	-	-	ETH _MII_TX_EN ETH _RMII_ TX_EN	FSMC_NCE4_ 2	-	-	EVENTOUT
	PG12	-	-	-	-	-	-	-	-	USART6_ RTS	-	-	-	FSMC_NE4	-	-	EVENTOUT
	PG13	-	-	-	-	-	-	-	-	UART6_CTS	-	-	ETH _MII_TXD0 ETH _RMII_TXD0	FSMC_A24	-	-	EVENTOUT
	PG14	-	-	-	-	-	-	-	-	USART6_TX	-	-	ETH _MII_TXD1 ETH _RMII_TXD1	FSMC_A25	-	-	EVENTOUT
	PG15	-	-	-	-	-	-	-	-	USART6_ CTS	-	-	-	-	DCMI_D13	-	EVENTOUT

Table 9. Alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/SPI2/I2S2/I2S2ext	SPI3/I2Sext/I2S3	USART1/2/3/I2S3ext	UART4/5/USART6	CAN1/2 TIM12/13/14	OTG_FS/OTG_HS	ETH	FSMC/SDIO/OTG_FS	DCMI		
Port I	PI0	-	-	TIM5_CH4	-	-	SPI2_NSS I2S2_WS	-	-	-	-	-	-	-	DCMI_D13	-	EVENTOUT
	PI1	-	-	-	-	-	SPI2_SCK I2S2_CK	-	-	-	-	-	-	-	DCMI_D8	-	EVENTOUT
	PI2	-	-	-	TIM8_CH4	-	SPI2_MISO	I2S2ext_SD	-	-	-	-	-	-	DCMI_D9	-	EVENTOUT
	PI3	-	-	-	TIM8_ETR	-	SPI2_MOSI I2S2_SD	-	-	-	-	-	-	-	DCMI_D10	-	EVENTOUT
	PI4	-	-	-	TIM8_BKIN	-	-	-	-	-	-	-	-	-	DCMI_D5	-	EVENTOUT
	PI5	-	-	-	TIM8_CH1	-	-	-	-	-	-	-	-	-	DCMI_VSYNC	-	EVENTOUT
	PI6	-	-	-	TIM8_CH2	-	-	-	-	-	-	-	-	-	DCMI_D6	-	EVENTOUT
	PI7	-	-	-	TIM8_CH3	-	-	-	-	-	-	-	-	-	DCMI_D7	-	EVENTOUT
	PI8	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PI9	-	-	-	-	-	-	-	-	-	CAN1_RX	-	-	-	-	-	EVENTOUT
	PI10	-	-	-	-	-	-	-	-	-	-	-	ETH _MII_RX_ER	-	-	-	EVENTOUT
	PI11	-	-	-	-	-	-	-	-	-	-	OTG_HS_ULPI_DIR	-	-	-	-	EVENTOUT

Table 14. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{12}	Regulator ON: 1.2 V internal voltage on V_{CAP_1}/V_{CAP_2} pins	VOS bit in PWR_CR register = 0(1) Max frequency 144MHz	1.08	1.14	1.20	V
		VOS bit in PWR_CR register= 1 Max frequency 168MHz	1.20	1.26	1.32	V
	Regulator OFF: 1.2 V external voltage must be supplied from external regulator on V_{CAP_1}/V_{CAP_2} pins	Max frequency 144MHz	1.10	1.14	1.20	V
		Max frequency 168MHz	1.20	1.26	1.30	V
V_{IN}	Input voltage on RST and FT pins(6)	2 V ≤ V_{DD} ≤ 3.6 V	–0.3	-	5.5	V
		V_{DD} ≤ 2 V	–0.3	-	5.2	
	Input voltage on TTa pins	-	–0.3	-	V_{DDA}+ 0.3	
	Input voltage on B pin	-	-	-	5.5	
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(7)	LQFP64	-	-	435	mW
		LQFP100	-	-	465	
		LQFP144	-	-	500	
		LQFP176	-	-	526	
		UFBGA176	-	-	513	
		WLCSP90	-	-	543	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	–40	-	85	°C
		Low-power dissipation(8)	–40	-	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	–40	-	105	°C
		Low-power dissipation(8)	–40	-	125	
T_J	Junction temperature range	6 suffix version	–40	-	105	°C
		7 suffix version	–40	-	125	

1. The average expected gain in power consumption when VOS = 0 compared to VOS = 1 is around 10% for the whole temperature range, when the system clock frequency is between 30 and 144 MHz.
2. V_{DD}/V_{DDA} minimum value of 1.7 V is obtained when the device operates in reduced temperature range, and with the use of an external power supply supervisor (refer to *Section : Internal reset OFF*).
3. When the ADC is used, refer to *Table 67: ADC characteristics*.
4. If V_{REF+} pin is present, it must respect the following condition: V_{DDA}-V_{REF+} < 1.2 V.
5. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and power-down operation.
6. To sustain a voltage higher than V_{DD}+0.3, the internal pull-up and pull-down resistors must be disabled.
7. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax}.
8. In low-power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax}.

5.3.5 Embedded reset and power control block characteristics

The parameters given in *Table 19* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Table 19. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.09	2.14	2.19	V
		PLS[2:0]=000 (falling edge)	1.98	2.04	2.08	V
		PLS[2:0]=001 (rising edge)	2.23	2.30	2.37	V
		PLS[2:0]=001 (falling edge)	2.13	2.19	2.25	V
		PLS[2:0]=010 (rising edge)	2.39	2.45	2.51	V
		PLS[2:0]=010 (falling edge)	2.29	2.35	2.39	V
		PLS[2:0]=011 (rising edge)	2.54	2.60	2.65	V
		PLS[2:0]=011 (falling edge)	2.44	2.51	2.56	V
		PLS[2:0]=100 (rising edge)	2.70	2.76	2.82	V
		PLS[2:0]=100 (falling edge)	2.59	2.66	2.71	V
		PLS[2:0]=101 (rising edge)	2.86	2.93	2.99	V
		PLS[2:0]=101 (falling edge)	2.65	2.84	2.92	V
		PLS[2:0]=110 (rising edge)	2.96	3.03	3.10	V
		PLS[2:0]=110 (falling edge)	2.85	2.93	2.99	V
		PLS[2:0]=111 (rising edge)	3.07	3.14	3.21	V
		PLS[2:0]=111 (falling edge)	2.95	3.03	3.09	V
$V_{PVDhyst}$(1)	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power-on/power-down reset threshold	Falling edge	1.60	1.68	1.76	V
		Rising edge	1.64	1.72	1.80	V
$V_{PDRhyst}$(1)	PDR hysteresis	-	-	40	-	mV
V_{BOR1}	Brownout level 1 threshold	Falling edge	2.13	2.19	2.24	V
		Rising edge	2.23	2.29	2.33	V

Table 19. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BOR2}	Brownout level 2 threshold	Falling edge	2.44	2.50	2.56	V
		Rising edge	2.53	2.59	2.63	V
V_{BOR3}	Brownout level 3 threshold	Falling edge	2.75	2.83	2.88	V
		Rising edge	2.85	2.92	2.97	V
$V_{BORhyst}$(1)	BOR hysteresis	-	-	100	-	mV
$T_{RSTTEMPO}$(1)(2)	Reset temporization	-	0.5	1.5	3.0	ms
I_{RUSH}(1)	InRush current on voltage regulator power-on (POR or wakeup from Standby)	-	-	160	200	mA
E_{RUSH}(1)	InRush energy on voltage regulator power-on (POR or wakeup from Standby)	V_{DD} = 1.8 V, T_A = 105 °C, I_{RUSH} = 171 mA for 31 µs	-	-	5.4	µC

1. Guaranteed by design.
2. The reset temporization is measured from the power-on (POR reset or wakeup from V_{BAT}) to the instant when first instruction is read by the user application code.

5.3.6 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.
The current consumption is measured as described in *Figure 22: Current consumption measurement scheme*.

All Run mode current consumption measurements given in this section are performed using a CoreMark-compliant code.

Typical and maximum current consumption

The MCU is placed under the following conditions:

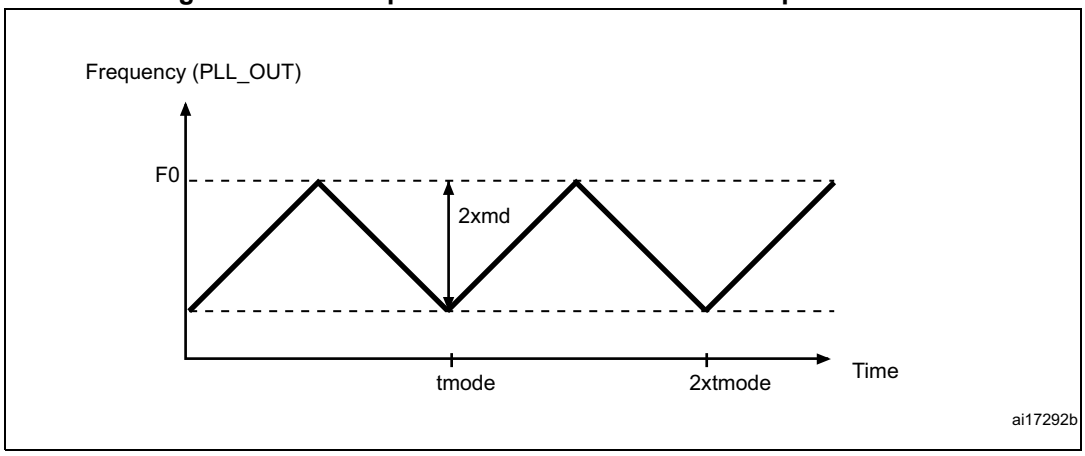
- At startup, all I/O pins are configured as analog inputs by firmware.
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash memory access time is adjusted to f_{HCLK} frequency (0 wait state from 0 to 30 MHz, 1 wait state from 30 to 60 MHz, 2 wait states from 60 to 90 MHz, 3 wait states from 90 to 120 MHz, 4 wait states from 120 to 150 MHz, and 5 wait states from 150 to 168 MHz).
- When the peripherals are enabled HCLK is the system clock, $f_{PCLK1} = f_{HCLK}/4$, and $f_{PCLK2} = f_{HCLK}/2$, except is explicitly mentioned.
- The maximum values are obtained for V_{DD} = 3.6 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Table 22. Typical and maximum current consumption in Sleep mode

Symbol	Parameter	Conditions	f_{HCLK}	Typ	Max(1)		Unit
				T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Sleep mode	External clock(2), all peripherals enabled(3)	168 MHz	59	77	84	mA
			144 MHz	46	61	67	
			120 MHz	38	53	60	
			90 MHz	30	44	51	
			60 MHz	20	34	41	
			30 MHz	11	24	31	
			25 MHz	8	21	28	
			16 MHz	6	18	25	
			8 MHz	3	16	23	
			4 MHz	2	15	22	
			2 MHz	2	14	21	
		External clock(2), all peripherals disabled	168 MHz	12	27	35	
			144 MHz	9	22	29	
			120 MHz	8	20	28	
			90 MHz	7	19	26	
			60 MHz	5	17	24	
			30 MHz	3	16	23	
			25 MHz	2	15	22	
			16 MHz	2	14	21	
			8 MHz	1	14	21	
			4 MHz	1	13	21	
			2 MHz	1	13	21	

1. Guaranteed by characterization, tested in production at V_{DD} max and f_{HCLK} max with peripherals enabled.
2. External clock is 4 MHz and PLL is on when f_{HCLK} > 25 MHz.
3. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).

Figure 36. PLL output clock waveforms in down spread mode



5.3.12 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 105 °C unless otherwise specified.

The devices are shipped to customers with the Flash memory erased.

Table 39. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current	Write / Erase 8-bit mode, V_{DD} = 1.8 V	-	5	-	mA
		Write / Erase 16-bit mode, V_{DD} = 2.1 V	-	8	-	
		Write / Erase 32-bit mode, V_{DD} = 3.3 V	-	12	-	

Table 40. Flash memory programming

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	Word programming time	Program/erase parallelism (PSIZE) = x 8/16/32	-	16	100(2)	µs
$t_{ERASE16KB}$	Sector (16 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	400	800	ms
		Program/erase parallelism (PSIZE) = x 16	-	300	600	
		Program/erase parallelism (PSIZE) = x 32	-	250	500	
$t_{ERASE64KB}$	Sector (64 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	1200	2400	ms
		Program/erase parallelism (PSIZE) = x 16	-	700	1400	
		Program/erase parallelism (PSIZE) = x 32	-	550	1100	

Table 41. Flash memory programming with V_{PP}

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	Double word programming	T_A = 0 to +40 °C V_{DD} = 3.3 V V_{PP} = 8.5 V	-	16	100(2)	µs
$t_{ERASE16KB}$	Sector (16 KB) erase time		-	230	-	ms
$t_{ERASE64KB}$	Sector (64 KB) erase time		-	490	-	
$t_{ERASE128KB}$	Sector (128 KB) erase time		-	875	-	
t_{ME}	Mass erase time		-	6.9	-	s
V_{prog}	Programming voltage	-	2.7	-	3.6	V
V_{PP}	V_{PP} voltage range	-	7	-	9	V
I_{PP}	Minimum current sunk on the V_{PP} pin	-	10	-	-	mA
t_{VPP}(3)	Cumulative time during which V_{PP} is applied	-	-	-	1	hour

1. Guaranteed by design.
2. The maximum programming time is measured after 100K erase operations.
3. V_{PP} should only be connected during programming/erasing.

Table 42. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value	Unit
			Min(1)	
N_{END}	Endurance	T_A = –40 to +85 °C (6 suffix versions) T_A = –40 to +105 °C (7 suffix versions)	10	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	Years
		1 kcycle(2) at T_A = 105 °C	10	
		10 kcycles(2) at T_A = 55 °C	20	

1. Guaranteed by characterization.
2. Cycling performed over the whole temperature range.

5.3.13 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

Table 53. Characteristics of TIMx connected to the APB2 domain(1)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	AHB/APB2 prescaler distinct from 1, $f_{TIMxCLK}$ = 168 MHz	1	-	$t_{TIMxCLK}$
			5.95	-	ns
		AHB/APB2 prescaler = 1, $f_{TIMxCLK}$ = 84 MHz	1	-	$t_{TIMxCLK}$
			11.9	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	$f_{TIMxCLK}$ = 168 MHz APB2 = 84 MHz	0	$f_{TIMxCLK}/2$	MHz
			0	84	MHz
Res_{TIM}	Timer resolution		-	16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected		1	65536	$t_{TIMxCLK}$
t_{MAX_COUNT}	Maximum possible count		-	32768	$t_{TIMxCLK}$

1. TIMx is used as a general term to refer to the TIM1, TIM8, TIM9, TIM10, and TIM11 timers.

5.3.19 Communications interfaces

I²C interface characteristics

The I²C interface meets the timings requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s.

The I²C timings requirements are guaranteed by design when the I2C peripheral is properly configured (refer to RM0090 reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present. Refer to *Section 5.3.16: I/O port characteristics* for more details on the I²C I/O characteristics.

All I²C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics:

Table 54. I2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50(2)	260(3)	ns

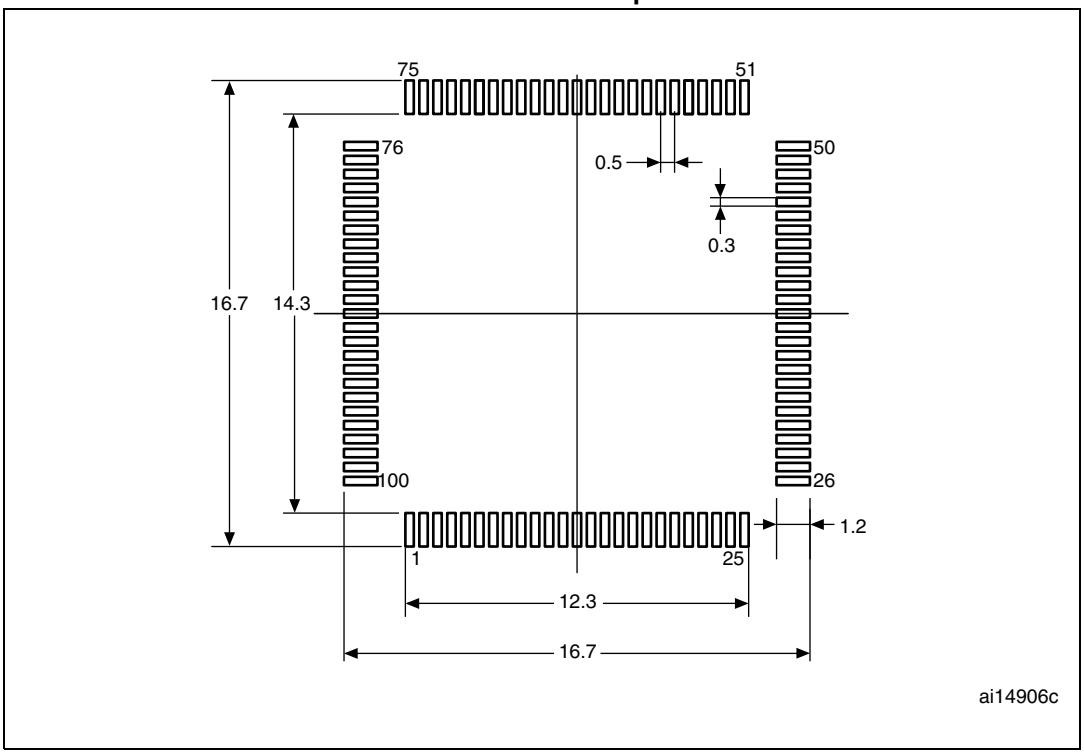
1. Guaranteed by design.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

Table 93. LQPF100 – 100-pin, 14 x 14 mm low-profile quad flat package mechanical data(1) (continued)

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

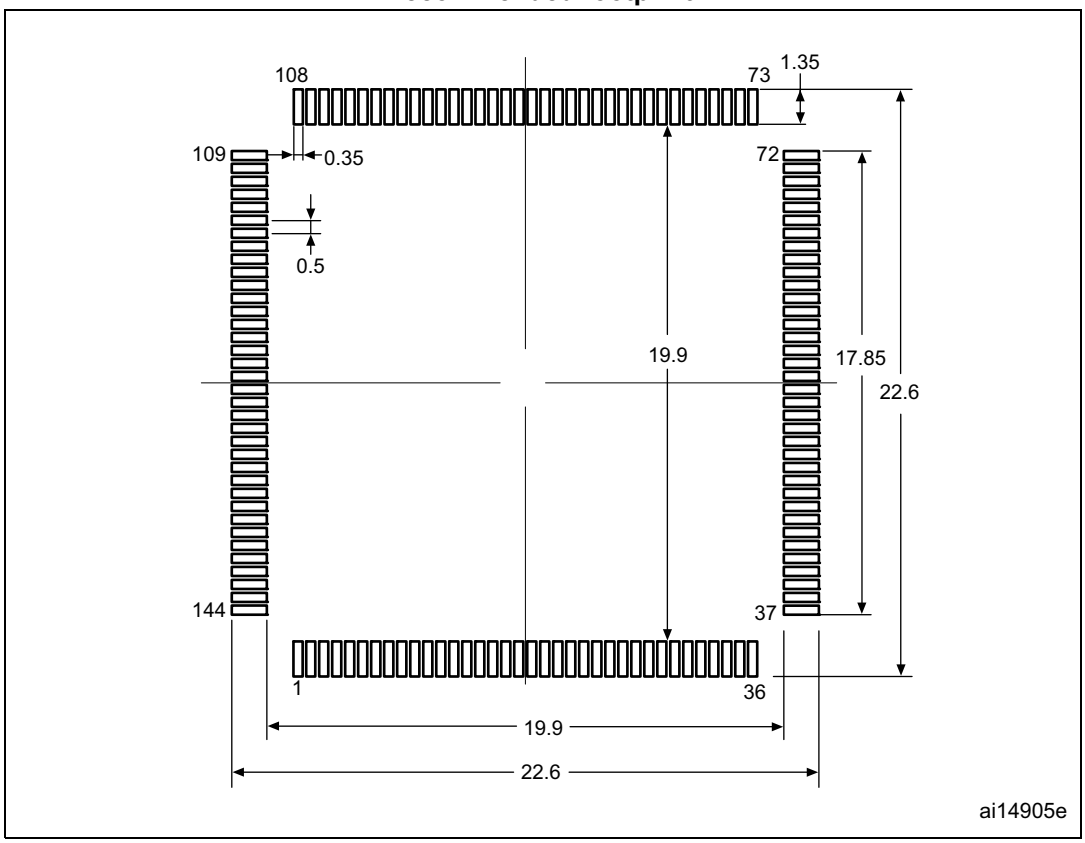
1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 82. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint



1. Dimensions are expressed in millimeters.

Figure 85. LQFP144 - 144-pin,20 x 20 mm low-profile quad flat package recommended footprint



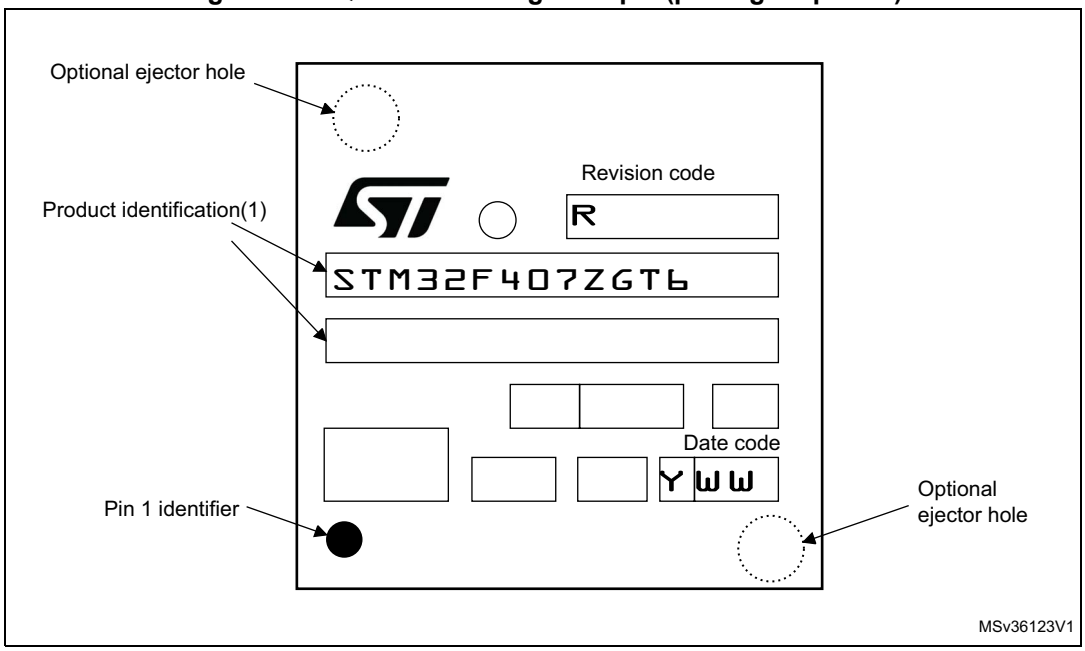
1. Dimensions are in millimeters.

Device marking for LQPF144

The following figure gives an example of topside marking and pin 1 position identifier location.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 86. LQFP144 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

6.7 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

T_J max = T_A max + (P_D max x Θ_{JA})

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$P_{I/O}$ max = Σ (V_{OL} × I_{OL}) + Σ((V_{DD} – V_{OH}) × I_{OH}),

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 98. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP64 - 10 × 10 mm / 0.5 mm pitch	46	°C/W
	Thermal resistance junction-ambient LQFP100 - 14 × 14 mm / 0.5 mm pitch	43	
	Thermal resistance junction-ambient LQFP144 - 20 × 20 mm / 0.5 mm pitch	40	
	Thermal resistance junction-ambient LQFP176 - 24 × 24 mm / 0.5 mm pitch	38	
	Thermal resistance junction-ambient UFBGA176 - 10× 10 mm / 0.65 mm pitch	39	
	Thermal resistance junction-ambient WLCSP90 - 0.400 mm pitch	38.1	

Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.