Microchip Technology - ATSAM4SP32A-ANU-Y Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	I²C, IrDA, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	38
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	160K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	128-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsam4sp32a-anu-y

Table 4-1. **Pin Description List (Continued)**

Pin Number	Pin Name	Functions	Type	Comments

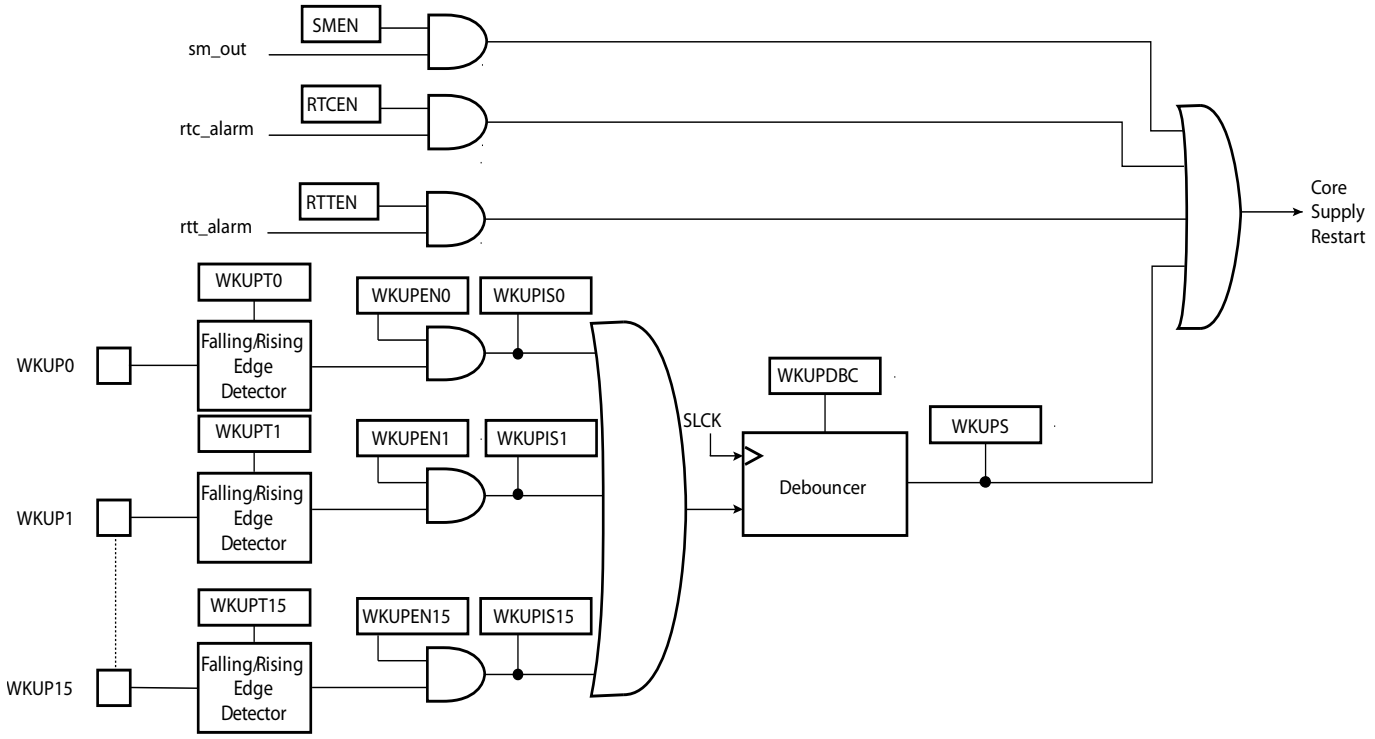
14	PB2	URXD1
		AC6
		WKUP12
			I/O	PIO Controller B Multiplexing (PB2):
				• UART1 Receive Input Data
				• Analog Comparator Input channel 6
				• Wake-up Source 12
				  • Fast start up of the Processor
				  • Active level: Low

15	AINPLC		Input	Direct-analog input voltage
16	PB3	UTXD1 PCK2 AC7	I/O	PIO Controller B Multiplexing (PB3): • UART1 Transmit Output Data • Programmable clock output 2 • Analog Comparator Input channel 7 • See Signal Description for details.
17	AVRL		Input	Analog input low voltage reference
18, 35, 114, 116	VDDIN		P	Voltage Regulator Input, Analog Comparator Power Supply. Voltage range: 3.0V – 3.6 V
19	VDDOUT12		P	Voltage output regulator of 1.2 volts
20	PA17/PGMD5	TD PCK1 PWMH3 AC0	I/O	PIO Controller A Multiplexing (PA17): • Synchronous Serial Controller (SSC) Transmit Output Data • Programmable clock output 1 • PWM Waveform Output High for channel 3 • Analog Comparator Input channel 0 • See Signal Description for details.
21	PC26	TIOA4	I/O	PIO Controller C Multiplexing (PC26): • Tmer/Counter Channel 4 I/O Line A • General purpose I/O
22	PA18/PGMD6	RD PCK2 AC1	I/O	PIO Controller A Multiplexing (PA18): • Synchronous Serial Controller (SSC) Receive Input Data • Programmable clock output 2 • Analog Comparator Input channel 1 • See Signal Description for details.

5.6 Wake-up Sources

The wake-up events allow the device to exit the backup mode. When a wake-up event is detected, the Supply Controller performs a sequence which automatically re-enables the core power supply and the SRAM power supply, if they are not already enabled.

Figure 5-4. Wake-up Sources

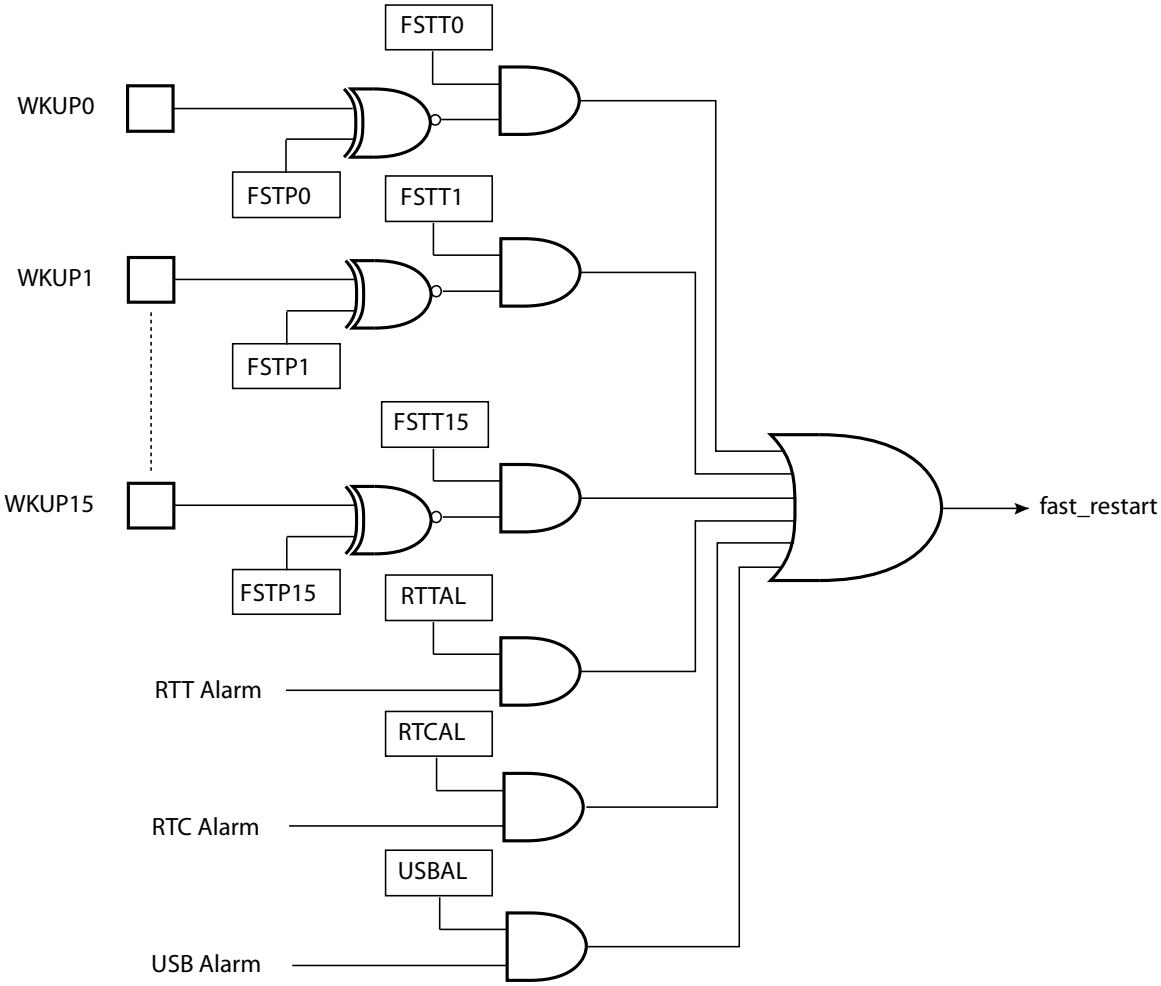


5.7 Fast Startup

The SAM4SP32A allows the processor to restart in a few microseconds while the processor is in wait mode or in sleep mode. A fast start up can occur upon detection of a low level on one of the 19 wake-up inputs (WKUP0 to 15 + SM + RTC + RTT).

The fast restart circuitry, as shown in Figure 5-5, is fully asynchronous and provides a fast start-up signal to the Power Management Controller. As soon as the fast start-up signal is asserted, the PMC automatically restarts the embedded 4/8/12 MHz Fast RC oscillator, switches the master clock on this 4 MHz clock and reenables the processor clock.

Figure 5-5. Fast Start-Up Sources



The Slow Clock generator is based on a 32 kHz crystal oscillator and an embedded 32 kHz RC oscillator. The Slow Clock defaults to the RC oscillator, but the software can enable the crystal oscillator and select it as the Slow Clock source.

The Supply Controller starts up the device by sequentially enabling the internal power switches and the Voltage Regulator, then it generates the proper reset signals to the core power supply.

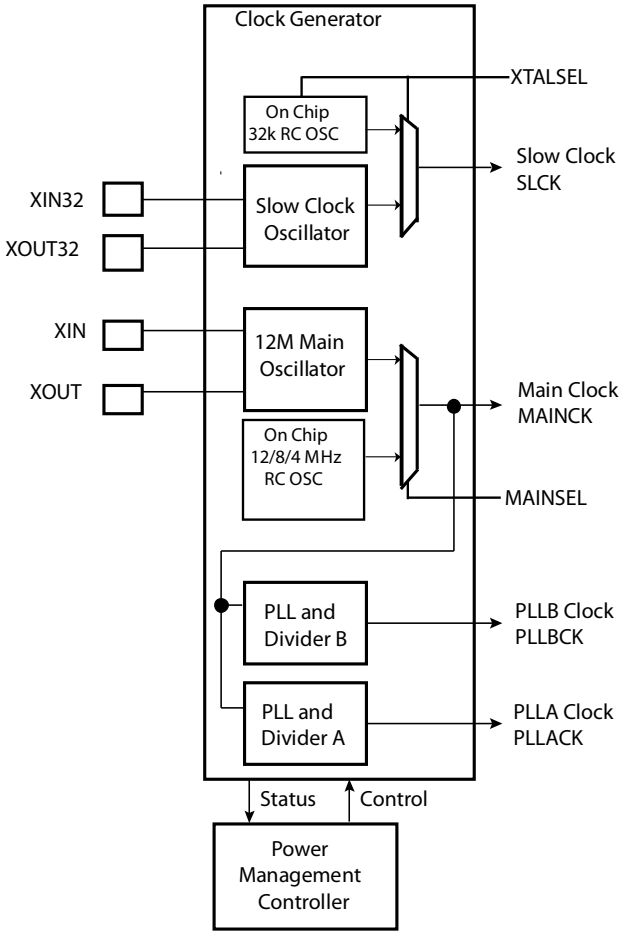
It also enables to set the system in different low-power modes and to wake it up from a wide range of events.

10.5 Clock Generator

The Clock Generator is made up of:

- One Low-power 32768Hz Slow Clock Oscillator with bypass mode
- One Low-power RC Oscillator
- One 3-20 MHz Crystal Oscillator, which can be bypassed
- One Fast RC Oscillator, factory programmed. Three output frequencies can be selected: 4, 8 or 12 MHz. By default 4 MHz is selected.
- One 80 to 240 MHz PLL (PLLB) providing a clock for the USB Full Speed Controller
- One 80 to 240 MHz programmable PLL (PLLA), provides the clock, MCK to the processor and peripherals. The PLLA input frequency is from 3 MHz to 32 MHz.

Figure 10-2. Clock Generator Block Diagram



- Programmable center or left aligned output waveform
- Independent Output Override for each channel
- Independent complementary Outputs with 12-bit dead time generator for each channel
- Independent Enable Disable Commands
- Independent Clock Selection
- Independent Period and Duty Cycle, with Double Buffering

- Synchronous Channel mode
  - Synchronous Channels share the same counter
  - Mode to update the synchronous channels registers after a programmable number of periods
- Connection to one PDC channel
  - Provides Buffer transfer without processor intervention, to update duty cycle of synchronous channels
- One programmable Fault Input providing an asynchronous protection of outputs
- Stepper motor control (2 Channels)

11.7 USB Device Port (UDP)

- USB V2.0 full-speed compliant,12 Mbits per second.
- Embedded USB V2.0 full-speed transceiver
- Embedded 2688-byte dual-port RAM for endpoints
- Eight endpoints
  - Endpoint 0: 64bytes
  - Endpoint 1 and 2: 64 bytes ping-pong
  - Endpoint 3: 64 bytes
  - Endpoint 4 and 5: 512 bytes ping-pong
  - Endpoint 6 and 7: 64 bytes ping-pong
  - Ping-pong Mode (two memory banks) for Isochronous and bulk endpoints
- Suspend/resume logic
- Integrated Pull-up on DDP
- Pull-down resistor on DDM and DDP when disabled

11.8 Analog Comparator

- One analog comparator
- High speed option vs. low-power option
  - 170 µA/xx ns active current consumption/propagation delay
  - 20 µA/xx ns active current consumption/propagation delay
- Selectable input hysteresis
  - 0, 15 mV, 30mV (Typ)
- Minus input selection:
  - Temperature Sensor
  - ADVREF
- Plus input selection:
  - All analog inputs
- output selection:
  - Internal signal

Table 12-3 shows the modulation and coding scheme and the size of the header portion of the PHY frame

Table 12-3. **Header parameters**

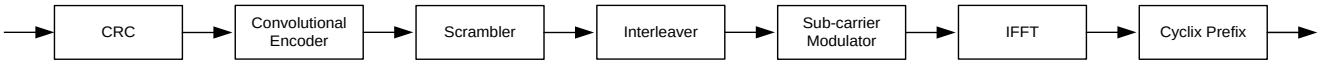
	DBPSK
Convolutional Code (1/2)	On
Information bits per subcarrier	0,5
Information bits per OFDM symbol	42

All the parameters of the physical layer such as the base band clock, subcarrier spacing, number of subcarriers...; are defined in PRIME Specification, and have to be identical in a network in order to achieve compatibility.

12.1.3 PHY Protocal Data Unit (PPDU) Format

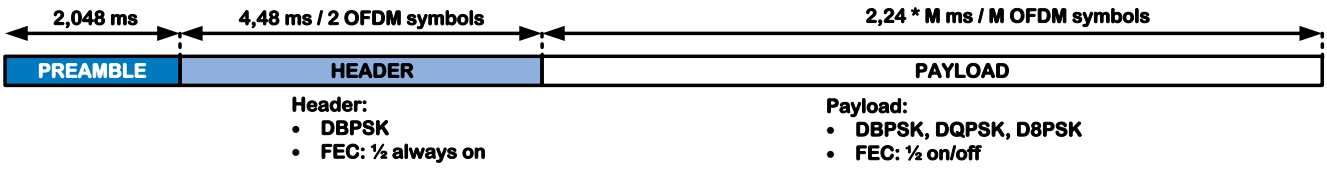
Figure 12-6 shows how OFDM symbols are transmitted in a PPDU (Physical layer Protocol Data Unit). The preamble is used at the beginning of every PPDU for synchronization purposes.

Figure 12-6. PHY layer transmitter block diagram



Phy layer adaptively modifies attenuation values applied to the whole signal. Also, additional attenuations are applied to the chirp section of the signal (preamble) and to the rest of the signal itself (header+payload), to smoothly adapt amplitude values and transitions.

Figure 12-7. PPDU OFDM symbols and duration



12.1.4 PHY Service Specification

There is an interface specified in PRIME for the PHY layer, with several primitives relative to both data and control planes.

PHY layer has a single 20-bit free-running clock measured in 10µs steps. Time measured by this clock is the one to be used in some PHY primitives to indicate a specific instant in time.

SAM4SP32A includes a hardware implementation of this clock, which consists of a 20-bit register. This register is read-only and it can be accessed as a 32-bit variable by the ADD8051C3A microcontroller.

12.1.5.20 EVM_PAYLOAD_ACUM Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
EVM_PAYLOAD_ACUM	EVM_PAYLOAD_ACUM(19:12)								@0xFE43
	EVM_PAYLOAD_ACUM(11:4)								@0xFE44
	EVM_PAYLOAD_ACUM(3:0)				“0000”				@0xFE45
	“00000000”								@0xFE46

Name: EVM_PAYLOAD_ACUM

Address: 0xFE43 – 0xFE46

Access: Read only

Reset: 0x00, …, 0x00;

- **EVM_PAYLOAD_ACUM:** Payload Total Error Vector Magnitude Accumulator

  When receiving an OFDM symbol, the summation of all its individual carriers EVMs is calculated in order to further calculate the average EVM value. These registers store the maximum summation between all the OFDM symbols received in a message payload.

12.1.5.21 RMS_CALC Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
RMS_CALC	RMS_CALC(7:0)							

Name: RMS_CALC

Address: 0xFE58

Access: Read only

Reset: 0x00

- **RMS_CALC:** This register stores an 8-bit value which magnitude is proportional to the emitted signal amplitude.

  By measuring the amplitude of the emitted signal, the hardware can estimate the power line input impedance. Thus hardware can adjust emission configuration appropriately.

12.1.5.37 EMIT_CONFIG Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
EMIT_CONFIG	--						TR_EMIT	TWO_H_BRIDGES

Name: EMIT_CONFIG

Address: 0xFE8F

Access: Read/write

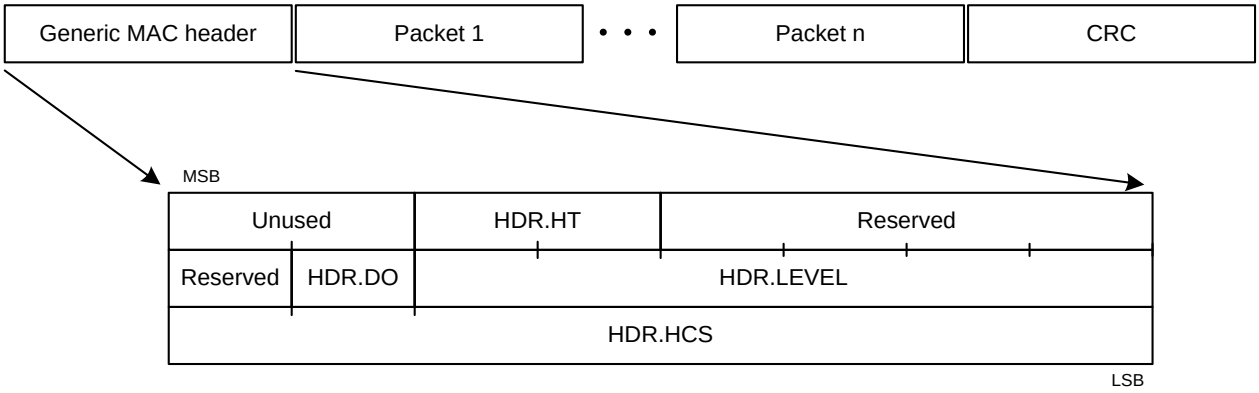
Reset: 0x03

- **TR_EMIT:** Emission mode
  This bit selects the emission mode (Internal Drive or External transistors bridge).
  - '0': Emission is done by means of internal SAM4SP32A driver.
  - '1': Emission is done by means of external transistors (Default).
- **TWO_H_BRIDGES:** This bit selects the number of semi-H-bridges in the external interface.
  - '0': There is only one semi-H-bridge in the external interface.
  - '1': There are two semi-H-bridges in the external interface and the field HIMP (AFE_CTL register) determines which one is active (Default).

  Semi-H-Bridges must be connected following the table below

	TWO_H_BRIDGES='0'	TWO_H_BRIDGES='1'
EMIT1	P	N1
EMIT2	P	N1
EMIT3	P	N1
EMIT4	N	P2
EMIT5	N	P2
EMIT6	N	P2

Figure 12-10. Generic MAC PDU format and generic MAC header detail



In transmission all CRC bytes are real-time calculated and the last bytes of the MAC PDU are overwritten with these values, (provided that the field HT in the first byte of the MAC header in transmission data is equal to the corresponding MAC PDU type).

In reception the CRC bytes are also real-time calculated and these bytes are checked with the last bytes of the MAC PDU. If the CRC is not correct, then an error flag is activated, the complete frame is discarded, and the corresponding error counter is increased. These counters allow the MAC layer to take decisions according to error ratio.

For the Generic MAC PDU, there is an 8-bit CRC in the Generic MAC header, which corresponds to PRIME HDR.HCS. In reception if this CRC doesn't check successfully, the current frame is discarded and no interruption is generated.

This works in the same way as CRC for the PHY layer (CRC Ctrl, located in the PHY header, see PRIME specification for further information).

There is another CRC for the Generic MAC PDU which is the last field of the GPDU. It is 32 bits long and it is used to detect transmission errors. The CRC shall cover the concatenation of the SNA with the GPDU except for the CRC field itself. In reception, if the CRC is not successful then an internal flag is set and the error counter is increased.

For the Promotion Needed PDU there is an 8-bit CRC, calculated with the first 13 bytes of the header. In reception, if this CRC is not correct, then an internal flag is set and the corresponding error counter is increased.

For the Beacon PDU there is a 32-bit CRC calculated with the same algorithm as the one defined for the CRC of the Generic MAC PDU. This CRC shall be calculated over the complete BPDU except for the CRC field itself. In reception, if this CRC is not successful, then an internal flag is set and the same error counter as for GPDU is increased. The hardware used for this CRC is the same as the one used for GPDU.

12.2.3.3 VITERBI_BER_SOFT Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
VITERBI_BER_SOFT	VITERBI_BER_SOFT(7:0)							

Name: VITERBI_BER_SOFT

Address: 0xFE37

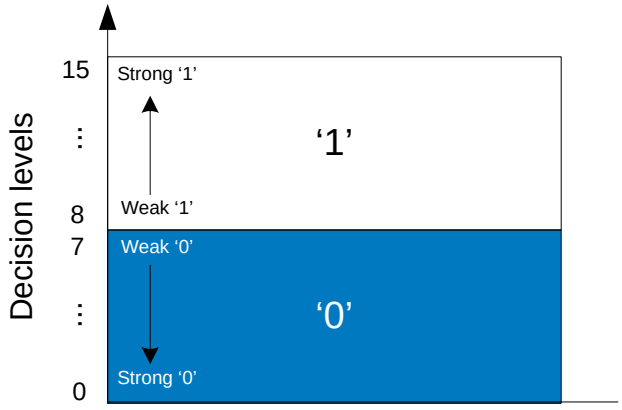
Access: Read only

Reset: 0x00

- **VITERBI_BER_SOFT:** This register stores a value proportional to the number of errors accumulated in a message reception using Viterbi soft* decision. The value is cleared by hardware each time a new message is received.

**Soft Decision: in "soft" decision there are fifteen decision levels. A strong '0' is represented by a value of "0", while a strong '1' is represented by a value of "15". The rest of values are intermediate, so "7" is used to represent a weak '0' and "8" represents a weak '1'. Soft decision calculates the error in one bit received as the distance in decision levels between the value received (a value in the range 0 to 15) and the corrected one (0 or 15).*

Figure 12-13. Viterbi Hard detection decision levels



12.2.3.5 ERR_CRC8_MAC Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
ERR_CRC8_MAC	ERR_CRC8_MAC(15:8)								@0xFEBC
	ERR_CRC8_MAC(7:0)								@0xFEBD

Name: ERR_CRC8_MAC

Address: 0xFEBC – 0xFEBD

Access: Read/write

Reset: 0x00, 0x00

- **ERR_CRC8_MAC:** 16-bit value that stores the number of received messages that have been discarded by an error in the payload MAC layer CRC8.

  Note: to clear this value, these registers must be reset by the SAM4SP32A microcontroller.

12.2.3.10 FALSE_DET Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
FALSE_DET	FALSE_DET(15:8)								@0xFEC5
	FALSE_DET(7:0)								@0xFEC6

Name: FALSE_DET

Address: 0xFEC5 – 0xFEC6

Access: Read/write

Reset: 0x00, 0x00

- **FALSE_DET:** Erroneous non-discarded messages.

  16-bit value that stores the number of received messages that have not been discarded since its PHY layer CRC8 is correct, but in which there are other incorrect fields. The fields that shall be taken into account to increase the counter in case they were wrong can be selected by FALSE_DET_CONFIG register.

  Note: to clear this value, these registers must be reset by the SAM4SP32A microcontroller

12.2.3.12 MAX_LEN_DBPSK_VTB Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0
MAX_LEN_DBPSK_VTB	--		MAX_LEN_DBPSK_VTB(5:0)					

Name: MAX_LEN_DBPSK_VTB

Address: 0xFEC9

Access: Read/write

Reset: 0xFF

- **--:** Reserved bits
- **MAX_LEN_DBPSK_VTB:** This register sets the maximum length, measured in OFDM symbols that the system allows to receive when working with DBPSK modulation and Viterbi encoding.

  If a message in such modulation/encoding is received and its LEN field indicates a length above the threshold defined by MAX_LEN_DBPSK_VTB value, the message will be discarded.

12.2.3.19 AES_DATA_OUT Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	B it 0	
AES_DATA_OUT	AES_DATA_OUT(127:120)								@FFB0
	…							…	
	AES_DATA_OUT(7: 0)								@FFBF

Name: AES_DATA_OUT

Address: 0xFFB0 – 0xFFBF

Access: Read only

Reset: 0x00, …, 0x00

- **AES_DATA_OUT:** Output buffer for AES128 block.

  This buffer stores the result of the encryption/decryption processing of data in AES_DATA_IN (see 12.2.3.18) register with the key in KEY_PERIPH (see 12.2.3.20) register.

Figure 13-1. Core Brownout Output Waveform

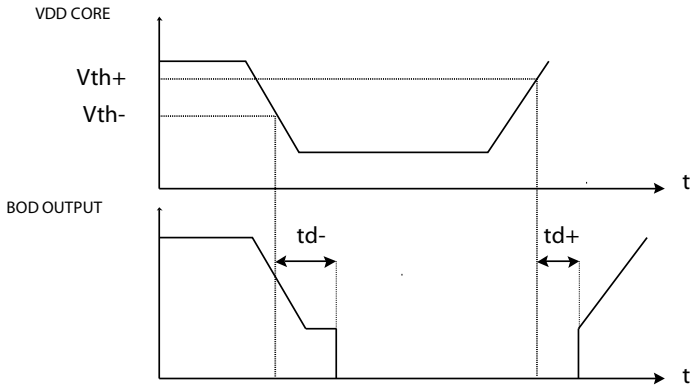


Table 13-5. **VDDIO Supply Monitor**

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Monitor Threshold	V_{TH}	16 selectable steps	1.6		3.34	V
Threshold Level Accuracy	$T_{ACCURACY}$	[-40/+85°C]	-2.5		+2.5	%
Hysteresis	V_{HYST}			20	30	mV
Current Consumption on VDDCOARE	I_{DDON}	Enabled			40	µA
	I_{DDOFF}	Disable			10	
Start Time	T_{START}	From disable state to enable state			320	µs

13.4 Oscillator Characteristics

13.4.1 32 kHz RC Oscillator Characteristics

Table 13-16. **32 kHz RC Oscillator Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	RC Oscillator Frequency		20	32	44	kHz
	Frequency Supply Dependency		-3		3	%/V
	Frequency Temperature Dependency	Over temperature range (-40°C/ +85°C) versus 25°C	-7		7	%
Duty	Duty Cycle		45	50	55	%
T_{ON}	Startup Time				100	µs
I_{DDON}	Current Consumption	After Startup Time Temp. Range = -40°C to +125°C Typical Consumption at 2.2V supply and Temp = 25°C		540	860	nA

Figure 13-14. SSC Receiver RK and RF as input

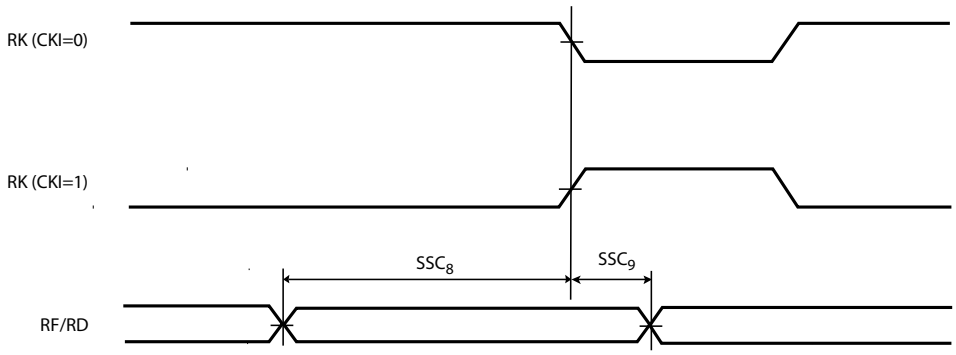


Figure 13-15. SSC Receiver, RK as input and RF as output

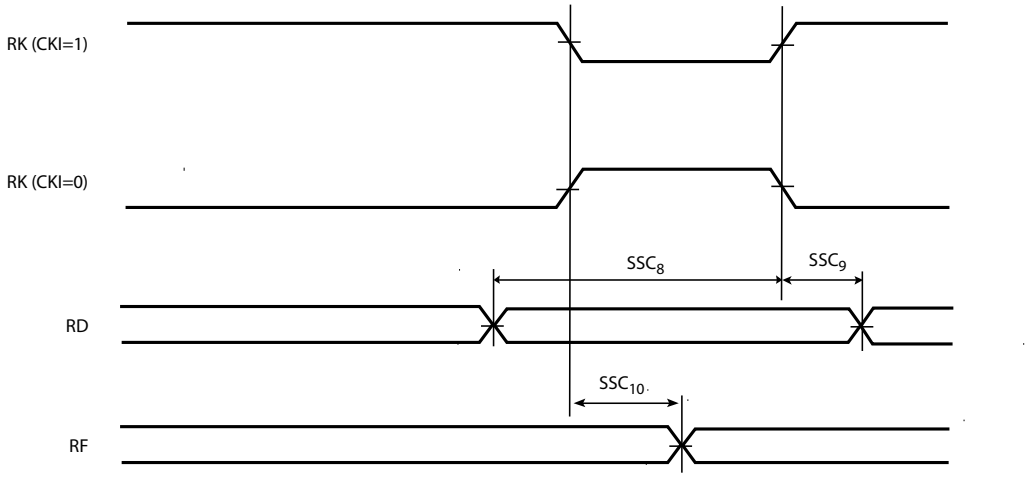
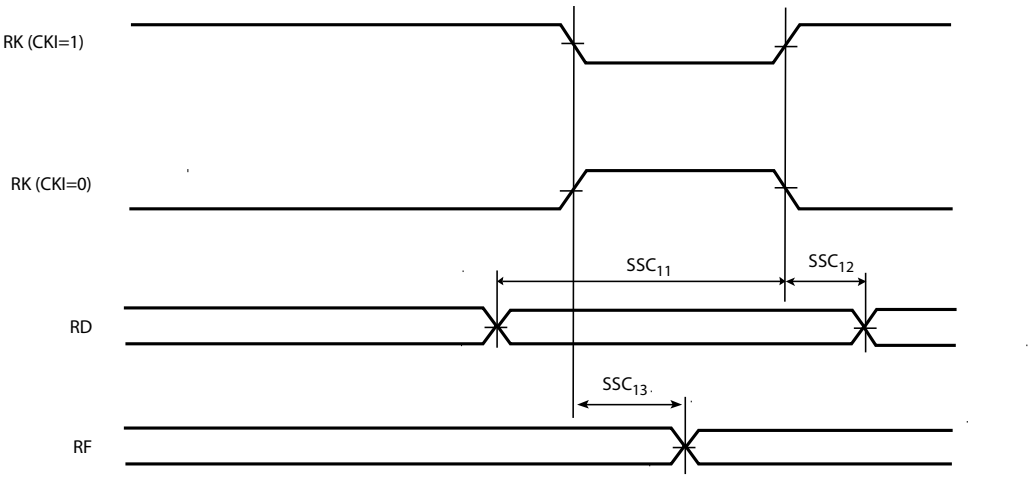


Figure 13-16. SSC Receiver, RK and RF as output



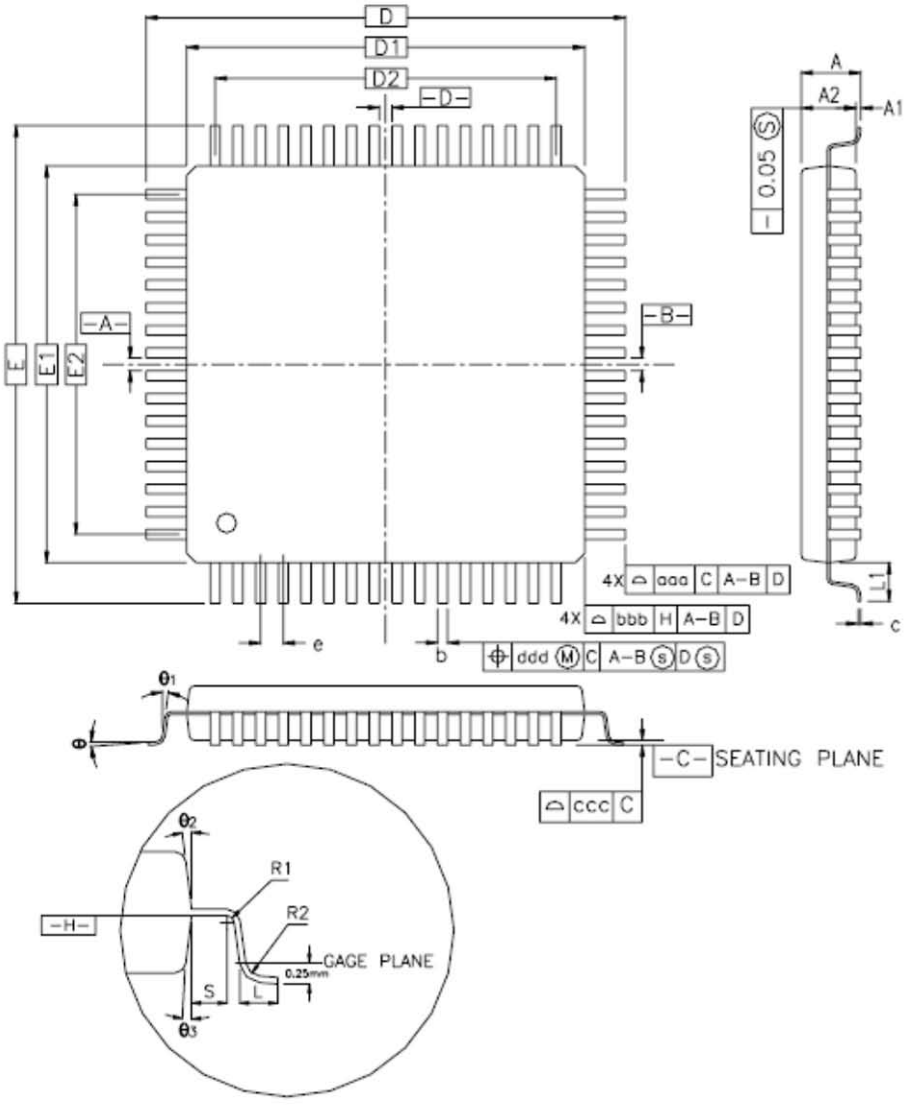
13.9.5.2 USART SPI TImings

Table 13-34. **USART SPI TImings**

Symbol	Parameter	Conditions	Min	Max	Units
Master Mode					
SPI_0	SCK Period	1.8v domain 3.3v domain	MCK/6		ns
SPI_1	Input Data Setup Time	1.8v domain 3.3v domain	0.5 * MCK + 0.8 0.5 * MCK + 1.0		ns
SPI_2	Input Data Hold Time	1.8v domain 3.3v domain	1.5 * MCK + 0.3 1.5 * MCK + 0.1		ns
SPI_3	Chip Select Active to Serial Clock	1.8v domain 3.3v domain	1.5 * SPCK - 1.5 1.5 * SPCK - 2.1		ns
SPI_4	Output Data Setup Time	1.8v domain 3.3v domain	- 7.9 - 7.2	9.9 10.7	ns
SPI_5	Serial Clock to Chip Select Inactive	1.8v domain 3.3v domain	1 * SPCK - 4.1 1 * SPCK - 4.8		ns
Slave Mode					
SPI_6	SCK falling to MISO	1.8V domain 3.3V domain	4.7 4	17.3 15.2	ns
SPI_7	MOSI Setup time before SCK rises	1.8V domain 3.3V domain	2 * MCK + 0.7 2 * MCK		ns
SPI_8	MOSI Hold time after SCK rises	1.8v domain 3.3v domain	0 0.1		ns
SPI_9	SCK rising to MISO	1.8v domain 3.3v domain	4.7 4.1	17.1 15.5	ns
SPI_{10}	MOSI Setup time before SCK falls	1.8v domain 3.3v domain	2 * MCK + 0.7 2 * MCK + 0.6		ns
SPI_{11}	MOSI Hold time after SCK falls	1.8v domain 3.3v domain	0.2 0.1		ns

14. Mechanical Characteristics

Figure 14-1. 128-lead LQFP Package Mechanical Drawing



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	16.00 BSC.			0.630 BSC.		
D1	14.00 BSC.			0.551 BSC.		
E	16.00 BSC.			0.630 BSC.		
E1	14.00 BSC.			0.551 BSC.		
R2	0.08	—	0.20	0.003	—	0.008
R1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BSC.			0.016 BSC.		
D2	12.40			0.488		
E2	12.40			0.488		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.07			0.003		

Note : 1. This drawing is for general information only. Refer to JEDEC Drawing MS-026 for additional information.