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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	Host Interface, Serial Port
Clock Rate	33MHz
Non-Volatile Memory	External
On-Chip RAM	10kB
Voltage - I/O	5.00V
Voltage - Core	5.00V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	128-BQFP
Supplier Device Package	128-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-2171bsz-133

Development System

The ADSP-2100 Family Development Software, a complete set of tools for software and hardware system development, supports the ADSP-217x. The System Builder provides a high-level method for defining the architecture of systems under development. The Assembler has an algebraic syntax that is easy to program and debug. The Linker combines object files into an executable file. The Simulator provides an interactive instruction-level simulation with a reconfigurable user interface to display different portions of the hardware environment. A PROM Splitter generates PROM programmer compatible files. The C Compiler, based on the Free Software Foundation's GNU C Compiler, generates ADSP-217x assembly source code. The Runtime Library includes over 100 ANSI-standard mathematical and DSP-specific functions.

EZ-Tools, low cost, easy-to-use hardware tools, also support the ADSP-217x.

The ADSP-217x EZ-ICE® Emulator aids in the hardware debugging of ADSP-217x systems. The emulator consists of hardware, host computer resident software, the emulator probe, and the pin adaptor. The emulator performs a full range of emulation functions including stand-alone operation or operation in the target, setting up to 20 breakpoints, single-step or full-speed operation in the target, examining and altering registers and memory values, and PC upload/download functions. If you plan to use the emulator, you should consider the emulator's restrictions (differences between emulator and processor operation).

The EZ-LAB® Evaluation Board is a PC plug-in card, but it can operate in stand-alone mode. The evaluation board/system development board executes EPROM-based or downloaded programs. Modular Analog Front End daughter cards with different codecs will be made available.

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Additional Information

This data sheet provides a general overview of ADSP-217x functionality. For additional information on the architecture and instruction set of the processor, refer to the *ADSP-2100 Family User's Manual*. For more information about the Development System and ADSP-217x programmer's reference information, refer to the *ADSP-2100 Family Assembler Tools & Simulator Manual*.

ARCHITECTURE OVERVIEW

Figure 1 is an overall block diagram of the ADSP-217x. The processor contains three independent computational units: the ALU, the multiplier/accumulator (MAC) and the shifter. The computational units process 16-bit data directly and have provisions to support multiprecision computations. The ALU performs a standard set of arithmetic and logic operations; division primitives are also supported. The MAC performs single-cycle multiply, multiply/add and multiply/subtract operations with 40 bits of accumulation. The shifter performs logical and arithmetic shifts, normalization, denormalization, and derive exponent operations. The shifter can be used to efficiently implement numeric format control including multiword and block floating-point representations.

The internal result (R) bus directly connects the computational units so that the output of any unit may be the input of any unit on the next cycle.

A powerful program sequencer and two dedicated data address generators ensure efficient delivery of operands to these computational units. The sequencer supports conditional jumps, subroutine calls and returns in a single cycle. With internal loop counters and loop stacks, the ADSP-217x executes looped code with zero overhead; no explicit jump instructions are required to maintain the loop.

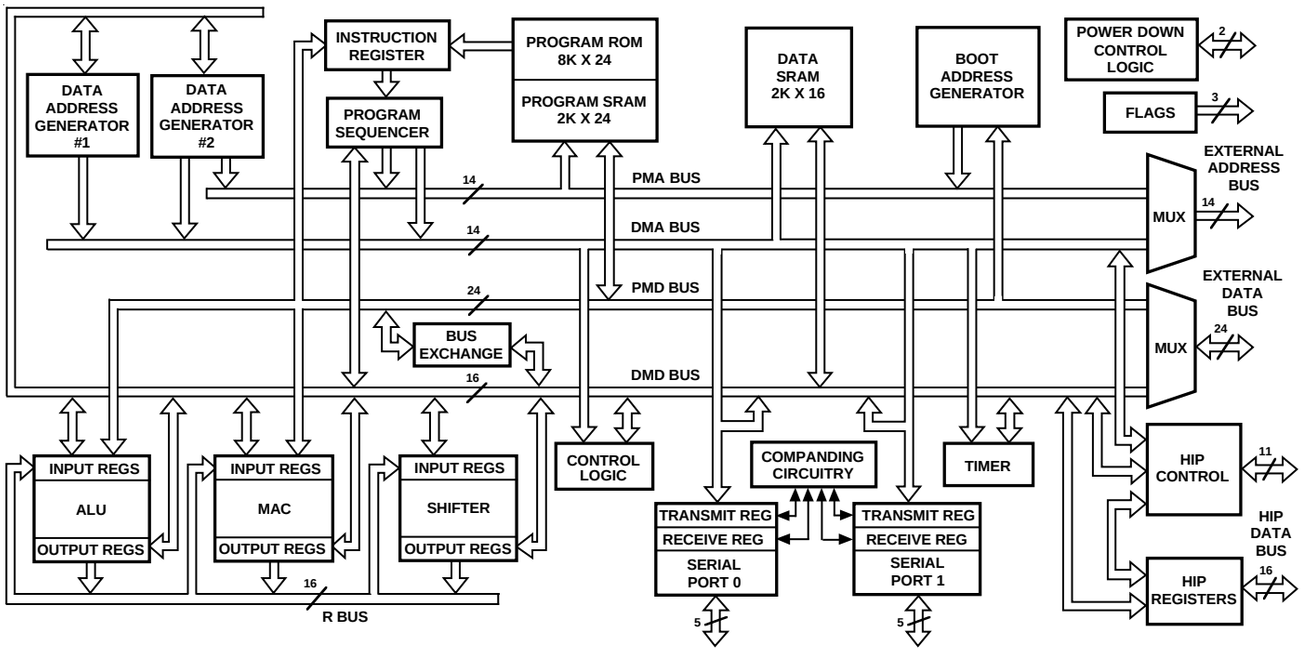


Figure 1. ADSP-217x Block Diagram

Two data address generators (DAGs) provide addresses for simultaneous dual operand fetches (from data memory and program memory). Each DAG maintains and updates four address pointers. Whenever the pointer is used to access data (indirect addressing), it is post-modified by the value of one of four possible modify registers. A length value may be associated with each pointer to implement automatic modulo addressing for circular buffers.

Efficient data transfer is achieved with the use of five internal buses.

- Program Memory Address (PMA) Bus
- Program Memory Data (PMD) Bus
- Data Memory Address (DMA) Bus
- Data Memory Data (DMD) Bus
- Result (R) Bus

The two address buses (PMA and DMA) share a single external address bus, allowing memory to be expanded off-chip, and the two data buses (PMD and DMD) share a single external data bus.

Program memory can store both instructions and data, permitting the ADSP-217x to fetch two operands in a single cycle, one from program memory and one from data memory. The ADSP-217x can fetch an operand from on-chip program memory and the next instruction in the same cycle.

The memory interface supports slow memories and memory-mapped peripherals with programmable wait state generation. External devices can gain control of external buses with bus request/grant signals ($\overline{BR}$ and $\overline{BG}$). One execution mode (Go Mode) allows the ADSP-217x to continue running from internal memory. Normal execution mode requires the processor to halt while buses are granted.

In addition to the address and data bus for external memory connection, the ADSP-217x has a configurable 8- or 16-bit Host Interface Port (HIP) for easy connection to a host processor. The HIP is made up of 16 data/address pins and 11 control pins. The HIP is extremely flexible and provides a simple interface to a variety of host processors. For example, the Motorola 68000 series, the Intel 80C51 series and the Analog Devices' ADSP-2101 can be easily connected to the HIP. The host processor can initialize the ASDP-217x's on-chip memory through the HIP.

The ADSP-217x can respond to eleven interrupts. There can be up to three external interrupts, configured as edge or level sensitive, and eight internal interrupts generated by the Timer, the Serial Ports ("SPORTs"), the HIP, the powerdown circuitry, and software. There is also a master RESET signal.

The two serial ports provide a complete synchronous serial interface with optional companding in hardware and a wide variety of framed or frameless data transmit and receive modes of operation. Each port can generate an internal programmable serial clock or accept an external serial clock.

Boot circuitry provides for loading on-chip program memory automatically from byte-wide external memory. After reset, seven wait states are automatically generated. This allows, for example, a 30 ns ADSP-217x to use an external 200 ns EPROM as boot memory. Multiple programs can be selected and loaded from the EPROM with no additional hardware. The on-chip program memory can also be initialized through the HIP.

The ADSP-217x features three general-purpose flag outputs whose states can be simultaneously changed through software. You can use these outputs to signal an event to an external device. In addition, the data input and output pins on SPORT1 can be alternatively configured as an input flag and an output flag.

A programmable interval timer generates periodic interrupts. A 16-bit count register (TCOUNT) is decremented every *n* processor cycles, where *n-l* is a scaling value stored in an 8-bit register (TSCALE). When the value of the count register reaches zero, an interrupt is generated and the count register is reloaded from a 16-bit period register (TPERIOD).

The ADSP-217x instruction set provides flexible data moves and multifunction (one or two data moves with a computation) instructions. Every instruction can be executed in a single processor cycle. The ADSP-217x assembly language uses an algebraic syntax for ease of coding and readability. A comprehensive set of development tools supports program development.

Serial Ports

The ADSP-217x incorporates two complete synchronous serial ports (SPORT0 and SPORT1) for serial communications and multiprocessor communication.

Here is a brief list of the capabilities of the ADSP-217x SPORTs. Refer to the *ADSP-2100 Family User's Manual* for further details.

- SPORTs are bidirectional and have a separate, double-buffered transmit and receive section.
- SPORTs can use an external serial clock or generate their own serial clock internally.
- SPORTs have independent framing for the receive and transmit sections. Sections run in a frameless mode or with frame synchronization signals internally or externally generated. Frame sync signals are active high or inverted, with either of two pulse widths and timings.
- SPORTs support serial data word lengths from 3 to 16 bits and provide optional A-law and μ-law companding according to CCITT recommendation G.711.
- SPORT receive and transmit sections can generate unique interrupts on completing a data word transfer.
- SPORTs can receive and transmit an entire circular buffer of data with only one overhead cycle per data word. An interrupt is generated after a data buffer transfer.
- SPORT0 has a multichannel interface to selectively receive and transmit a 24 or 32 word, time-division multiplexed, serial bitstream.
- SPORT1 can be configured to have two external interrupts (IRQ0 and IRQ1) and the Flag In and Flag Out signals. The internally generated serial clock may still be used in this configuration.

Pin Description

The ADSP-217x is available in 128-lead TQFP and 128-lead PQFP packages. Table I contains the pin descriptions.

Table I. ADSP-217x Pin List

Pin Group Name	# of Pins	Input/ Output	Function
Address	14	O	Address output for program, data and boot memory spaces
Data	24	I/O	Data I/O pins for program and data memories. Input only for boot memory space, with two MSBs used as boot space addresses.
$\overline{\text{RESET}}$	1	I	Processor reset input
$\overline{\text{IRQ2}}$	1	I	External interrupt request #2
$\overline{\text{BR}}$	1	I	External bus request input
$\overline{\text{BG}}$	1	O	External bus grant output
$\overline{\text{BGH}}$	1	O	External bus grant hang output
$\overline{\text{PMS}}$	1	O	External program memory select
$\overline{\text{DMS}}$	1	O	External data memory select
$\overline{\text{BMS}}$	1	O	Boot memory select
$\overline{\text{RD}}$	1	O	External memory read enable
$\overline{\text{WR}}$	1	O	External memory write enable
MMAP	1	I	Memory map select
CLKIN, XTAL	2	I	External clock or quartz crystal input
CLKOUT	1	O	Processor clock output
$\overline{\text{HSEL}}$	1	I	HIP select input
$\overline{\text{HACK}}$	1	O	HIP acknowledge output
HSIZE	1		8/16 bit host select input 0 = 16-bit; 1 = 8-bit
BMODE	1	I	Boot mode select input 0 = EPROM/data bus; 1 = HIP
HMD0	1	I	Bus strobe select input 0 = RD, WR; 1 = RW, DS
HMD1	1	I	HIP address/data mode select input 0 = separate; 1 = multiplexed
$\overline{\text{HRD}}$/HRW	1	I	HIP read strobe/read/write select input
$\overline{\text{HWR}}$/$\overline{\text{HDS}}$	1	I	HIP write strobe/host data strobe select input
HD15–0/ HAD15-0	16	I/O	HIP data/data and address
HA2/ALE	1	I	Host address 2/Address latch enable input
HA1–0/ Unused	2	I	Host addresses 1 and 0 inputs
SPORT0	5	I/O	Serial port 0 I/O pins (TFS0, RFS0, DT0, DR0, SCLK0)
SPORT1 or $\overline{\text{IRQ1}}$ (TFS1)	5	I/O	Serial port 1 I/O pins
$\overline{\text{IRQ1}}$ (TFS1)	1	I	External interrupt request #1
$\overline{\text{IRQ0}}$ (RFS1)	1	I	External interrupt request #0
SCLK1	1	O	Programmable clock output
FO (DT1)	1	O	Flag Output pin
FI (DR1)	1	I	Flag Input pin
FL2–0	3	O	General purpose flag output pins
V_{DD}	6		Power supply pins
GND	11		Ground pins
$\overline{\text{PWD}}$	1	I	Powerdown pin
PWDACK	1	O	Powerdown acknowledge pin

Host Interface Port

The ADSP-217x host interface port is a parallel I/O port that allows for an easy connection to a host processor. Through the HIP, the ADSP-217x can be used as a memory-mapped peripheral to a host computer. The HIP can be thought of as an area of dual-ported memory, or mailbox registers, that allow communication between the computational core of the ADSP-217x and the host computer.

The HIP is completely asynchronous. The host processor can write data into the HIP while the ADSP-217x is operating at full speed.

The HIP can be configured with the following pins:

- HSIZE configures HIP for 8-bit or 16-bit communication with the host processor.
- BMODE (when MMAP = 0) determines whether the ADSP-217x boots from the host processor (through the HIP) or external EPROM (through the data bus).
- HMD0 configures the bus strobes as separate read and write strobes, or a single read/write select and a host data strobe.
- HMD1 selects separate address (3-bit) and data (16-bit) buses, or a multiplexed, 16-bit address/data bus with address latch enable.

Tying these pins to appropriate values configures the ADSP-217x for straight-wire interface to a variety of industry-standard microprocessors and microcomputers.

In 8-bit reads, the ADSP-217x three-states the upper eight bits of the bus. When the host processor writes an 8-bit value to the HIP, the upper eight bits are all zeros. For additional information refer to the *ADSP-2100 Family User's Manual.*

HIP Operation

The HIP contains six data registers (HDR5–0) and two status registers (HSR7–6) with an associated HMASK register for masking interrupts from individual HIP data registers. All HIP data registers are memory-mapped into the internal data memory of the ADSP-217x. HIP transfers can be managed using either interrupts or a polling scheme. These registers are shown in the section "ADSP-217x Registers."

The HIP allows a software reset to be performed by the host processor. The internal software reset signal is asserted for five ADSP-217x processor cycles.

LOW POWER OPERATION

The ADSP-217x has three low power modes that significantly reduce the power dissipation when the device operates under standby conditions. These modes are:

- Powerdown
- Idle
- Slow Idle

The CLKOUT pin may also be disabled to reduce external power dissipation. The CLKOUT pin is controlled by Bit 14 of SPORT0 Autobuffer Control Register, DM[0x3FF3].

Powerdown

The ADSP-217x processor has a low power feature that lets the processor enter a very low power dormant state through hardware or software control. Here is a brief list of powerdown features. Refer to the *ADSP-2100 Family User's Manual*, Chapter 9 "System Interface" for detailed information about the powerdown feature.

- Powerdown mode holds the processor in CMOS standby with a maximum current of less than 100 µA in some modes.
- Quick recovery from powerdown. The processor begins executing instructions in as few as 100 CLKIN cycles.
- Support for an externally generated TTL or CMOS processor clock. The external clock can continue running during powerdown without affecting the lowest power rating and 100 CLKIN cycle recovery.
- Support for crystal operation includes disabling the oscillator to save power (the processor automatically waits 4096 CLKIN cycles for the crystal oscillator to start and stabilize), and letting the oscillator run to allow 100 CLKIN cycle startup.
- Powerdown is initiated by either the powerdown pin ($\overline{\text{PWD}}$) or the software powerdown force bit.
- Interrupt support allows an unlimited number of instructions to be executed before optionally powering down. The powerdown interrupt also can be used as a non-maskable, edge sensitive interrupt.
- Context clear/save control allows the processor to continue where it left off or start with a clean context when leaving the powerdown state.
- The $\overline{\text{RESET}}$ pin also can be used to terminate powerdown, and the host software reset feature can be used to terminate powerdown under certain conditions.
- Powerdown acknowledge pin indicates when the processor has entered powerdown.

Idle

When the ADSP-217x is in the Idle Mode, the processor waits indefinitely in a low power state until an interrupt occurs. When an unmasked interrupt occurs, it is serviced; execution then continues with the instruction following the *IDLE* instruction.

Slow Idle

The *IDLE* instruction is enhanced on the ADSP-217x to let the processor's internal clock signal be slowed during *IDLE*, further reducing power consumption. The reduced clock frequency, a programmable fraction of the normal clock rate, is specified by a selectable divisor given in the *IDLE* instruction. The format of the instruction is

IDLE (n);

where *n* = 16, 32, 64, or 128. This instruction keeps the processor fully functional, but operating at the slower clock rate. While it is in this state, the processor's other internal clock signals, such as SCLK, CLKOUT, and timer clock, are reduced by the same ratio. The default form of the instruction, when no clock divisor is given, is the standard *IDLE* instruction.

When the *IDLE (n)* instruction is used, it effectively slows down the processor's internal clock and thus its response time to incoming interrupts—the 1-cycle response time of the standard idle state is increased by *n*, the clock divisor. When an enabled interrupt is received, the ADSP-217x will remain in the idle state for up to a maximum of *n* processor cycles (*n* = 16, 32, 64, or 128) before resuming normal operation.

When the *IDLE (n)* instruction is used in systems that have an externally generated serial clock (SCLK), the serial clock rate may be faster than the processor's reduced internal clock rate. Under these conditions, interrupts must not be generated at a faster rate than can be serviced, due to the additional time the processor takes to come out of the idle state (a maximum of *n* processor cycles).

SYSTEM INTERFACE

Figure 3 shows a basic system configuration with the ADSP-217x, two serial devices, a host processor, a boot EPROM, and optional external program and data memories. Up to 14K words of data memory and 16K words of program memory can be supported. Programmable wait state generation allows the processor to interface easily to slow memories. The ADSP-217x also provides one external interrupt and two serial ports or three external interrupts and one serial port.

Clock Signals

The ADSP-217x can be clocked by either a crystal or by a TTL-compatible clock signal.

The CLKIN input cannot be halted, changed during operation, or operated below the specified frequency during normal operation. The only exception is while the processor is in the Powerdown State. For additional information, refer to Chapter 9, *ADSP-2100 Family User's Manual* for detailed information on this powerdown feature.

If an external clock is used, it should be a TTL-compatible signal running at half the instruction rate. The signal is connected to the processor's CLKIN input. When an external clock is used, the XTAL input *must* be left unconnected.

The ADSP-217x uses an input clock with a frequency equal to half the instruction rate; a 16.67 MHz input clock yields a 30 ns processor cycle (which is equivalent to 33 MHz). Normally, instructions are executed in a single processor cycle. All device timing is relative to the internal instruction clock rate, which is indicated by the CLKOUT signal when enabled.

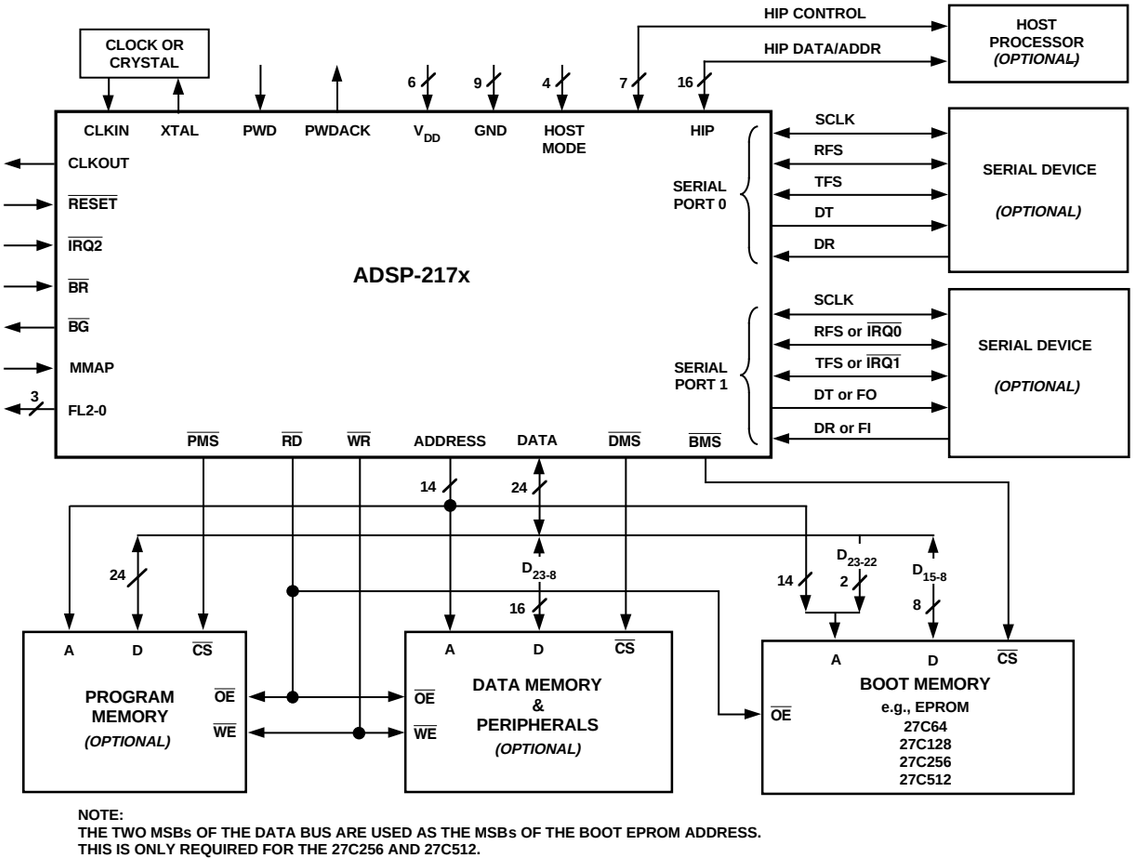


Figure 3. ADSP-217x Basic System Configuration

Because the ADSP-217x includes an on-chip oscillator circuit, an external crystal may be used. The crystal should be connected across the CLKIN and XTAL pins, with two capacitors connected as shown in Figure 4. A parallel-resonant, fundamental frequency, microprocessor-grade crystal should be used.

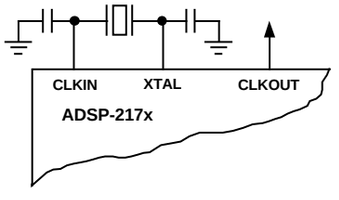


Figure 4. External Crystal Connections

A clock output (CLKOUT) signal is generated by the processor at the processor's cycle rate. This can be enabled and disabled by the CLKODIS bit in the SPORT0 Autobuffer Control Register, DM[0x3FF3].

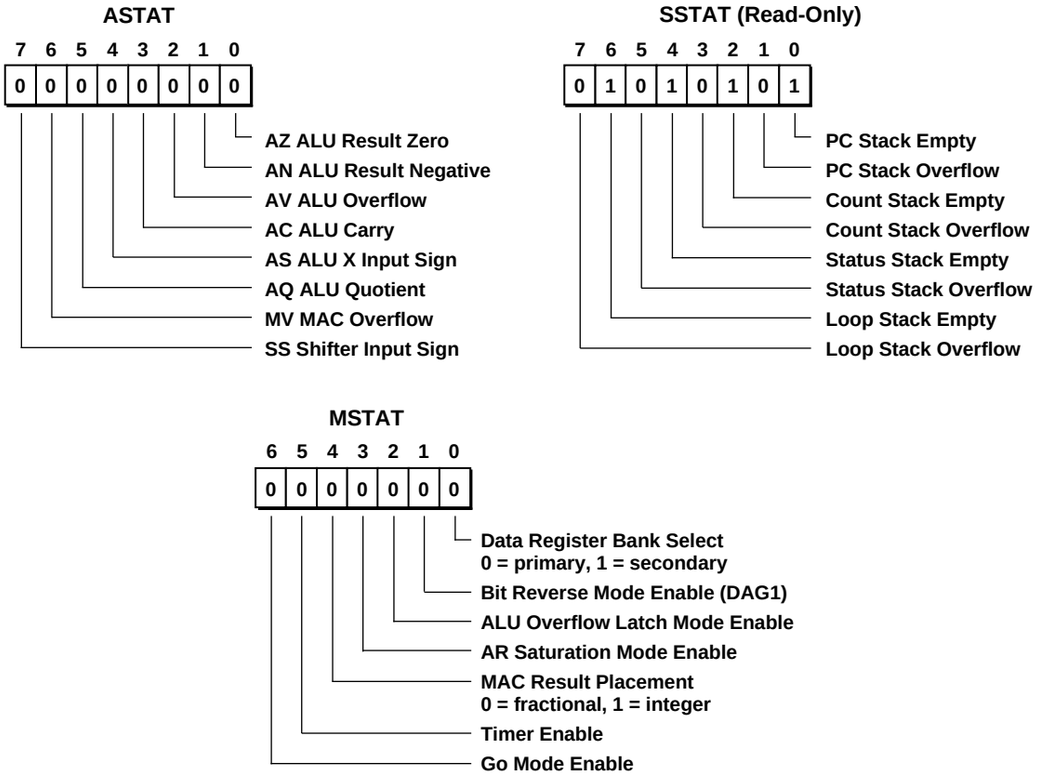
Reset

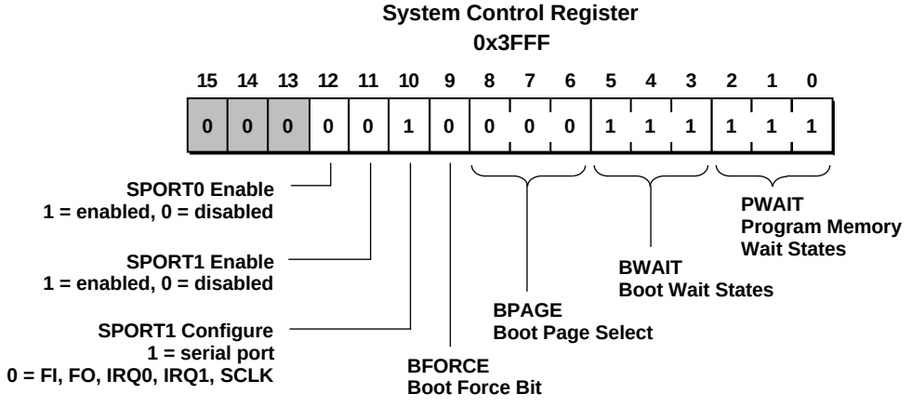
The $\overline{\text{RESET}}$ signal initiates a master reset of the ADSP-217x. The $\overline{\text{RESET}}$ signal must be asserted during the power-up sequence to assure proper initialization. $\overline{\text{RESET}}$ during initial power-up must be held long enough to allow the internal clock to stabilize. If $\overline{\text{RESET}}$ is activated any time after power-up, the clock continues to run and does not require stabilization time.

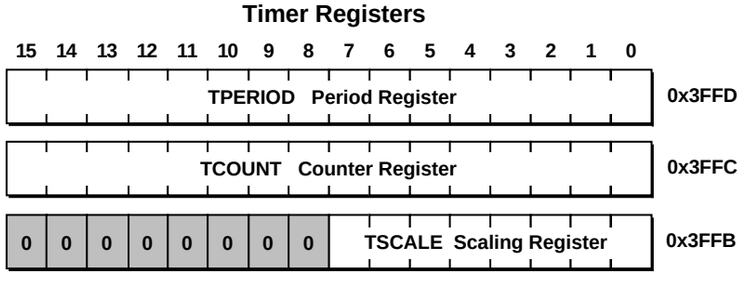
The power-up sequence is defined as the total time required for the crystal oscillator circuit to stabilize after a valid V_{DD} is applied to the processor, and for the internal phase-locked loop (PLL) to lock onto the specific crystal frequency. A minimum of 2000 CLKIN cycles ensures that the PLL has locked but does not include the crystal oscillator start-up time. During this power-up sequence the $\overline{\text{RESET}}$ signal should be held low. On any subsequent resets, the $\overline{\text{RESET}}$ signal must meet the minimum pulse width specification, t_{RSP}.

The $\overline{\text{RESET}}$ input contains some hysteresis; however, if you use an RC circuit to generate your $\overline{\text{RESET}}$ signal, the use of an external Schmidt trigger is recommended.

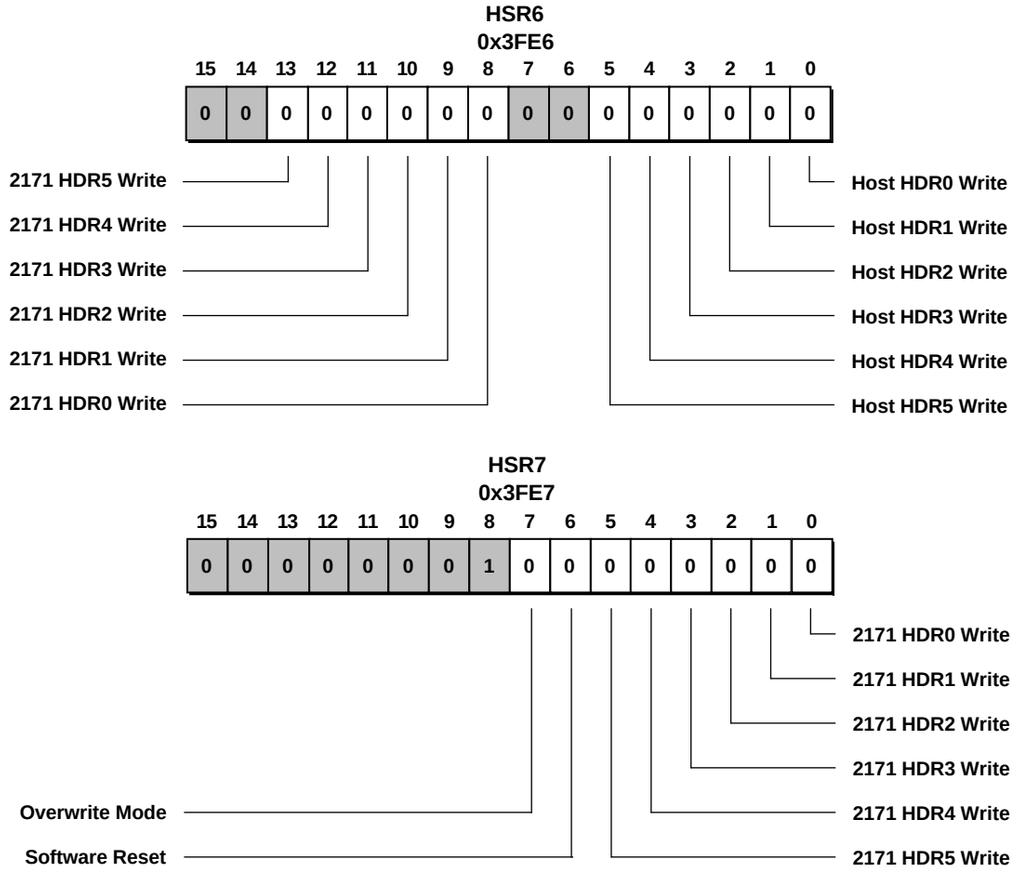
The master reset sets all internal stack pointers to the empty stack condition, masks all interrupts and clears the MSTAT register. When $\overline{\text{RESET}}$ is released, if there is no pending bus request and the chip is configured for booting (MMAP = 0), the boot-loading sequence is performed. Then the first instruction is fetched from internal program memory location 0x0000.







Control Registers



Control Registers

Biased Rounding

A new mode allows biased rounding in addition to the normal unbiased rounding. When the BIASRND bit is set to 0, the normal unbiased rounding operations occur. When the BIASRND bit is set to 1, biased rounding occurs instead of the normal unbiased rounding. When operating in biased rounding mode all rounding operations with MR0 set to 0x8000 will round up, rather than only rounding odd MR1 values up. For example:

MR value before RND	biased RND result	unbiased RND result
00-0000-8000	00-0001-8000	00-0000-8000
00-0001-8000	00-0002-8000	00-0002-8000
00-0000-8001	00-0001-8001	00-0001-8001
00-0001-8001	00-0002-8001	00-0002-8001
00-0000-7FFF	00-0000-7FFF	00-0000-7FFF
00-0001-7FFF	00-0001-7FFF	00-0001-7FFF

This mode only has an effect when the MR0 register contains 0x8000, all other rounding operation work normally. This mode was added to allow more efficient implementation of bit specified algorithms which specify biased rounding such as the GSM speech compression routines. Unbiased rounding is preferred for most algorithms.

Note: BIASRND bit is Bit 12 of the SPORT0 Autobuffer Control register.

INSTRUCTION SET DESCRIPTION

The ADSP-217x assembly language instruction set has an algebraic syntax that was designed for ease of coding and readability. The assembly language, which takes full advantage of the processor's unique architecture, offers the following benefits:

- The algebraic syntax eliminates the need to remember cryptic assembler mnemonics. For example, a typical arithmetic add instruction, such as AR = AX0 + AY0, resembles a simple equation.
- Every instruction assembles into a single, 24-bit word that can execute in a single instruction cycle.
- The syntax is a superset ADSP-2100 Family assembly language and is completely source and object code compatible with other family members. Programs may need to be relocated to utilize internal memory and conform to the ADSP-217x's interrupt vector and reset vector map.
- Sixteen condition codes are available. For conditional jump, call, return, or arithmetic instructions, the condition can be checked and the operation executed in the same instruction cycle.
- Multifunction instructions allow parallel execution of an arithmetic instruction with up to two fetches or one write to processor memory space during a single instruction cycle.

Consult the *ADSP-2100 Family User's Manual* for a complete description of the syntax and an instruction set reference.

ADSP-2171/ADSP-2172

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . –0.3 V to +7 V
Input Voltage . . . . . –0.3 V to V_{DD} + 0.3 V
Output Voltage Swing . . . . . –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range (Ambient) . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (5 sec) TQFP . . . . . +280°C
Lead Temperature (5 sec) PQFP . . . . . +280°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD SENSITIVITY

The ADSP-217x is an ESD (electrostatic discharge) sensitive device. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur to devices subjected to high energy electrostatic discharges.

The ADSP-217x features proprietary ESD protection circuitry to dissipate high energy discharges (Human Body Model). Per method 3015 of MIL-STD-883, the ADSP-217x has been classified as a Class 1 device.

Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Unused devices must be stored in conductive foam or shunts, and the foam should be discharged to the destination before devices are removed.

ADSP-2171/ADSP-2172 TIMING PARAMETERS

GENERAL NOTES

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, you cannot meaningfully add up parameters to derive longer times.

TIMING NOTES

Switching characteristics specify how the processor changes its signals. You have no control over this timing; it is dependent on the internal design. Timing requirements apply to signals that are controlled outside the processor, such as the data input for a read operation.

Timing requirements guarantee that the processor operates correctly with another device. Switching characteristics tell you what the device will do under a given circumstance. Also, use the switching characteristics to ensure any timing requirement of a device connected to the processor (such as memory) is satisfied.

ADSP-2171/ADSP-2172

MEMORY REQUIREMENTS

This chart links common memory device specification names and ADSP-2171/ADSP-2172 timing parameters for your convenience.

Parameter Name	Function	Common Memory Device Specification Name
t_{ASW}	A0-A13, $\overline{DMS}$, $\overline{PMS}$ Setup before $\overline{WR}$ Low	Address Setup to Write Start
t_{AW}	A0-A13, $\overline{DMS}$, $\overline{PMS}$ before $\overline{WR}$ Deasserted	Setup Address Setup to Write End
t_{WRA}	A0-A13, $\overline{DMS}$, $\overline{PMS}$ Hold after $\overline{WR}$ Deasserted	Address Hold Time
t_{DW}	Data Setup before $\overline{WR}$ High	Data Setup Time
t_{DH}	Data Hold after $\overline{WR}$ High	Data Hold Time
t_{RDD}	$\overline{RD}$ Low to Data Valid	$\overline{OE}$ to Data Valid
t_{AA}	A0-A13, $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$ to Data Valid	Address Access Time

ADSP-2171/ADSP-2172

Parameter		Min	Max	Unit
Clock Signals				
t_{CK} is defined as 0.5 t_{CKI}. The ADSP-2171/ADSP-2172 uses an input clock with a frequency equal to half the instruction rate; a clock (which is equivalent to 60 ns) yields a 30 ns processor cycle 16.67 MHz input (equivalent to 33 MHz). t_{CK} values within the range of 0.5 t_{CKI} period should be substituted for all relevant timing parameters to obtain specification value. Example: $t_{CKH} = 0.5t_{CK} – 7$ ns = 0.5 (30 ns) – 7 ns = 8 ns.				
Timing Requirement:				
t_{CKI}	CLKIN Period	60	150	ns
t_{CKIL}	CLKIN Width Low	20		ns
t_{CKIH}	CLKIN Width High	20		ns
Switching Characteristic:				
t_{CKL}	CLKOUT Width Low	$0.5t_{CK} – 7$		ns
t_{CKH}	CLKOUT Width High	$0.5t_{CK} – 7$		ns
t_{CKOH}	CLKIN High to CLKOUT High	0	20	ns
Control Signals				
Timing Requirement:				
t_{RSP}	RESET Width Low	$5t_{CK}$[1]		ns

NOTE
[1]Applies after power-up sequence is complete. Internal phase lock loop requires no more than 2000 CLKIN cycles assuming stable CLKIN (not including crystal oscillator start-up time).

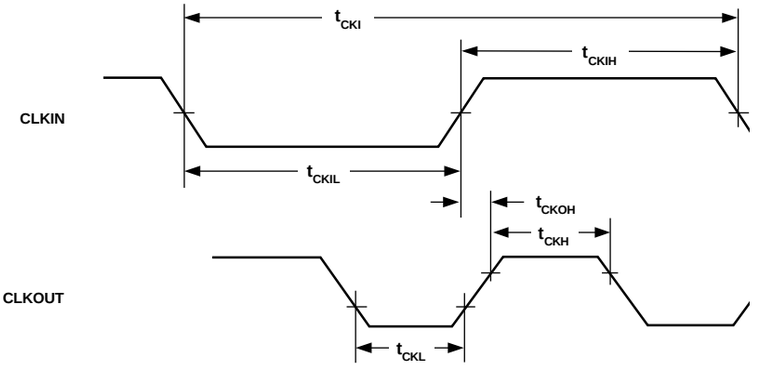


Figure 8. Clock Signals

ADSP-2171/ADSP-2172

Parameter		Min	Max	Unit
Memory Read				
Timing Requirement:				
t_{RDD}	$\overline{RD}$ Low to Data Valid		$0.5t_{CK} - 9 + w$	ns
t_{AA}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ to Data Valid		$0.75t_{CK} - 10.5 + w$	ns
t_{RDH}	Data Hold from $\overline{RD}$ High	0		ns
Switching Characteristic:				
t_{RP}	$\overline{RD}$ Pulse Width	$0.5t_{CK} - 5 + w$		ns
t_{CRD}	CLKOUT High to $\overline{RD}$ Low	$0.25t_{CK} - 5$	$0.25t_{CK} + 7$	ns
t_{ASR}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ Setup before $\overline{RD}$ Low	$0.25t_{CK} - 6$		ns
t_{RDA}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ Hold after $\overline{RD}$ Deasserted	$0.25t_{CK} - 3$		ns
t_{RWR}	$\overline{RD}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK} - 5$		ns

w = wait states x t_{CK}.

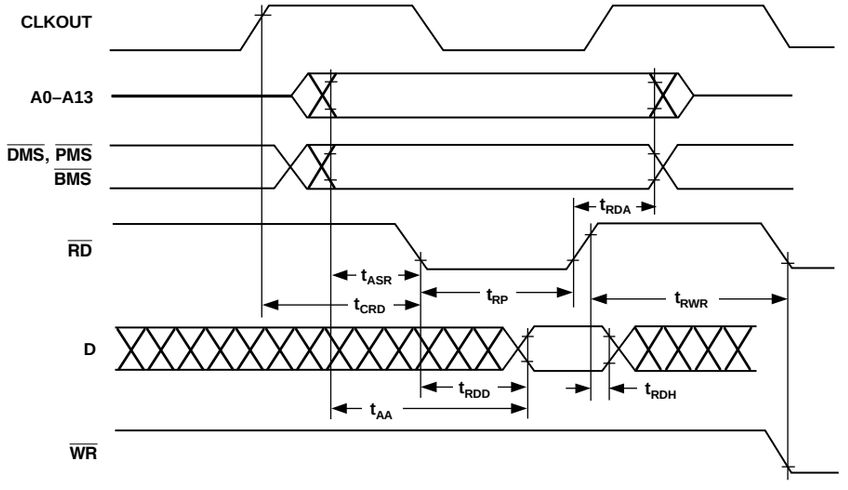


Figure 11. Memory Read

ADSP-2171/ADSP-2172

Parameter		Min	Max	Unit
Serial Ports				
Timing Requirement:				
t_{SCK}	SCLK Period	50		ns
t_{SCS}	DR/TFS/RFS Setup before SCLK Low	4		ns
t_{SCH}	DR/TFS/RFS Hold after SCLK Low	7		ns
t_{SCP}	$SCLK_{IN}$ Width	20		ns
Switching Characteristic:				
t_{CC}	CLKOUT High to $SCLK_{OUT}$	$0.25t_{CK}$	$0.25t_{CK}$ + 10	ns
t_{SCDE}	SCLK High to DT Enable	0		ns
t_{SCDV}	SCLK High to DT Valid		15	ns
t_{RH}	TFS/RFS_{OUT} Hold after SCLK High	0		ns
t_{RD}	TFS/RFS_{OUT} Delay from SCLK High		15	ns
t_{SCDH}	DT Hold after SCLK High	0		ns
t_{TDE}	TFS(Alt) to DT Enable	0		ns
t_{TDV}	TFS(Alt) to DT Valid		15	ns
t_{SCDD}	SCLK High to DT Disable		15	ns
t_{RDV}	RFS (Multichannel, Frame Delay Zero) to DT Valid		15	ns

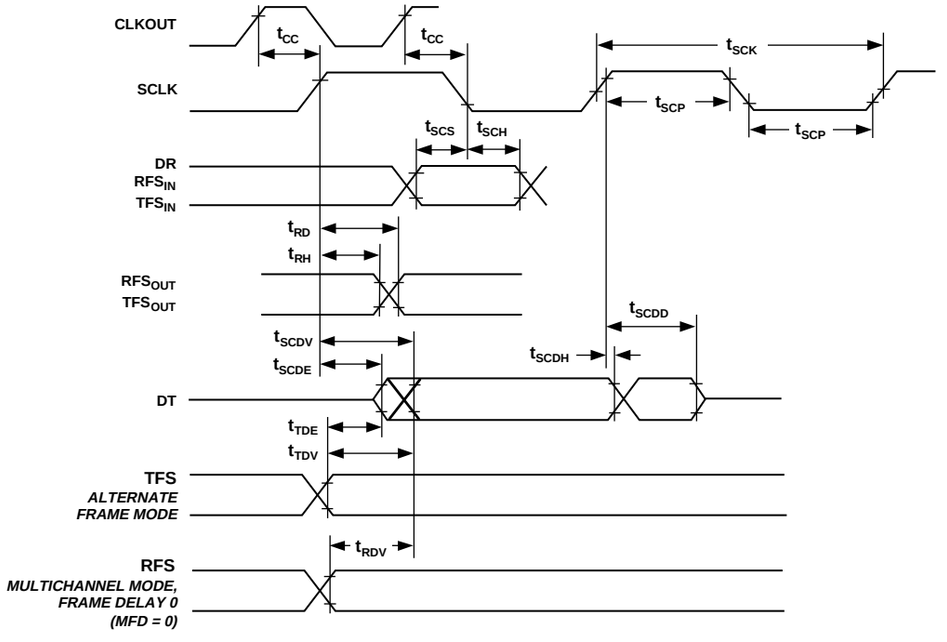


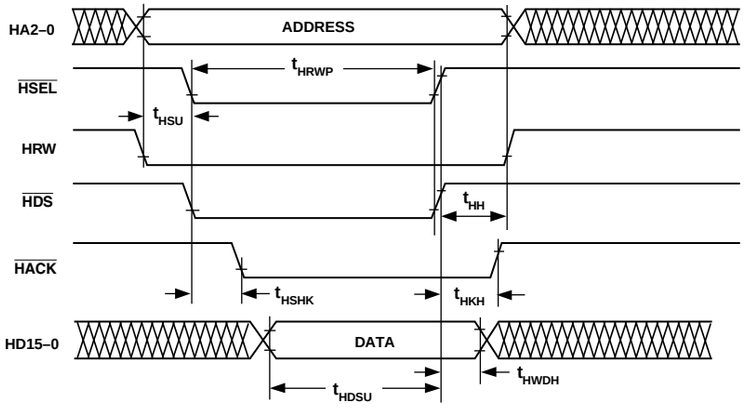
Figure 13. Serial Ports

ADSP-2171/ADSP-2172

Parameter		Min	Max	Unit
Host Interface Port				
Separate Data and Address (HMD1 = 0)				
Read Strobe and Write Strobe (HMD0 = 1)				
Timing Requirement:				
t_{HSU}	HA2–0, HRW Setup before Start of Write or Read[1]	5		ns
t_{HDSU}	Data Setup before End of Write[2]	5		ns
t_{HWDH}	Data Hold after End of Write[2]	3		ns
t_{HH}	HA2–0, HRW Hold after End of Write or Read[2]	3		ns
t_{HRWP}	Read or Write Pulse Width[3]	20		ns
Switching Characteristic:				
t_{HSHK}	$\overline{HACK}$ Low after Start of Write or Read[1]	0	15	ns
t_{HKH}	$\overline{HACK}$ Hold after End of Write or Read[2]	0	15	ns
t_{HDE}	Data Enabled after Start of Read[1]	0		ns
t_{HDD}	Data Valid after Start of Read[1]		18	ns
t_{HRDH}	Data Hold after End of Read[2]	0		ns
t_{HRDD}	Data Disabled after End of Read[2]		7	ns

NOTES
[1]Start of Write or Read = $\overline{HDS}$ Low and $\overline{HSEL}$ Low.
[2]End of Write or Read = $\overline{HDS}$ High and $\overline{HSEL}$ High.
[3]Read or Write Pulse Width = $\overline{HDS}$ Low and $\overline{HSEL}$ Low.

Host Write Cycle



Host Read Cycle

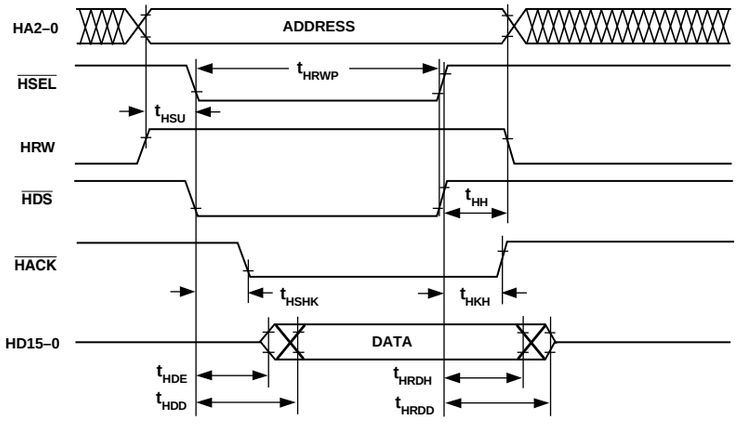


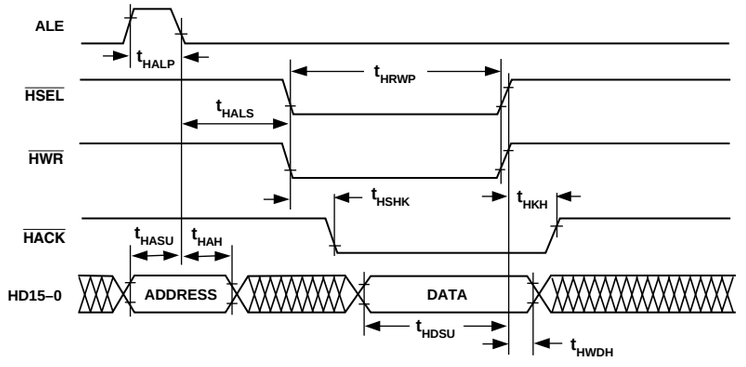
Figure 15. Host Interface Port (HMD1 = 0, HMD0 = 1)

ADSP-2171/ADSP-2172

Parameter		Min	Max	Unit
Host Interface Port				
Multiplexed Data and Address (HMD1 = 1)				
Read Strobe and Write Strobe (HMD0 = 0)				
Timing Requirement:				
t_{HALP}	ALE Pulse Width	10		ns
t_{HASU}	HAD15–0 Address Setup, before ALE Low	5		ns
t_{HAH}	HAD15–0 Address Hold after ALE Low	2		ns
t_{HALS}	Start of Write or Read after ALE Low[1, 2]	10		ns
t_{HDSU}	HAD15–0 Data Setup before End of Write[3]	5		ns
t_{HWDH}	HAD15–0 Data Hold after End of Write[3]	3		ns
t_{HRWP}	Read or Write Pulse Width[4]	20		ns
Switching Characteristic:				
t_{HSHK}	$\overline{HACK}$ Low after Start of Write or Read[1, 2]	0	15	ns
t_{HKH}	$\overline{HACK}$ Hold after End of Write or Read[3, 5]	0	15	ns
t_{HDE}	HAD15–0 Data Enabled after Start of Read[2]	0		ns
t_{HDD}	HAD15–0 Data Valid after Start of Read[2]		18	ns
t_{HRDH}	HAD15–0 Data Hold after End of Read	0		ns
t_{HRDD}	HAD15–0 Data Disabled after End of Read[5]		7	ns

NOTES
[1]Start of Write = $\overline{HWR}$ Low and $\overline{HSEL}$ Low.
[2]Start of Read = $\overline{HRD}$ Low and $\overline{HSEL}$ Low.
[3]End of Write = $\overline{HWR}$ High or $\overline{HSEL}$ High.
[4]Read Pulse Width = $\overline{HRD}$ Low and $\overline{HSEL}$ Low, Write Pulse Width = $\overline{HWR}$ Low and $\overline{HSEL}$ Low.
[5]End of Read = $\overline{HRD}$ High or $\overline{HSEL}$ High.

Host Write Cycle



Host Read Cycle

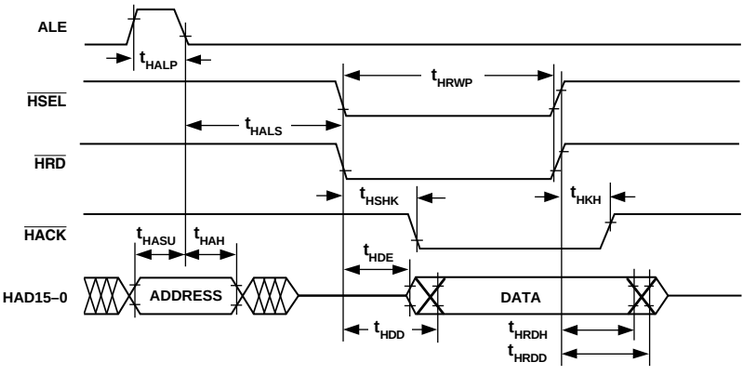


Figure 16. Host Interface Port (HMD1 = 1, HMD0 = 0)

ADSP-2173 TIMING PARAMETERS

GENERAL NOTES

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, you cannot meaningfully add up parameters to derive longer times.

TIMING NOTES

Switching characteristics specify how the processor changes its signals. You have no control over this timing; it is dependent on the internal design. Timing requirements apply to signals that are controlled outside the processor, such as the data input for a read operation.

Timing requirements guarantee that the processor operates correctly with another device. Switching characteristics tell you what the device will do under a given circumstance. Also, use the switching characteristics to ensure any timing requirement of a device connected to the processor (such as memory) is satisfied.

MEMORY REQUIREMENTS

This chart links common memory device specification names and ADSP-2173 timing parameters for your convenience.

Parameter Name	Function	Common Memory Device Specification Name
t_{ASW}	A0-A13, $\overline{DMS}$, $\overline{PMS}$ Setup before $\overline{WR}$ Low	Address Setup to Write Start
t_{AW}	A0-A13, $\overline{DMS}$, $\overline{PMS}$ before $\overline{WR}$ Deasserted	Setup Address Setup to Write End
t_{WRA}	A0-A13, $\overline{DMS}$, $\overline{PMS}$ Hold after $\overline{WR}$ Deasserted	Address Hold Time
t_{DW}	Data Setup before $\overline{WR}$ High	Data Setup Time
t_{DH}	Data Hold after $\overline{WR}$ High	Data Hold Time
t_{RDD}	$\overline{RD}$ Low to Data Valid	$\overline{OE}$ to Data Valid
t_{AA}	A0-A13, $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$ to Data Valid	Address Access Time

ADSP-2173

Parameter		Min	Max	Unit
Clock Signals				
t_{CK} is defined as 0.5 t_{CKI}. The ADSP-2173 uses an input clock with a frequency equal to half the instruction rate; a 10.0 MHz input clock (which is equivalent to 100 ns) yields a 50 ns processor cycle (equivalent to 20 MHz). t_{CK} values within the range of 0.5 t_{CKI} period should be substituted for all relevant timing parameters to obtain specification value. Example: t_{CKH} = 0.5t_{CK} – 10 ns = 0.5 (50 ns) – 10 ns = 15 ns.				
Timing Requirement:				
t_{CKI}	CLKIN Period	100	160	ns
t_{CKIL}	CLKIN Width Low	20		ns
t_{CKIH}	CLKIN Width High	20		ns
Switching Characteristic:				
t_{CKL}	CLKOUT Width Low	0.5t_{CK} – 10		ns
t_{CKH}	CLKOUT Width High	0.5t_{CK} – 10		ns
t_{CKOH}	CLKIN High to CLKOUT High	0	25	ns
Control Signals				
Timing Requirement:				
t_{RSP}	RESET Width Low	5t_{CK}[1]		ns

NOTE
[1]Applies after power-up sequence is complete. Internal phase lock loop requires no more than 2000 CLKIN cycles assuming stable CLKIN (not including crystal oscillator start-up time).

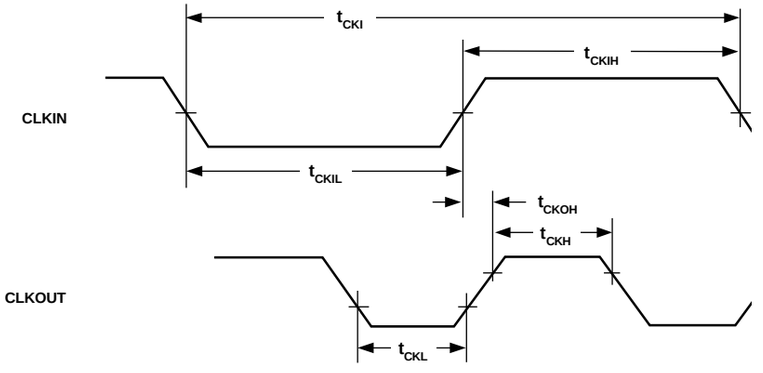


Figure 24. Clock Signals

ADSP-2173

Parameter		Min	Max	Unit
Interrupts and Flags				
Timing Requirement:				
t_{IFS}	$\overline{IRQx}$ or FI Setup before CLKOUT Low[1, 2, 3]	$0.25t_{CK}$ + 23		ns
t_{IFH}	$\overline{IRQx}$ or FI Hold after CLKOUT High[1, 2, 3]	$0.25t_{CK}$		ns
Switching Characteristic:				
t_{FOH}	Flag Output Hold after CLKOUT Low[4]	$0.5t_{CK}$ – 10		ns
t_{FOD}	Flag Output Delay from CLKOUT Low[4]		$0.5t_{CK}$ + 5	ns

NOTES
[1]If $\overline{IRQx}$ and FI inputs meet t_{IFS} and t_{IFH} setup/hold requirements, they will be recognized during the current clock cycle; otherwise the signals will be recognized on the following cycle. (Refer to "Interrupt Controller Operation" in the Program Control chapter of the User's Manual for further information on interrupt servicing.)
[2]Edge-sensitive interrupts require pulse widths greater than 10 ns; level-sensitive interrupts must be held low until serviced.
[3]$\overline{IRQx}$ = $\overline{IRQ0}$, $\overline{IRQ1}$, and $\overline{IRQ2}$.
[4]Flag Output = FL0, FL1, FL2, and FO.

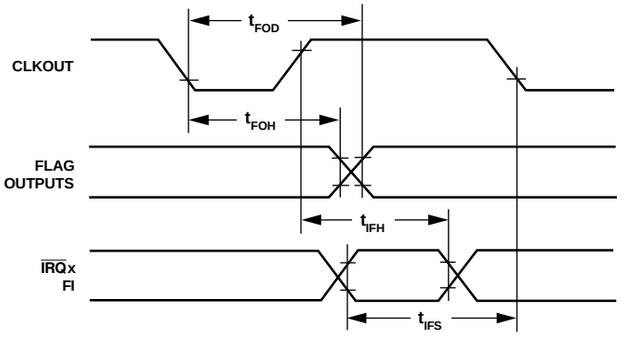


Figure 25. Interrupts and Flags

ADSP-2173

Parameter		Min	Max	Unit
Host Interface Port				
Multiplexed Data and Address (HMD1 = 1)				
Read Strobe and Write Strobe (HMD0 = 1)				
Timing Requirement:				
t_{HALP}	ALE Pulse Width	15		ns
t_{HASU}	HAD15–0 Address Setup before ALE Low	5		ns
t_{HAH}	HAD15–0 Address Hold after ALE Low	2		ns
t_{HALS}	Start of Write or Read after ALE Low[1]	15		ns
t_{HSU}	HRW Setup before Start of Write or Read[1]	8		ns
t_{HDSU}	HAD15–0 Data Setup before End of Write[2]	8		ns
t_{HWDH}	HAD15–0 Data Hold after End of Write[2]	3		ns
t_{HH}	HRW Hold after End of Write or Read[2]	3		ns
t_{HRWP}	Read or Write Pulse Width[3]	30		ns
Switching Characteristic:				
t_{HSHK}	$\overline{HACK}$ Low after Start of Write or Read[1]	0	20	ns
t_{HKH}	$\overline{HACK}$ Hold after End of Write or Read[2]	0	20	ns
t_{HDE}	HAD15–0 Data Enabled after Start of Read[1]	0		ns
t_{HDD}	HAD15–0 Data Valid after Start of Read[1]		23	ns
t_{HRDH}	HAD15–0 Data Hold after End of Read[2]	0		ns
t_{HRDD}	HAD15–0 Data Disabled after End of Read[2]		15	ns

NOTES
[1]Start of Write or Read = $\overline{HDS}$ Low and $\overline{HSEL}$ Low.
[2]End of Write or Read = $\overline{HDS}$ High and $\overline{HSEL}$ High.
[3]Read or Write Pulse Width = $\overline{HDS}$ Low and $\overline{HSEL}$ Low.

Host Write Cycle

Host Read Cycle

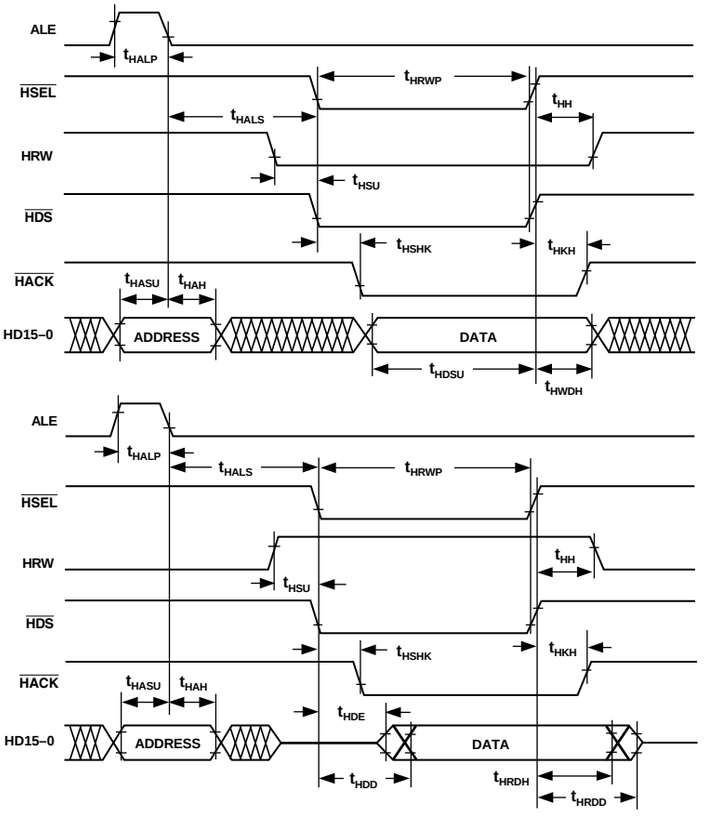


Figure 33. Host Interface Port (HMD1 = 1, HMD0 = 1)

ADSP-2173

CAPACITIVE LOADING

Figures 35 and 36 show the capacitive loading characteristics of the ADSP-2173.

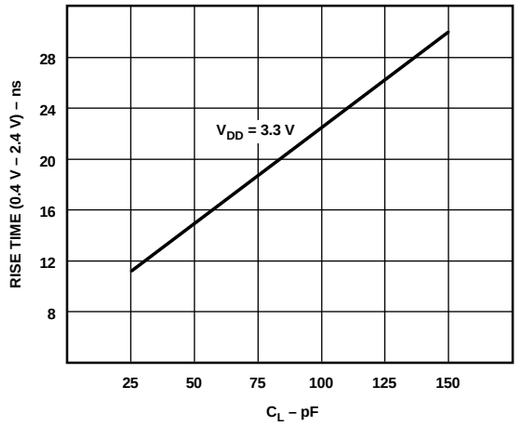


Figure 35. Typical Output Rise Time vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

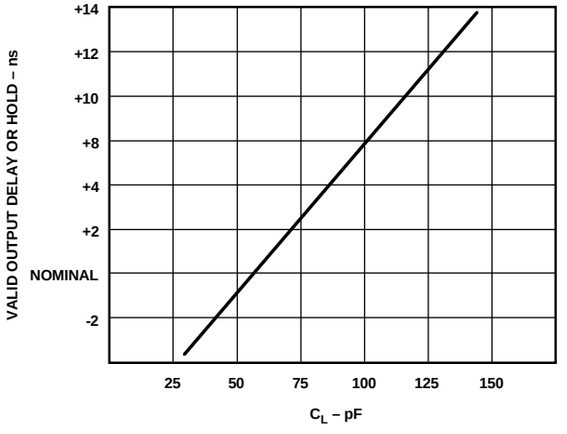


Figure 36. Typical Output Valid Delay or Hold vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

TEST CONDITIONS

Output Disable Time

Output pins are considered to be disabled when they have stopped driving and started a transition from the measured output high or low voltage to a high impedance state. The output disable time (t_{DIS}) is the difference of $t_{MEASURED}$ and t_{DECAY}, as shown in the Output Enable/Disable diagram. The time is the interval from when a reference signal reaches a high or low voltage level to when the output voltages have changed by 0.5 V from the measured output high or low voltage. The decay time, t_{DECAY}, is dependent on the capacitative load, C_L, and the current load, i_L, on the output pin. It can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \bullet 0.5\,V}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. If multiple pins (such as the data bus) are disabled, the measurement value is that of the last pin to stop driving.

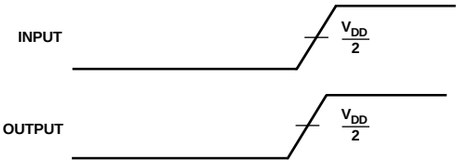


Figure 37. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Enable Time

Output pins are considered to be enabled when that have made a transition from a high-impedance state to when they start driving. The output enable time (t_{ENA}) is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in the Output Enable/Disable diagram. If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

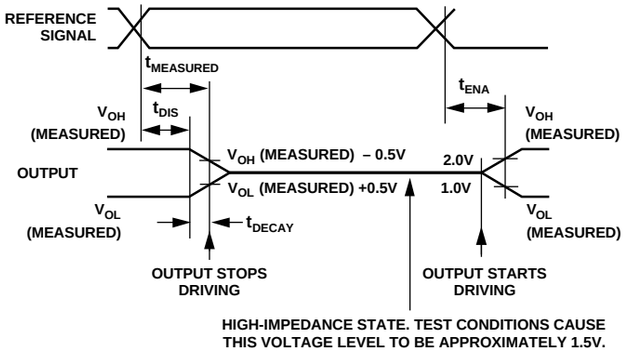


Figure 38. Output Enable/Disable

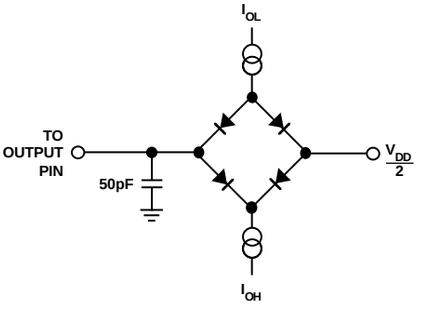
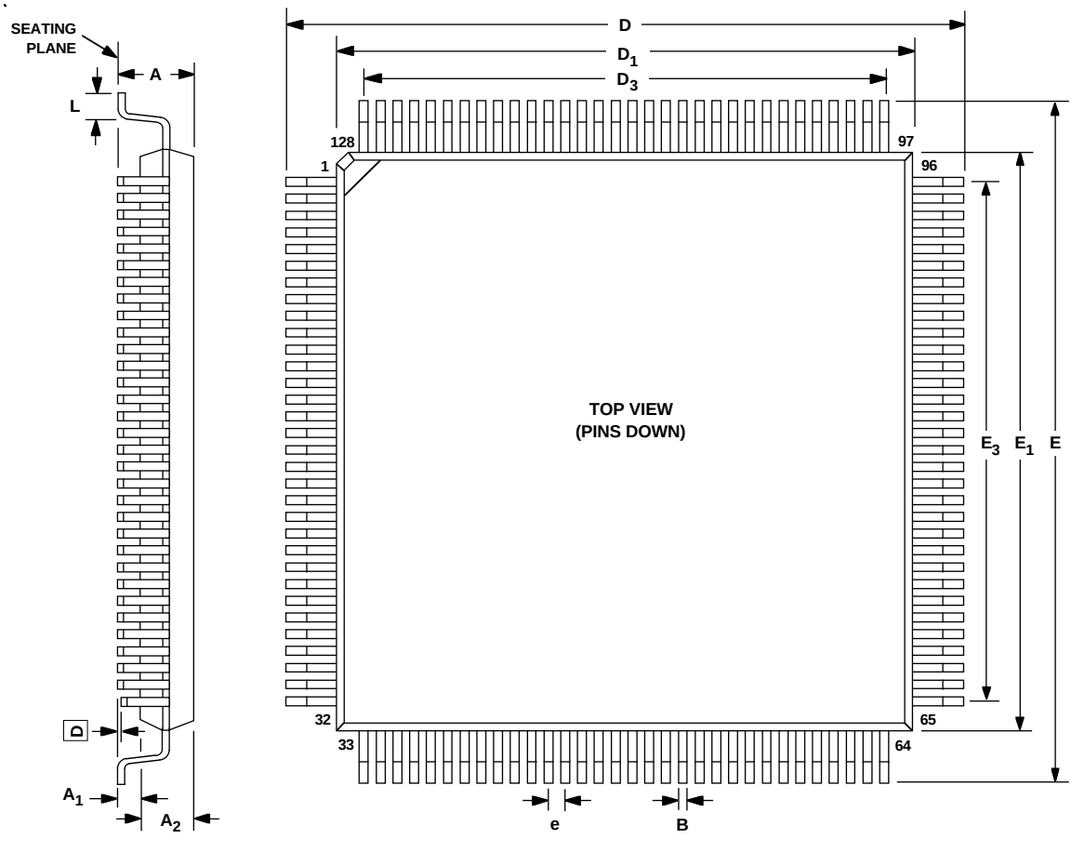


Figure 39. Equivalent Device Loading for AC Measurements (Including All Fixtures)

OUTLINE DIMENSIONS
128-Lead Metric Thin Plastic Quad Flatpack (PQFP)



SYMBOL	MILLIMETERS			INCHES		
	MIN	TYP	MAX	MIN	TYP	MAX
A			4.07			0.160
A_1	0.25			0.010		
A_2	3.17	3.49	3.67	0.125	0.137	0.144
D, E	30.95	31.20	31.45	1.219	1.228	1.238
D_1, E_1	27.90	28.00	28.10	1.098	1.102	1.106
D_3, E_3	24.73	24.80	24.87	0.974	0.976	0.979
L	0.65	0.88	1.03	0.031	0.035	0.041
e	0.73	0.80	0.87	0.029	0.031	0.034
B	0.30	0.35	0.45	0.012	0.014	0.018
D			0.10			0.004

ORDERING GUIDE*

Part Number**	Ambient Temperature Range	Instruction Rate (MHz)	Package Description
ADSP-2171KST-133	0°C to +70°C	33.33	128-Lead TQFP
ADSP-2171BST-133	–40°C to +85°C	33.33	128-Lead TQFP
ADSP-2171KS-133	0°C to +70°C	33.33	128-Lead PQFP
ADSP-2171BS-133	–40°C to +85°C	33.33	128-Lead PQFP
ADSP-2171KST-104	0°C to +70°C	26	128-Lead TQFP
ADSP-2171BST-104	–40°C to +85°C	26	128-Lead TQFP
ADSP-2171KS-104	0°C to +70°C	26	128-Lead PQFP
ADSP-2171BS-104	–40°C to +85°C	26	128-Lead PQFP
ADSP-2173BST-80	–40°C to +85°C	20	128-Lead TQFP
ADSP-2173BS-80	–40°C to +85°C	20	128 Lead PQFP

*Refer to section titled “Ordering Procedure for ADSP-2172 ROM Processors” for information about ordering ROM-coded parts.
**S = Plastic Quad Flatpack, ST = Plastic Thin Quad Flatpack.