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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	AVR
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	32
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atmega164a-au

- Programmable Watchdog Timer with Separate On-chip Oscillator
- On-chip Analog Comparator
- Interrupt and Wake-up on Pin Change
- Special Microcontroller Features
 - Power-on Reset and Programmable Brown-out Detection
 - Internal Calibrated RC Oscillator
 - External and Internal Interrupt Sources
 - Six Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby and Extended Standby
- I/O and Packages
 - 32 Programmable I/O Lines
 - 40-pin PDIP, 44-lead TQFP, 44-pad VQFN/QFN/MLF
 - 44-pad DRQFN
- **49-ball VFBGA**
 - Operating Voltages
 - 1.8 - 5.5V
 - Speed Grades
 - 0 - 4MHz @ 1.8 - 5.5V
 - 0 - 10MHz @ 2.7 - 5.5V
 - 0 - 20MHz @ 4.5 - 5.5V
 - Power Consumption at 1MHz, 1.8V, 25°C
 - Active: 0.4mA
 - Power-down Mode: 0.1µA
 - Power-save Mode: 0.6µA (Including 32kHz RTC)

Note: 1. See ["Data retention" on page 9](#) for details.

1.2 Pinout - DRQFN for Atmel ATmega164A/164PA/324A/324PA

Figure 1-2. DRQFN - pinout.

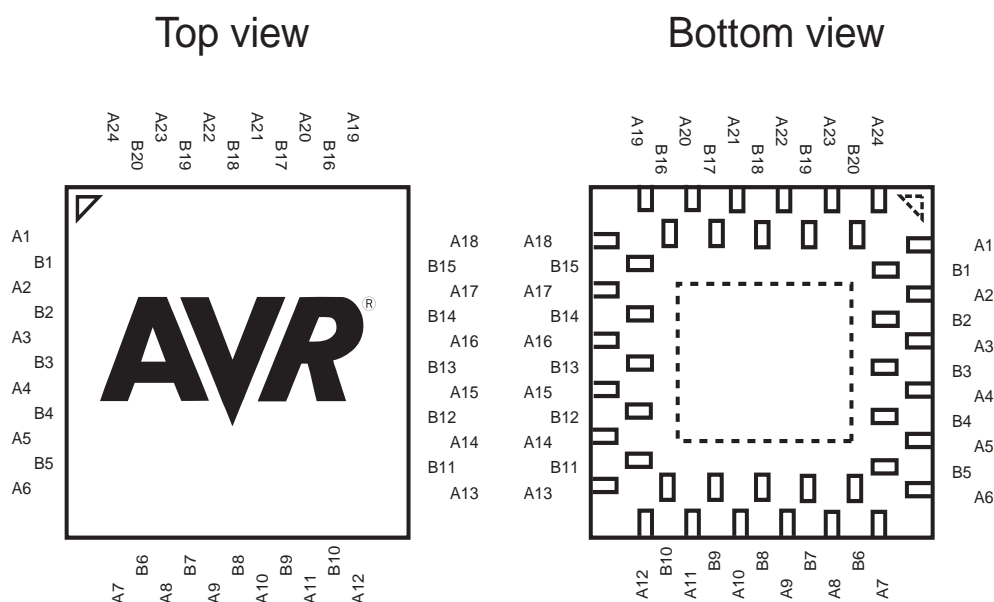
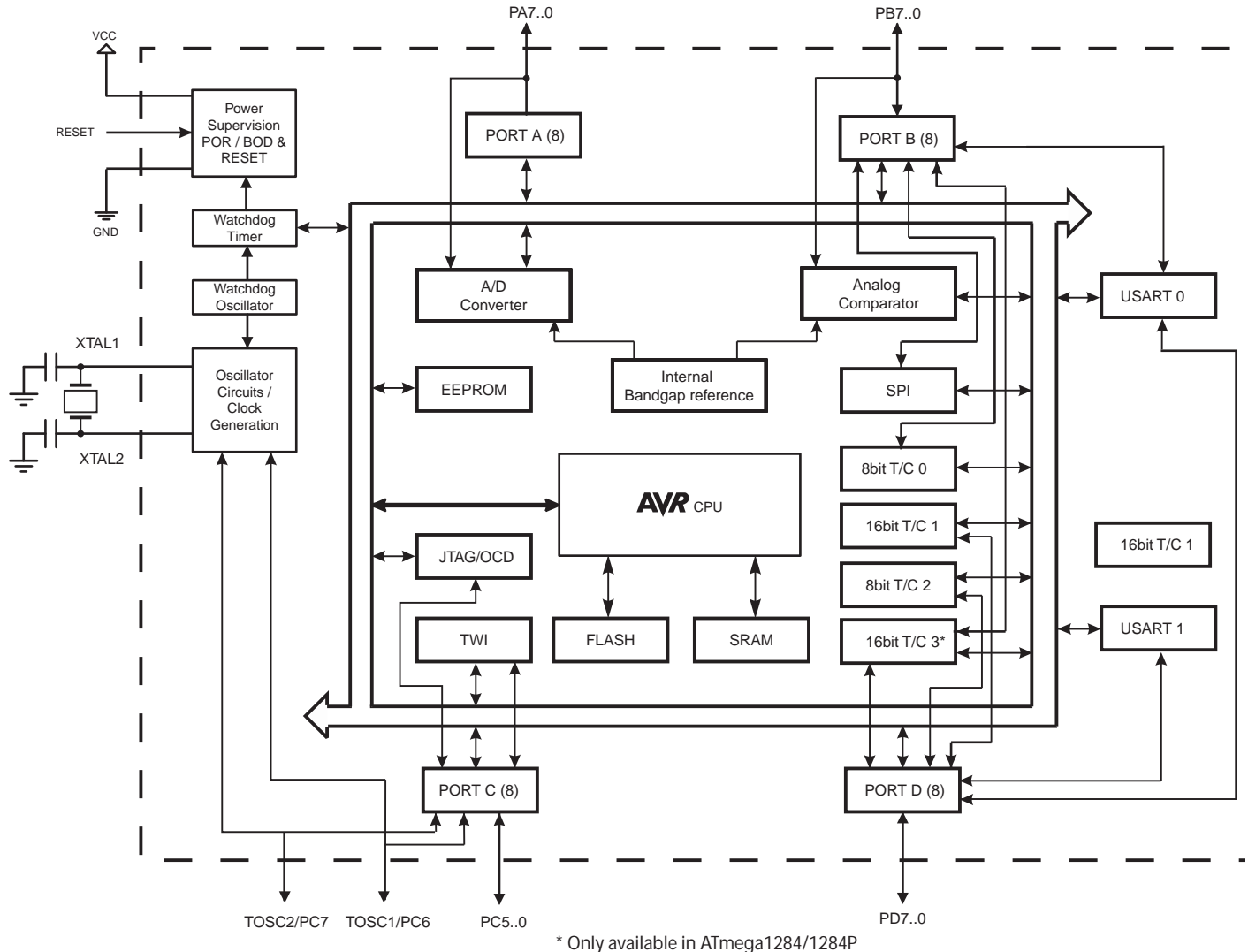


Table 1-1. DRQFN - pinout.

A1	PB5	A7	PD3	A13	PC4	A19	PA3
B1	PB6	B6	PD4	B11	PC5	B16	PA2
A2	PB7	A8	PD5	A14	PC6	A20	PA1
B2	RESET	B7	PD6	B12	PC7	B17	PA0
A3	VCC	A9	PD7	A15	AVCC	A21	VCC
B3	GND	B8	VCC	B13	GND	B18	GND
A4	XTAL2	A10	GND	A16	AREF	A22	PB0
B4	XTAL1	B9	PC0	B14	PA7	B19	PB1
A5	PD0	A11	PC1	A17	PA6	A23	PB2
B5	PD1	B10	PC2	B15	PA5	B20	PB3
A6	PD2	A12	PC3	A18	PA4	A24	PB4

2.1 Block diagram

Figure 2-1. Block diagram.



The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The Atmel ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P provide the following features:

16/32/64/128Kbytes of In-System Programmable Flash with Read-While-Write capabilities, 512/1K/2K/4Kbytes EEPROM, 1/2/4/16Kbytes SRAM, 32 general purpose I/O lines, 32 general purpose working registers, Real Time Counter (RTC), three (four for ATmega1284/1284P) flexible Timer/Counters with compare modes and PWM, 2 USARTs, a byte oriented two-wire Serial Interface, a 8-channel, 10-bit ADC with optional differential input stage with programmable gain, programmable Watchdog Timer with Internal Oscillator, an SPI serial port, IEEE std. 1149.1 compliant JTAG test interface, also used for accessing the On-chip Debug system and programming and six software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, SPI port, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next interrupt or Hardware Reset. In Power-save mode, the asynchronous timer continues to run, allowing the user to maintain a

timer base while the rest of the device is sleeping. The ADC Noise Reduction mode stops the CPU and all I/O modules except Asynchronous Timer and ADC, to minimize switching noise during ADC conversions. In Standby mode, the Crystal/Resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low power consumption. In Extended Standby mode, both the main Oscillator and the Asynchronous Timer continue to run.

Atmel offers the QTouch® library for embedding capacitive touch buttons, sliders and wheels functionality into AVR microcontrollers. The patented charge-transfer signal acquisition offers robust sensing and includes fully debounced reporting of touch keys and includes Adjacent Key Suppression® (AKS™) technology for unambiguous detection of key events. The easy-to-use QTouch Suite toolchain allows you to explore, develop and debug your own touch applications.

The device is manufactured using Atmel's high-density nonvolatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed in-system through an SPI serial interface, by a conventional nonvolatile memory programmer, or by an On-chip Boot program running on the AVR core. The boot program can use any interface to download the application program in the application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P is supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, in-circuit emulators, and evaluation kits.

2.2 Comparison between ATmega164A, ATmega164PA, ATmega324A, ATmega324PA, ATmega644A, ATmega644PA, ATmega1284 and ATmega1284P

Table 2-1. Differences between ATmega164A, ATmega164PA, ATmega324A, ATmega324PA, ATmega644A, ATmega644PA, ATmega1284 and ATmega1284P.

Device	Flash	EEPROM	RAM	Units
ATmega164A	16K	512	1K	bytes
ATmega164PA	16K	512	1K	
ATmega324A	32K	1K	2K	
ATmega324PA	32K	1K	2K	
ATmega644A	64K	2K	4K	
ATmega644PA	64K	2K	4K	
ATmega1284	128K	4K	16K	
ATmega1284P	128K	4K	16K	

2.3 Pin Descriptions¹¹

2.3.1 VC

Digital supply voltage.

2.3.2 GND

Ground.

2.3.3 Port A (PA7:PA0)

Port A serves as analog inputs to the Analog-to-digital Converter.

Port A also serves as an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port A output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port A pins that are externally pulled low will source current if the pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port A also serves the functions of various special features of the Atmel ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P as listed on [page 79](#).

2.3.4 Port B (PB7:PB0)

Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B also serves the functions of various special features of the ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P as listed on [page 80](#).

2.3.5 Port C (PC7:PC0)

Port C is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port C also serves the functions of the JTAG interface, along with special features of the Atmel ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P as listed on [page 83](#).

2.3.6 Port D (PD7:PD0)

Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port D also serves the functions of various special features of the ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P as listed on [page 86](#).

2.3.7 RESET

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in [" on page 325](#). Shorter pulses are not guaranteed to generate a reset.

2.3.8 XTAL1

Input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

2.3.9 XTAL2

Output from the inverting Oscillator amplifier.

2.3.10 AVCC

AVCC is the supply voltage pin for Port A and the Analog-to-digital Converter. It should be externally connected to V_{CC} , even if the ADC is not used. If the ADC is used, it should be connected to V_{CC} through a low-pass filter.

2.3.11 AREF

This is the analog reference pin for the Analog-to-digital Converter.

8. Instruction set summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
ARITHMETIC AND LOGIC INSTRUCTIONS					
ADD	Rd, Rr	Add two Registers	$Rd \leftarrow Rd + Rr$	Z,C,N,V,H	1
ADC	Rd, Rr	Add with Carry two Registers	$Rd \leftarrow Rd + Rr + C$	Z,C,N,V,H	1
ADIW	RdI,K	Add Immediate to Word	$Rdh:Rdl \leftarrow Rdh:Rdl + K$	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract two Registers	$Rd \leftarrow Rd - Rr$	Z,C,N,V,H	1
SUBI	Rd, K	Subtract Constant from Register	$Rd \leftarrow Rd - K$	Z,C,N,V,H	1
SBC	Rd, Rr	Subtract with Carry two Registers	$Rd \leftarrow Rd - Rr - C$	Z,C,N,V,H	1
SBCI	Rd, K	Subtract with Carry Constant from Reg.	$Rd \leftarrow Rd - K - C$	Z,C,N,V,H	1
SBIW	RdI,K	Subtract Immediate from Word	$Rdh:Rdl \leftarrow Rdh:Rdl - K$	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND Registers	$Rd \leftarrow Rd \bullet Rr$	Z,N,V	1
ANDI	Rd, K	Logical AND Register and Constant	$Rd \leftarrow Rd \bullet K$	Z,N,V	1
OR	Rd, Rr	Logical OR Registers	$Rd \leftarrow Rd \vee Rr$	Z,N,V	1
ORI	Rd, K	Logical OR Register and Constant	$Rd \leftarrow Rd \vee K$	Z,N,V	1
EOR	Rd, Rr	Exclusive OR Registers	$Rd \leftarrow Rd \oplus Rr$	Z,N,V	1
COM	Rd	One's Complement	$Rd \leftarrow 0xFF - Rd$	Z,C,N,V	1
NEG	Rd	Two's Complement	$Rd \leftarrow 0x00 - Rd$	Z,C,N,V,H	1
SBR	Rd,K	Set Bit(s) in Register	$Rd \leftarrow Rd \vee K$	Z,N,V	1
CBR	Rd,K	Clear Bit(s) in Register	$Rd \leftarrow Rd \bullet (0xFF - K)$	Z,N,V	1
INC	Rd	Increment	$Rd \leftarrow Rd + 1$	Z,N,V	1
DEC	Rd	Decrement	$Rd \leftarrow Rd - 1$	Z,N,V	1
TST	Rd	Test for Zero or Minus	$Rd \leftarrow Rd \bullet Rd$	Z,N,V	1
CLR	Rd	Clear Register	$Rd \leftarrow Rd \oplus Rd$	Z,N,V	1
SER	Rd	Set Register	$Rd \leftarrow 0xFF$	None	1
MUL	Rd, Rr	Multiply Unsigned	$R1:R0 \leftarrow Rd \times Rr$	Z,C	2
MULS	Rd, Rr	Multiply Signed	$R1:R0 \leftarrow Rd \times Rr$	Z,C	2
MULSU	Rd, Rr	Multiply Signed with Unsigned	$R1:R0 \leftarrow Rd \times Rr$	Z,C	2
FMUL	Rd, Rr	Fractional Multiply Unsigned	$R1:R0 \leftarrow (Rd \times Rr) \ll 1$	Z,C	2
FMULS	Rd, Rr	Fractional Multiply Signed	$R1:R0 \leftarrow (Rd \times Rr) \ll 1$	Z,C	2
FMULSU	Rd, Rr	Fractional Multiply Signed with Unsigned	$R1:R0 \leftarrow (Rd \times Rr) \ll 1$	Z,C	2
BRANCH INSTRUCTIONS					
RJMP	k	Relative Jump	$PC \leftarrow PC + k + 1$	None	2
IJMP		Indirect Jump to (Z)	$PC \leftarrow Z$	None	2
JMP	k	Direct Jump	$PC \leftarrow k$	None	3
RCALL	k	Relative Subroutine Call	$PC \leftarrow PC + k + 1$	None	3
ICALL		Indirect Call to (Z)	$PC \leftarrow Z$	None	3
CALL	k	Direct Subroutine Call	$PC \leftarrow k$	None	4
RET		Subroutine Return	$PC \leftarrow STACK$	None	4
RETI		Interrupt Return	$PC \leftarrow STACK$	I	4
CPSE	Rd,Rr	Compare, Skip if Equal	if $(Rd = Rr)$ $PC \leftarrow PC + 2$ or 3	None	1/2/3
CP	Rd,Rr	Compare	$Rd - Rr$	Z, N,V,C,H	1
CPC	Rd,Rr	Compare with Carry	$Rd - Rr - C$	Z, N,V,C,H	1
CPI	Rd,K	Compare Register with Immediate	$Rd - K$	Z, N,V,C,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if $(Rr(b)=0)$ $PC \leftarrow PC + 2$ or 3	None	1/2/3
SBRSC	Rr, b	Skip if Bit in Register is Set	if $(Rr(b)=1)$ $PC \leftarrow PC + 2$ or 3	None	1/2/3
SBIC	P, b	Skip if Bit in I/O Register Cleared	if $(P(b)=0)$ $PC \leftarrow PC + 2$ or 3	None	1/2/3
SBIS	P, b	Skip if Bit in I/O Register is Set	if $(P(b)=1)$ $PC \leftarrow PC + 2$ or 3	None	1/2/3
BRBS	s, k	Branch if Status Flag Set	if $(SREG(s) = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRBC	s, k	Branch if Status Flag Cleared	if $(SREG(s) = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BREQ	k	Branch if Equal	if $(Z = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRNE	k	Branch if Not Equal	if $(Z = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRCS	k	Branch if Carry Set	if $(C = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRCC	k	Branch if Carry Cleared	if $(C = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRSH	k	Branch if Same or Higher	if $(C = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRLO	k	Branch if Lower	if $(C = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRMI	k	Branch if Minus	if $(N = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRPL	k	Branch if Plus	if $(N = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRGE	k	Branch if Greater or Equal, Signed	if $(N \oplus V = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRLT	k	Branch if Less Than Zero, Signed	if $(N \oplus V = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRHS	k	Branch if Half Carry Flag Set	if $(H = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRHC	k	Branch if Half Carry Flag Cleared	if $(H = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRTS	k	Branch if T Flag Set	if $(T = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRTC	k	Branch if T Flag Cleared	if $(T = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRVS	k	Branch if Overflow Flag is Set	if $(V = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2

Mnemonics	Operands	Description	Operation	Flags	#Clocks
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then PC ← PC + k + 1	None	1/2
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then PC ← PC + k + 1	None	1/2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then PC ← PC + k + 1	None	1/2
BIT AND BIT-TEST INSTRUCTIONS					
SBI	P,b	Set Bit in I/O Register	I/O(P,b) ← 1	None	2
CBI	P,b	Clear Bit in I/O Register	I/O(P,b) ← 0	None	2
LSL	Rd	Logical Shift Left	Rd(n+1) ← Rd(n), Rd(0) ← 0	Z,C,N,V	1
LSR	Rd	Logical Shift Right	Rd(n) ← Rd(n+1), Rd(7) ← 0	Z,C,N,V	1
ROL	Rd	Rotate Left Through Carry	Rd(0) ← C, Rd(n+1) ← Rd(n), C ← Rd(7)	Z,C,N,V	1
ROR	Rd	Rotate Right Through Carry	Rd(7) ← C, Rd(n) ← Rd(n+1), C ← Rd(0)	Z,C,N,V	1
ASR	Rd	Arithmetic Shift Right	Rd(n) ← Rd(n+1), n=0..6	Z,C,N,V	1
SWAP	Rd	Swap Nibbles	Rd(3..0) ← Rd(7..4), Rd(7..4) ← Rd(3..0)	None	1
BSET	s	Flag Set	SREG(s) ← 1	SREG(s)	1
BCLR	s	Flag Clear	SREG(s) ← 0	SREG(s)	1
BST	Rr, b	Bit Store from Register to T	T ← Rr(b)	T	1
BLD	Rd, b	Bit load from T to Register	Rd(b) ← T	None	1
SEC		Set Carry	C ← 1	C	1
CLC		Clear Carry	C ← 0	C	1
SEN		Set Negative Flag	N ← 1	N	1
CLN		Clear Negative Flag	N ← 0	N	1
SEZ		Set Zero Flag	Z ← 1	Z	1
CLZ		Clear Zero Flag	Z ← 0	Z	1
SEI		Global Interrupt Enable	I ← 1	I	1
CLI		Global Interrupt Disable	I ← 0	I	1
SES		Set Signed Test Flag	S ← 1	S	1
CLS		Clear Signed Test Flag	S ← 0	S	1
SEV		Set Twos Complement Overflow.	V ← 1	V	1
CLV		Clear Twos Complement Overflow	V ← 0	V	1
SET		Set T in SREG	T ← 1	T	1
CLT		Clear T in SREG	T ← 0	T	1
SEH		Set Half Carry Flag in SREG	H ← 1	H	1
CLH		Clear Half Carry Flag in SREG	H ← 0	H	1
DATA TRANSFER INSTRUCTIONS					
MOV	Rd, Rr	Move Between Registers	Rd ← Rr	None	1
MOVW	Rd, Rr	Copy Register Word	Rd+1:Rd ← Rr+1:Rr	None	1
LDI	Rd, K	Load Immediate	Rd ← K	None	1
LD	Rd, X	Load Indirect	Rd ← (X)	None	2
LD	Rd, X+	Load Indirect and Post-Inc.	Rd ← (X), X ← X + 1	None	2
LD	Rd, -X	Load Indirect and Pre-Dec.	X ← X - 1, Rd ← (X)	None	2
LD	Rd, Y	Load Indirect	Rd ← (Y)	None	2
LD	Rd, Y+	Load Indirect and Post-Inc.	Rd ← (Y), Y ← Y + 1	None	2
LD	Rd, -Y	Load Indirect and Pre-Dec.	Y ← Y - 1, Rd ← (Y)	None	2
LDD	Rd,Y+q	Load Indirect with Displacement	Rd ← (Y + q)	None	2
LD	Rd, Z	Load Indirect	Rd ← (Z)	None	2
LD	Rd, Z+	Load Indirect and Post-Inc.	Rd ← (Z), Z ← Z + 1	None	2
LD	Rd, -Z	Load Indirect and Pre-Dec.	Z ← Z - 1, Rd ← (Z)	None	2
LDD	Rd, Z+q	Load Indirect with Displacement	Rd ← (Z + q)	None	2
LDS	Rd, k	Load Direct from SRAM	Rd ← (k)	None	2
ST	X, Rr	Store Indirect	(X) ← Rr	None	2
ST	X+, Rr	Store Indirect and Post-Inc.	(X) ← Rr, X ← X + 1	None	2
ST	-X, Rr	Store Indirect and Pre-Dec.	X ← X - 1, (X) ← Rr	None	2
ST	Y, Rr	Store Indirect	(Y) ← Rr	None	2
ST	Y+, Rr	Store Indirect and Post-Inc.	(Y) ← Rr, Y ← Y + 1	None	2
ST	-Y, Rr	Store Indirect and Pre-Dec.	Y ← Y - 1, (Y) ← Rr	None	2
STD	Y+q,Rr	Store Indirect with Displacement	(Y + q) ← Rr	None	2
ST	Z, Rr	Store Indirect	(Z) ← Rr	None	2
ST	Z+, Rr	Store Indirect and Post-Inc.	(Z) ← Rr, Z ← Z + 1	None	2
ST	-Z, Rr	Store Indirect and Pre-Dec.	Z ← Z - 1, (Z) ← Rr	None	2
STD	Z+q,Rr	Store Indirect with Displacement	(Z + q) ← Rr	None	2
STS	k, Rr	Store Direct to SRAM	(k) ← Rr	None	2
LPM		Load Program Memory	R0 ← (Z)	None	3
LPM	Rd, Z	Load Program Memory	Rd ← (Z)	None	3
LPM	Rd, Z+	Load Program Memory and Post-Inc	Rd ← (Z), Z ← Z + 1	None	3
SPM		Store Program Memory	(Z) ← R1:R0	None	-
IN	Rd, P	In Port	Rd ← P	None	1
OUT	P, Rr	Out Port	P ← Rr	None	1
PUSH	Rr	Push Register on Stack	STACK ← Rr	None	2
POP	Rd	Pop Register from Stack	Rd ← STACK	None	2

Mnemonics	Operands	Description	Operation	Flags	#Clocks
MCU CONTROL INSTRUCTIONS					
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep function)	None	1
WDR		Watchdog Reset	(see specific descr. for WDR/timer)	None	1
BREAK		Break	For On-chip Debug Only	None	N/A

9. Ordering information

9.1 Atmel ATmega164A

Speed [MHz] ⁽³⁾	Power supply	Ordering code ⁽²⁾	Package ⁽¹⁾	Operational range
20	1.8 - 5.5V	ATmega164A-AU	44A	Industrial (-40°C to 85°C)
		ATmega164A-AUR ⁽⁵⁾	44A	
		ATmega164A-PU	40P6	
		ATmega164A-MU	44M1	
		ATmega164A-MUR ⁽⁵⁾	44M1	
		ATmega164A-MCH ⁽⁴⁾	44MC	
		ATmega164A-MCHR ⁽⁴⁾⁽⁵⁾	44MC	
		ATmega164A-CU	49C2	
		ATmega164A-CUR ⁽⁵⁾	49C2	

- Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
 2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
 3. For Speed vs. V_{CC} see ["Speed grades" on page 324](#).
 4. NiPdAu Lead Finish.
 5. Tape & Reel.

Package Type	
44A	44-lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP)
40P6	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)
44M1	44-pad, 7 × 7 × 1.0mm body, lead pitch 0.50mm, Thermally Enhanced Plastic Very Thin Quad Flat No-Lead (VQFN)
44MC	44-lead (2-row Staggered), 5 × 5 × 1.0mm body, 2.60 × 2.60mm Exposed Pad, Quad Flat No-Lead Package (QFN)
49C2	49-ball, (7 × 7 Array) 0.65mm Pitch, 5 × 5 × 1mm, Very Thin, Fine-Pitch Ball Grid Array Package (VFBGA)

9.2 Atmel ATmega164PA

Speed [MHz] ⁽³⁾	Power supply	Ordering code ⁽²⁾	Package ⁽¹⁾	Operational range
20	1.8 - 5.5V	ATmega164PA-AU	44A	Industrial (-40°C to 85°C)
		ATmega164PA-AUR ⁽⁵⁾	44A	
		ATmega164PA-PU	40P6	
		ATmega164PA-MU	44M1	
		ATmega164PA-MUR ⁽⁵⁾	44M1	
		ATmega164PA-MCH ⁽⁴⁾	44MC	
		ATmega164PA-MCHR ⁽⁴⁾⁽⁵⁾	44MC	
		ATmega164PA-CU	49C2	
		ATmega164PA-CUR ⁽⁵⁾	49C2	
20	1.8 - 5.5V	ATmega164PA-AN	44A	Industrial (-40°C to 105°C)
		ATmega164PA-ANR ⁽⁵⁾	44A	
		ATmega164PA-PN	40P6	
		ATmega164PA-MN	44M1	
		ATmega164PA-MNR ⁽⁵⁾	44M1	

- Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
 2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
 3. For Speed vs. V_{CC} see ["Speed grades" on page 324](#).
 4. NiPdAu Lead Finish.
 5. Tape & Reel.

Package Type	
44A	44-lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP)
40P6	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)
44M1	44-pad, 7 × 7 × 1.0mm body, lead pitch 0.50mm, Thermally Enhanced Plastic Very Thin Quad Flat No-Lead (VQFN)
44MC	44-lead (2-row Staggered), 5 × 5 × 1.0mm body, 2.60 × 2.60mm Exposed Pad, Quad Flat No-Lead Package (QFN)
49C2	49-ball, (7 × 7 Array) 0.65mm Pitch, 5 × 5 × 1mm, Very Thin, Fine-Pitch Ball Grid Array Package (VFBGA)

9.5 Atmel ATmega644A

Speed [MHz] ⁽³⁾	Power supply	Ordering code ⁽²⁾	Package ⁽¹⁾	Operational range
20	1.8 - 5.5V	ATmega644A-AU ATmega644A-AUR ⁽⁴⁾ ATmega644A-PU ATmega644A-MU ATmega644A-MUR ⁽⁴⁾	44A 44A 40P6 44M1 44M1	Industrial (-40°C to 85°C)

- Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
 2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
 3. For Speed vs. V_{CC} see ["Speed grades" on page 324](#).
 4. Taper & Reel.

Package Type	
44A	44-lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP)
40P6	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)
44M1	44-pad, 7 × 7 × 1.0mm body, lead pitch 0.5 mm, Thermally Enhanced Plastic Very Thin Quad Flat No-Lead (VQFN)

9.6 Atmel ATmega644PA

Speed [MHz] ⁽³⁾	Power supply	Ordering code ⁽²⁾	Package ⁽¹⁾	Operational range
20	1.8 - 5.5V	ATmega644PA-AU ATmega644PA-AUR ⁽⁴⁾ ATmega644PA-PU ATmega644PA-MU ATmega644PA-MUR ⁽⁴⁾	44A 44A 40P6 44M1 44M1	Industrial (-40°C to 85°C)
20	1.8 - 5.5V	ATmega644PA-AN ATmega644PA-ANR ⁽⁴⁾ ATmega644PA-PN ATmega644PA-MN ATmega644PA-MNR ⁽⁴⁾	44A 44A 40P6 44M1 44M1	Industrial (-40°C to 105°C)

- Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
 2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
 3. For Speed vs. V_{CC} see ["Speed grades" on page 324](#).
 4. Taper & Reel.

Package Type	
44A	44-lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP)
40P6	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)
44M1	44-pad, 7 × 7 × 1.0mm body, lead pitch 0.50mm, Thermally Enhanced Plastic Very Thin Quad Flat No-Lead (VQFN)

9.7 Atmel ATmega1284

Speed [MHz] ⁽³⁾	Power supply	Ordering code ⁽²⁾	Package ⁽¹⁾	Operational range
20	1.8 - 5.5V	ATmega1284-AU ATmega1284-AUR ⁽⁴⁾ ATmega1284-PU ATmega1284-MU ATmega1284-MUR ⁽⁴⁾	44A 44A 40P6 44M1 44M1	Industrial (-40°C to 85°C)

- Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
 2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
 3. For Speed vs. V_{CC} see ["Speed grades" on page 324](#).
 4. Tape & Reel.

Package Type	
44A	44-lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP)
40P6	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)
44M1	44-pad, 7 × 7 × 1.0mm body, lead pitch 0.50mm, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)

9.8 Atmel ATmega1284P

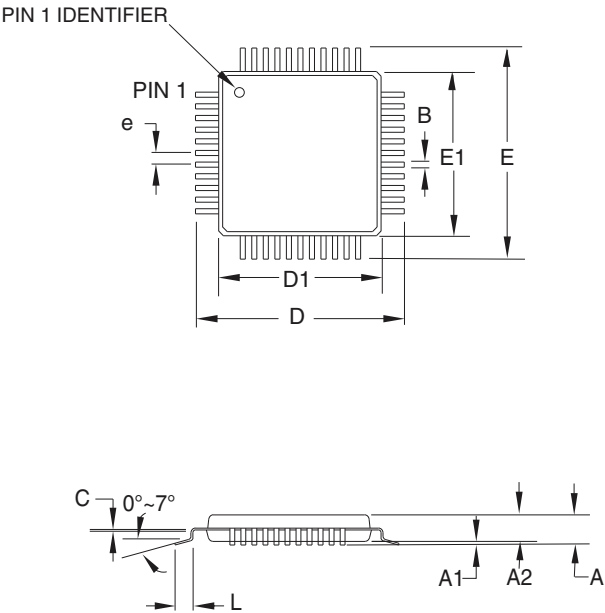
Speed [MHz] ⁽³⁾	Power supply	Ordering code ⁽²⁾	Package ⁽¹⁾	Operational range
20	1.8 - 5.5V	ATmega1284P-AU ATmega1284P-AUR ⁽⁴⁾ ATmega1284P-PU ATmega1284P-MU ATmega1284P-MUR ⁽⁴⁾	44A 44A 40P6 44M1 44M1	Industrial (-40°C to 85°C)
20	1.8 - 5.5V	ATmega1284P-AN ATmega1284P-ANR ⁽⁴⁾ ATmega1284P-PN ATmega1284P-MN ATmega1284P-MNR ⁽⁴⁾	44A 44A 40P6 44M1 44M1	Industrial (-40°C to 105°C)

- Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
 2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
 3. For Speed vs. V_{CC} see ["Speed grades" on page 324](#).
 4. Tape & Reel.

Package Type	
44A	44-lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP)
40P6	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)
44M1	44-pad, 7 × 7 × 1.0mm body, lead pitch 0.50mm, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)

10. Packaging information

10.1 44A



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	11.75	12.00	12.25	
D1	9.90	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
B	0.30	0.37	0.45	
C	0.09	(0.17)	0.20	
L	0.45	0.60	0.75	
e	0.80 TYP			

- Notes:
- 1. This package conforms to JEDEC reference MS-026, Variation ACB.
 - 2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
 - 3. Lead coplanarity is 0.10mm maximum.

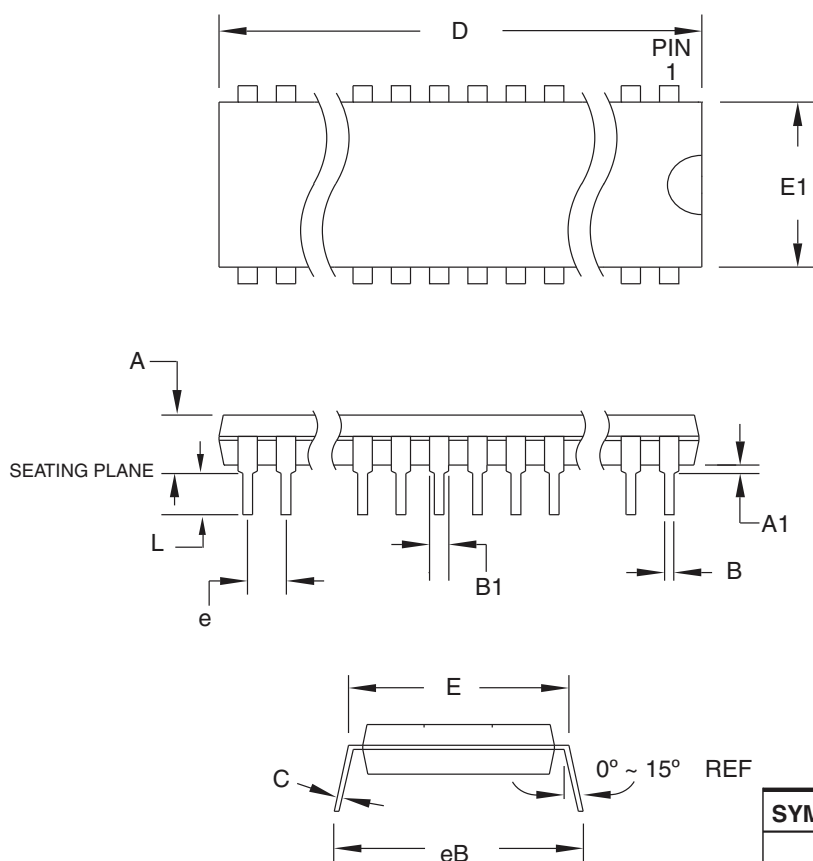
06/02/2014

Atmel® Package Drawing Contact:
packagedrawings@atmel.com

TITLE
44A, 44-lead, 10 x 10mm body size, 1.0mm body thickness,
0.8 mm lead pitch, thin profile plastic quad flat package (TQFP)

DRAWING NO.	REV.
44A	C

10.2 40P6




COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	—	—	4.826	
A1	0.381	—	—	
D	52.070	—	52.578	Note 2
E	15.240	—	15.875	
E1	13.462	—	13.970	Note 2
B	0.356	—	0.559	
B1	1.041	—	1.651	
L	3.048	—	3.556	
C	0.203	—	0.381	
eB	15.494	—	17.526	
e	2.540 TYP			

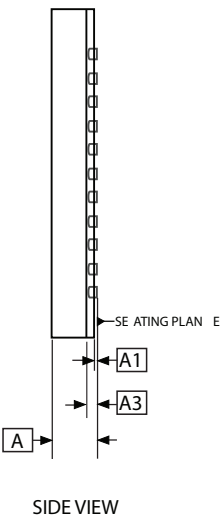
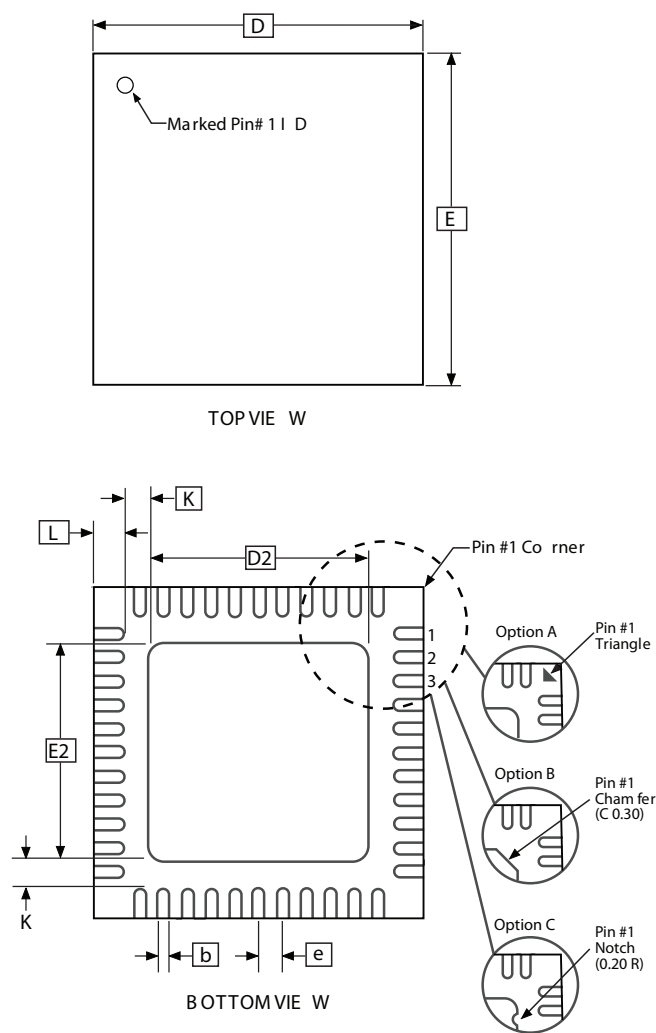
Notes:

1. This package conforms to JEDEC reference MS-011, Variation AC.
2. Dimensions D and $E1$ do not include mold Flash or Protrusion.
Mold Flash or Protrusion shall not exceed 0.25mm (0.010").

13/02/2014

 Package Drawing Contact: packagedrawings@atmel.com	TITLE 40P6, 40-lead (0.600"/15.24mm Wide) Plastic Dual Inline Package (PDIP)	DRAWING NO.	REV.
		40P6	C

10.3 44M1




COMMON DIMENSIONS
(Unit of Measure = mm)

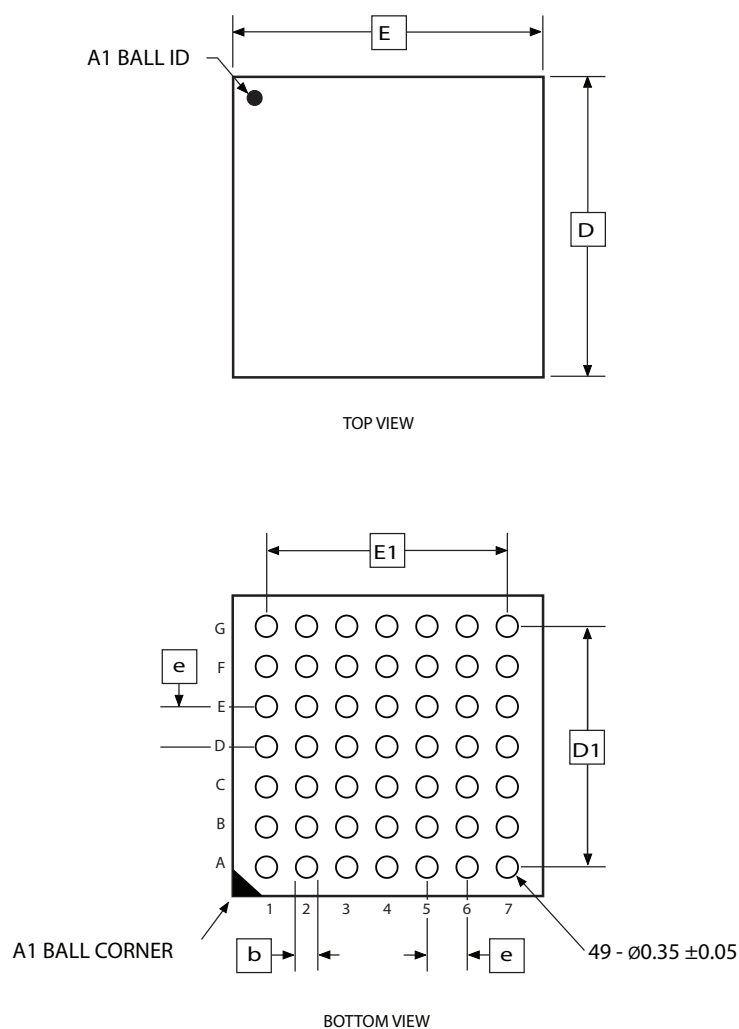
SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	—	0.02	0.05	
A3	0.20 REF			
b	0.18	0.23	0.30	
D	6.90	7.00	7.10	
D2	5.00	5.20	5.40	
E	6.90	7.00	7.10	
E2	5.00	5.20	5.40	
e	0.50 BSC			
L	0.59	0.64	0.69	
K	0.20	0.26	0.41	

Note: JEDEC Standard MO-220, Fig . 1 (S AW Singulation) VKKD-3 .

9/26/08

 Package Drawing Contact: avr@atmel.com	TITLE 44M1, 44-pad, 7 x 7 x 1.0mm body, lead pitch 0.50mm, 5.20mm exposed pad, thermally enhanced plastic very thin quad flat no lead package (VQFN)	GPC	DRAWING NO.	REV.
		ZWS	44M1	H

10.5 49C2



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	—	—	1.00	
A1	0.20	—	—	
A2	0.65	—	—	
D	4.90	5.00	5.10	
D1	3.90 BSC			
E4.90	5.00	5.10		
E1	3.90 BSC			
b	0.30	0.35	0.40	
e	0.65 BSC			

3/14/08



Package Drawing Contact:
packagedrawings@atmel.com

TITLE
49C2, 49-ball (7 x 7 array), 0.65mm pitch,
5.0 x 5.0 x 1.0mm, very thin, fine-pitch
ball grid array package (VFBGA)

GPC
CBD

DRAWING NO.
49C2

REV.
A

12. Datasheet revision history

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

12.1 Rev. 8272G - 01/2015

1. Updated [Table 1-2 on page 5](#), [Table 8-1 on page 25](#), [Table 10-1 on page 42](#), [Table 14-3 on page 79](#), [Table 19-4 on page 187](#), [Table 19-11 on page 192](#) and [Table 28-16 on page 328](#) for formatting consistency errors
2. Updated ["Ordering information" on page 17](#):
 - Added ordering information for ATmega164PA @105°C; ATmega324PA @ 105°C; ATmega324PA @105°C; ATmega644PA @ 105°C and ATmega1284P @ 105°C
3. Updated the ["Packaging information" on page 25](#):
 - Replaced the drawing ["44M1" on page 27](#) by a correct package

12.2 Rev. 8272F - 08/2014

1. Updated text in [Section 13.2.8 "PCMSK1 – Pin Change Mask Register 1" on page 70](#) to: "If PCINT15:8 is set and the PCIE1 bit in PCICR is set, pin change interrupt is enabled on the corresponding I/O pin."
2. Corrected description of PAGESMB in [Table 26-9 on page 281](#). The device has 64 words in a page and not 128.
3. Corrected description of PAGESMB in [Table 26-12 on page 282](#). PAGESMB is 5 and the device has 64 words in a page and not 128. The page require six bits and not seven.
4. Corrected values in [Table 26-16 on page 284](#). PAGESMB is 6. ZPAGESMB is Z7 and PCPAGE is Z15:Z8
5. Corrected value for PCPAGE in [Table 27-7 on page 290](#). The correct value is PC[14:7]
6. Updated description in [Table 17-2 on page 151](#) to "Normal port operation, OC2A disconnected."
7. Updated Assembly code examples on for ["Watchdog Timer" on page 55](#). and onwards
 - "out WDTCR, r16" changed to "sts WDTCR, r16"
 - "in r16, WDTCR" changed to "lds r16, WDTCR"
 - "ldi r16, WDTCR" changed to "lds r16, WDTCR"
8. Updated addresses 0x65 and 0x64 in [Section 7. "Register summary" on page 10](#).
9. Removed notes 5 and 6 from [Table 28-16 on page 328](#).
10. Corrected values in [Section 8. "Instruction set summary" on page 14](#). Changed clock values for RCALL and ICALL to 2, for Call, Ret and RETI to 4. Also changed values in [Section 7.7.1 "Interrupt response time" on page 18](#).
11. Updated layout, footer and back page according to template 0205/2014

12. Added "OCR3AH and OCR3AL – Output Compare Register3 A" on page 133
13. Added "OCR3BH and OCR3BL – Output Compare Register3 B" on page 133
14. Added "TIMSK3 – Timer/Counter3 Interrupt Mask Register" on page 134
15. Updated All "SPI – Serial Peripheral Interface" "Register description" to reflect ATmega1284 and ATmega1284P.
16. Updated "Addressing the Flash During Self-Programming" on page 274 to include RAMPZ register.
17. Updated Table 27-16 on page 303. t_{WD_EEPROM} is 3.6ms instead of 9ms.
18. BODS and BODSE bits denoted as R/W
19. Description of external pin modes below table 16-9 removed.
20. Updated "Register summary" on page 10 to include Timer/Counter3.
21. Updated the datasheet with Atmel new style guide.

12.7 Rev. 8272A - 01/10

1. Initial revision (Based on the ATmega164PA/324PA/644PA/1284P datasheet 8252G-AVR-11/09 and on the ATmega644 datasheet 2593N-AVR-09/09).
2. Changes done:
 - Non-picoPower devices added: ATmega164A/324A/644A/1284
 - Updated Table 2-1 on page 7
 - Updated Table 10-1 on page 42
 - Updated "Sleep Modes" on page 42 and "BOD disable⁽¹⁾" on page 43
 - Updated "Register description" on page 67
 - Updated "USART" on page 167 and "USART in SPI mode" on page 194
 - Updated "Signature Bytes" on page 290 and "Page Size" on page 290
 - Added "DC Characteristics" on page 318 for non-picoPower devices.
 - Added "Atmel ATmega164A typical characteristics" on page 333
 - Added "Atmel ATmega324A typical characteristics" on page 386
 - Added "Atmel ATmega644A typical characteristics" on page 438
 - Added "ATmega1284 typical characteristics" on page 490
 - Added "Ordering information" on page 17 for non-picoPower devices
 - Added "Errata for ATmega164A" on page 30
 - Added "Errata for ATmega324A" on page 30
 - Added "Errata for ATmega644PA" on page 30
 - Added "Errata for ATmega1284" on page 30