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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

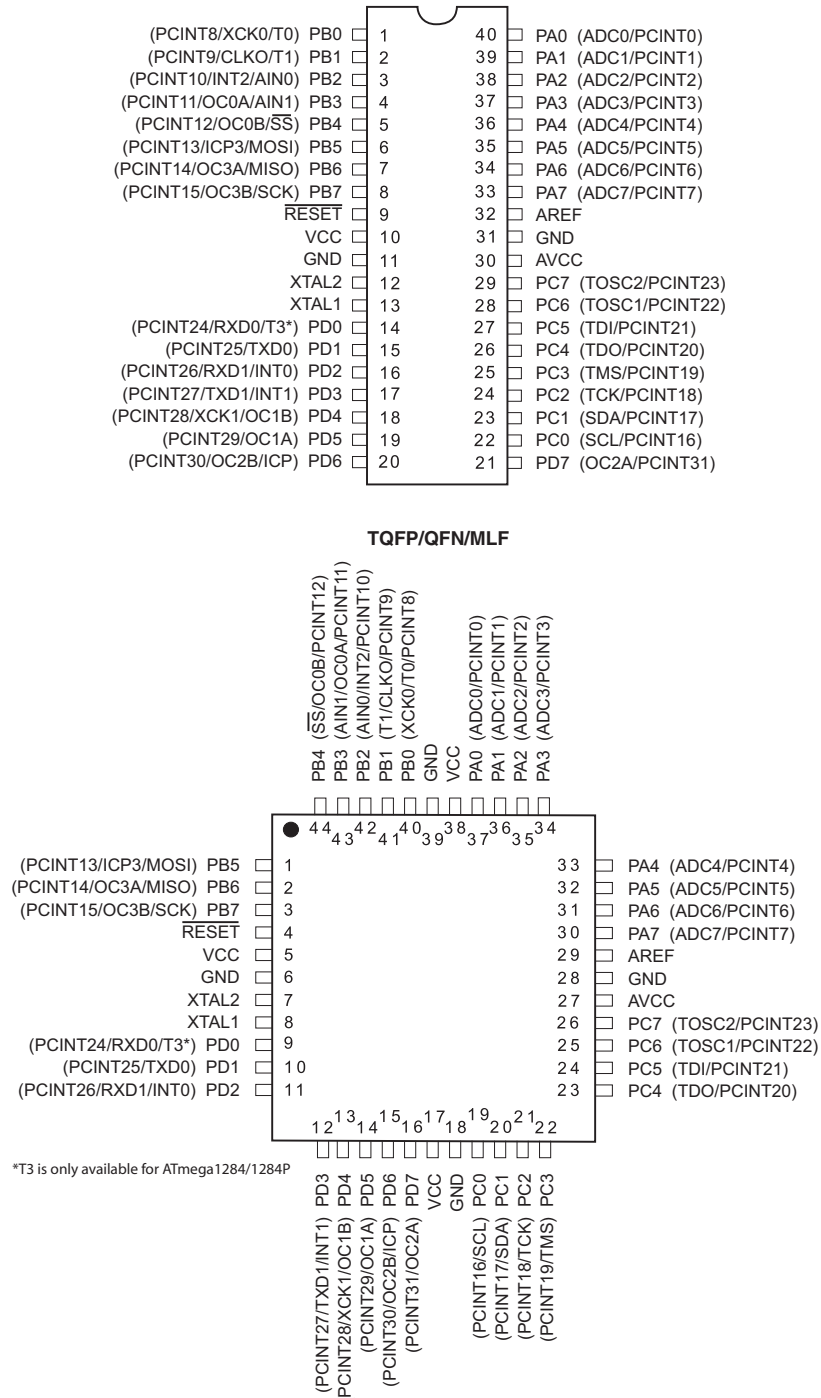
Details

Product Status	Active
Core Processor	AVR
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	32
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Dual Rows, Exposed Pad
Supplier Device Package	44-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/atmel/atmega164a-mch

1. Pin configurations

1.1 Pinout - PDIP/TQFP/VQFN/QFN/MLF for ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P

Figure 1-1. Pinout.



Note: The large center pad underneath the VQFN/QFN/MLF package should be soldered to ground on the board to ensure good mechanical stability.

1.2 Pinout - DRQFN for Atmel ATmega164A/164PA/324A/324PA

Figure 1-2. DRQFN - pinout.

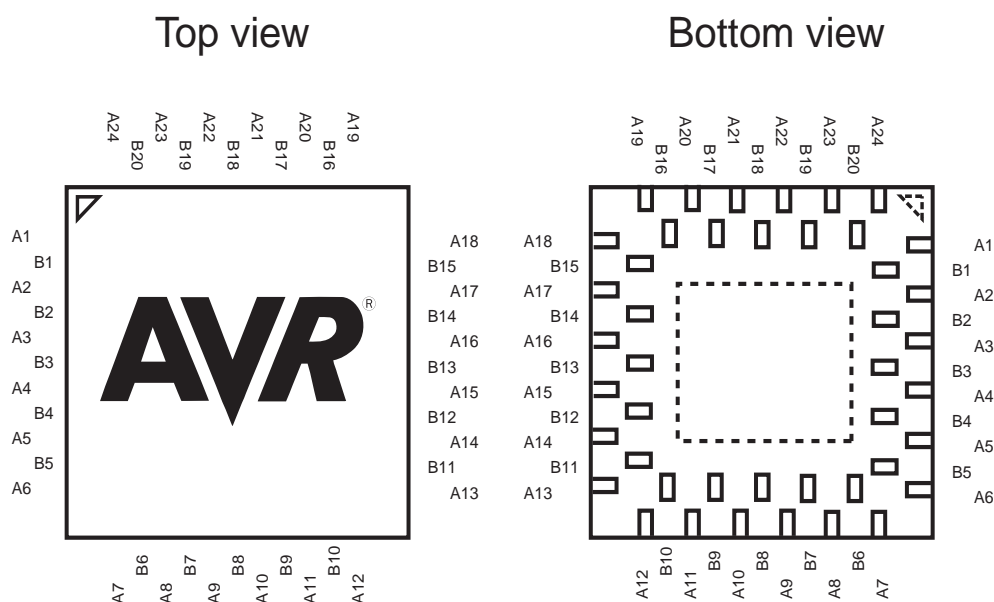
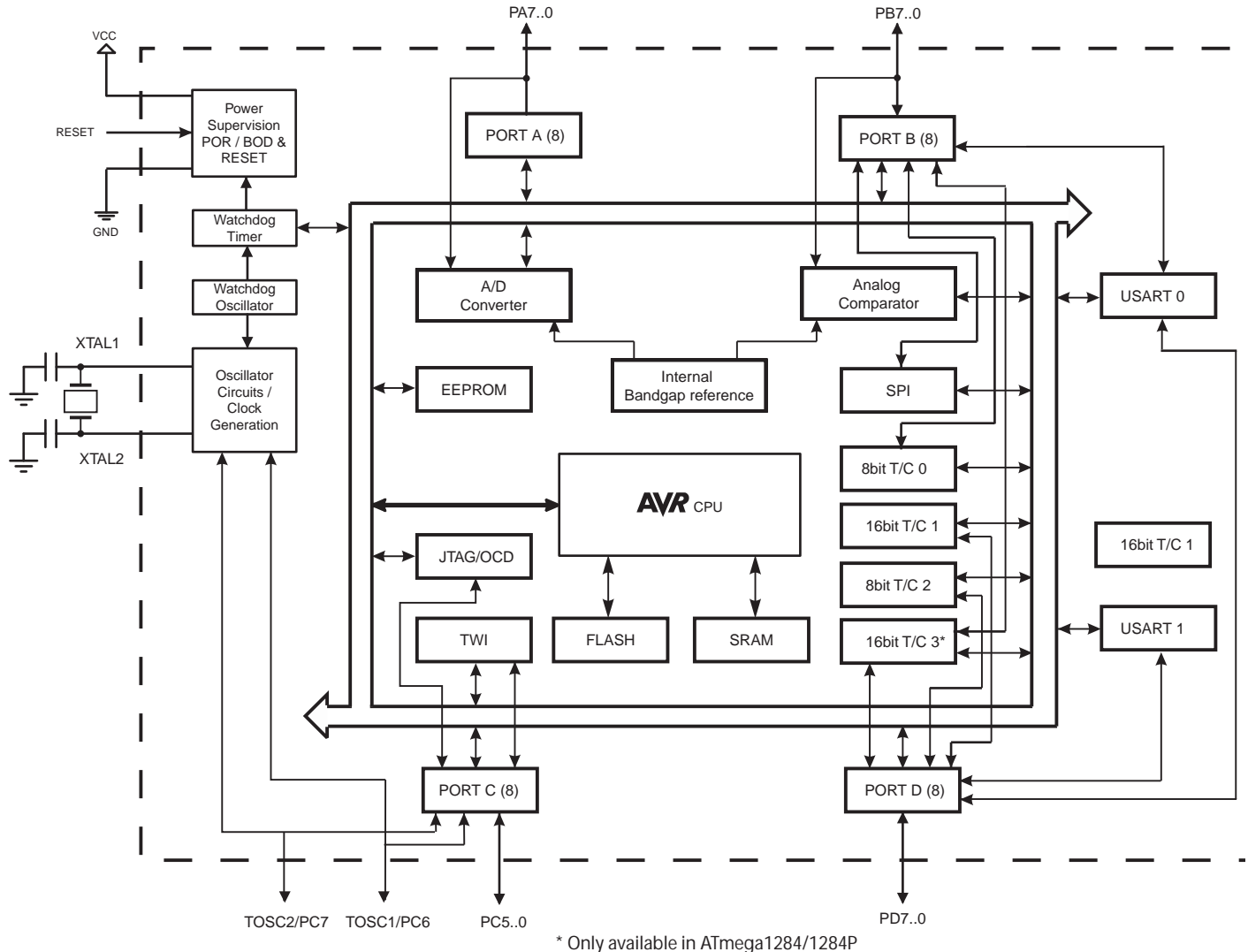


Table 1-1. DRQFN - pinout.

A1	PB5	A7	PD3	A13	PC4	A19	PA3
B1	PB6	B6	PD4	B11	PC5	B16	PA2
A2	PB7	A8	PD5	A14	PC6	A20	PA1
B2	RESET	B7	PD6	B12	PC7	B17	PA0
A3	VCC	A9	PD7	A15	AVCC	A21	VCC
B3	GND	B8	VCC	B13	GND	B18	GND
A4	XTAL2	A10	GND	A16	AREF	A22	PB0
B4	XTAL1	B9	PC0	B14	PA7	B19	PB1
A5	PD0	A11	PC1	A17	PA6	A23	PB2
B5	PD1	B10	PC2	B15	PA5	B20	PB3
A6	PD2	A12	PC3	A18	PA4	A24	PB4

2.1 Block diagram

Figure 2-1. Block diagram.



The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The Atmel ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P provide the following features:

16/32/64/128Kbytes of In-System Programmable Flash with Read-While-Write capabilities, 512/1K/2K/4Kbytes EEPROM, 1/2/4/16Kbytes SRAM, 32 general purpose I/O lines, 32 general purpose working registers, Real Time Counter (RTC), three (four for ATmega1284/1284P) flexible Timer/Counters with compare modes and PWM, 2 USARTs, a byte oriented two-wire Serial Interface, a 8-channel, 10-bit ADC with optional differential input stage with programmable gain, programmable Watchdog Timer with Internal Oscillator, an SPI serial port, IEEE std. 1149.1 compliant JTAG test interface, also used for accessing the On-chip Debug system and programming and six software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, SPI port, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next interrupt or Hardware Reset. In Power-save mode, the asynchronous timer continues to run, allowing the user to maintain a

2.3.3 Port A (PA7:PA0)

Port A serves as analog inputs to the Analog-to-digital Converter.

Port A also serves as an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port A output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port A pins that are externally pulled low will source current if the pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port A also serves the functions of various special features of the Atmel ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P as listed on [page 79](#).

2.3.4 Port B (PB7:PB0)

Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B also serves the functions of various special features of the ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P as listed on [page 80](#).

2.3.5 Port C (PC7:PC0)

Port C is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port C also serves the functions of the JTAG interface, along with special features of the Atmel ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P as listed on [page 83](#).

2.3.6 Port D (PD7:PD0)

Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port D also serves the functions of various special features of the ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P as listed on [page 86](#).

2.3.7 RESET

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in [" on page 325](#). Shorter pulses are not guaranteed to generate a reset.

2.3.8 XTAL1

Input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

2.3.9 XTAL2

Output from the inverting Oscillator amplifier.

2.3.10 AVCC

AVCC is the supply voltage pin for Port A and the Analog-to-digital Converter. It should be externally connected to V_{CC} , even if the ADC is not used. If the ADC is used, it should be connected to V_{CC} through a low-pass filter.

2.3.11 AREF

This is the analog reference pin for the Analog-to-digital Converter.

3. Resources

A comprehensive set of development tools, application notes and datasheets are available for download on <http://www.atmel.com/avr>.

4. About code examples

This documentation contains simple code examples that briefly show how to use various parts of the device. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C compiler documentation for more details.

The code examples assume that the part specific header file is included before compilation. For I/O registers located in extended I/O map, "IN", "OUT", "SBIS", "SBIC", "CBI", and "SBI" instructions must be replaced with instructions that allow access to extended I/O. Typically "LDS" and "STS" combined with "SBR", "SBRC", "SBR", and "CBR".

5. Data retention

Reliability Qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C or 100 years at 25°C.

6. Capacitive touch sensing

The Atmel QTouch Library provides a simple to use solution to realize touch sensitive interfaces on most Atmel AVR microcontrollers. The QTouch Library includes support for the QTouch and QMatrix acquisition methods.

Touch sensing can be added to any application by linking the appropriate Atmel QTouch Library for the AVR Microcontroller. This is done by using a simple set of APIs to define the touch channels and sensors, and then calling the touch sensing API's to retrieve the channel information and determine the touch sensor states.

The QTouch Library is FREE and downloadable from the Atmel website at the following location: www.atmel.com/qtouchlibrary. For implementation details and other information, refer to the [Atmel QTouch Library User Guide](#) - also available for download from the Atmel website.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
(0xC0)	UCSR0A	RXC0	TXC0	UDRE0	FE0	DOR0	UPE0	U2X0	MPCM0	185/200
(0xBF)	Reserved	-	-	-	-	-	-	-	-	
(0xBE)	Reserved	-	-	-	-	-	-	-	-	
(0xBD)	TWAMR	TWAM6	TWAM5	TWAM4	TWAM3	TWAM2	TWAM1	TWAM0	-	231
(0xBC)	TWCR	TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	-	TWIE	228
(0xBB)	TWDR	two-wire Serial Interface Data Register								230
(0xBA)	TWAR	TWA6	TWA5	TWA4	TWA3	TWA2	TWA1	TWA0	TWGCE	231
(0xB9)	TWSR	TWS7	TWS6	TWS5	TWS4	TWS3	-	TWPS1	TWPS0	229
(0xB8)	TWBR	two-wire Serial Interface Bit Rate Register								228
(0xB7)	Reserved	-	-	-	-	-	-	-	-	
(0xB6)	ASSR	-	EXCLK	AS2	TCN2UB	OCR2AUB	OCR2BUB	TCR2AUB	TCR2BUB	155
(0xB5)	Reserved	-	-	-	-	-	-	-	-	
(0xB4)	OCR2B	Timer/Counter2 Output Compare Register B								155
(0xB3)	OCR2A	Timer/Counter2 Output Compare Register A								155
(0xB2)	TCNT2	Timer/Counter2 (8 Bit)								154
(0xB1)	TCCR2B	FOC2A	FOC2B	-	-	WGM22	CS22	CS21	CS20	153
(0xB0)	TCCR2A	COM2A1	COM2A0	COM2B1	COM2B0	-	-	WGM21	WGM20	151
(0xAF)	Reserved	-	-	-	-	-	-	-	-	
(0xAE)	Reserved	-	-	-	-	-	-	-	-	
(0xAD)	Reserved	-	-	-	-	-	-	-	-	
(0xAC)	Reserved	-	-	-	-	-	-	-	-	
(0xAB)	Reserved	-	-	-	-	-	-	-	-	
(0xAA)	Reserved	-	-	-	-	-	-	-	-	
(0xA9)	Reserved	-	-	-	-	-	-	-	-	
(0xA8)	Reserved	-	-	-	-	-	-	-	-	
(0xA7)	Reserved	-	-	-	-	-	-	-	-	
(0xA6)	Reserved	-	-	-	-	-	-	-	-	
(0xA5)	Reserved	-	-	-	-	-	-	-	-	
(0xA4)	Reserved	-	-	-	-	-	-	-	-	
(0xA3)	Reserved	-	-	-	-	-	-	-	-	
(0xA2)	Reserved	-	-	-	-	-	-	-	-	
(0xA1)	Reserved	-	-	-	-	-	-	-	-	
(0xA0)	Reserved	-	-	-	-	-	-	-	-	
(0x9F)	Reserved	-	-	-	-	-	-	-	-	
(0x9E)	Reserved	-	-	-	-	-	-	-	-	
(0x9D)	Reserved	-	-	-	-	-	-	-	-	
(0x9C)	Reserved	-	-	-	-	-	-	-	-	
(0x9B)	OCR3BH	Timer/Counter3 - Output Compare Register B High Byte ⁽⁷⁾								132
(0x9A)	OCR3BL	Timer/Counter3 - Output Compare Register B Low Byte ⁽⁷⁾								132
(0x99)	OCR3AH	Timer/Counter3 - Output Compare Register A High Byte ⁽⁷⁾								132
(0x98)	OCR3AL	Timer/Counter3 - Output Compare Register A Low Byte ⁽⁷⁾								132
(0x97)	ICR3H	Timer/Counter3 - Input Capture Register High Byte ⁽⁷⁾								133
(0x96)	ICR3L	Timer/Counter3 - Input Capture Register Low Byte ⁽⁷⁾								133
(0x95)	TCNT3H	Timer/Counter3 - Counter Register High Byte ⁽⁷⁾								132
(0x94)	TCNT3L	Timer/Counter3 - Counter Register Low Byte ⁽⁷⁾								132
(0x93)	Reserved	-	-	-	-	-	-	-	-	
(0x92)	TCCR3C	FOC3A	FOC3B	-	-	-	-	-	-	131
(0x91)	TCCR3B	ICNC3	ICES3	-	WGM33	WGM32	CS32	CS31	CS30	130
(0x90)	TCCR3A	COM3A1	COM3A0	COM3B1	COM3B0	-	-	WGM31	WGM30	128
(0x8F)	Reserved	-	-	-	-	-	-	-	-	
(0x8E)	Reserved	-	-	-	-	-	-	-	-	
(0x8D)	Reserved	-	-	-	-	-	-	-	-	
(0x8C)	Reserved	-	-	-	-	-	-	-	-	
(0x8B)	OCR1BH	Timer/Counter1 - Output Compare Register B High Byte								132
(0x8A)	OCR1BL	Timer/Counter1 - Output Compare Register B Low Byte								132
(0x89)	OCR1AH	Timer/Counter1 - Output Compare Register A High Byte								132
(0x88)	OCR1AL	Timer/Counter1 - Output Compare Register A Low Byte								132
(0x87)	ICR1H	Timer/Counter1 - Input Capture Register High Byte								133
(0x86)	ICR1L	Timer/Counter1 - Input Capture Register Low Byte								133
(0x85)	TCNT1H	Timer/Counter1 - Counter Register High Byte								132
(0x84)	TCNT1L	Timer/Counter1 - Counter Register Low Byte								132
(0x83)	Reserved	-	-	-	-	-	-	-	-	
(0x82)	TCCR1C	FOC1A	FOC1B	-	-	-	-	-	-	131
(0x81)	TCCR1B	ICNC1	ICES1	-	WGM13	WGM12	CS12	CS11	CS10	130
(0x80)	TCCR1A	COM1A1	COM1A0	COM1B1	COM1B0	-	-	WGM11	WGM10	128
(0x7F)	DIDR1	-	-	-	-	-	-	AIN1D	AIN0D	234
(0x7E)	DIDR0	ADC7D	ADC6D	ADC5D	ADC4D	ADC3D	ADC2D	ADC1D	ADC0D	253
(0x7D)	Reserved	-	-	-	-	-	-	-	-	

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x18 (0x38)	TIFR3	-	-	ICF3	-	-	OCF3B	OCF3A	TOV3	136
0x17 (0x37)	TIFR2	-	-	-	-	-	OCF2B	OCF2A	TOV2	156
0x16 (0x36)	TIFR1	-	-	ICF1	-	-	OCF1B	OCF1A	TOV1	135
0x15 (0x35)	TIFR0	-	-	-	-	-	OCF0B	OCF0A	TOV0	106
0x14 (0x34)	Reserved	-	-	-	-	-	-	-	-	
0x13 (0x33)	Reserved	-	-	-	-	-	-	-	-	
0x12 (0x32)	Reserved	-	-	-	-	-	-	-	-	
0x11 (0x31)	Reserved	-	-	-	-	-	-	-	-	
0x10 (0x30)	Reserved	-	-	-	-	-	-	-	-	
0x0F (0x2F)	Reserved	-	-	-	-	-	-	-	-	
0x0E (0x2E)	Reserved	-	-	-	-	-	-	-	-	
0x0D (0x2D)	Reserved	-	-	-	-	-	-	-	-	
0x0C (0x2C)	Reserved	-	-	-	-	-	-	-	-	
0x0B (0x2B)	PORTD	PORTD7	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	90
0x0A (0x2A)	DDRD	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	90
0x09 (0x29)	PIND	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	90
0x08 (0x28)	PORTC	PORTC7	PORTC6	PORTC5	PORTC4	PORTC3	PORTC2	PORTC1	PORTC0	90
0x07 (0x27)	DDRC	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	90
0x06 (0x26)	PINC	PINC7	PINC6	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0	90
0x05 (0x25)	PORTB	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	89
0x04 (0x24)	DDRB	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	89
0x03 (0x23)	PINB	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	90
0x02 (0x22)	PORTA	PORTA7	PORTA6	PORTA5	PORTA4	PORTA3	PORTA2	PORTA1	PORTA0	89
0x01 (0x21)	DDRA	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0	89
0x00 (0x20)	PINA	PINA7	PINA6	PINA5	PINA4	PINA3	PINA2	PINA1	PINA0	89

- Notes:
1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
 2. I/O registers within the address range \$00 - \$1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions.
 3. Some of the status flags are cleared by writing a logical one to them. Note that the CBI and SBI instructions will operate on all bits in the I/O register, writing a one back into any flag read as set, thus clearing the flag. The CBI and SBI instructions work with registers 0x00 to 0x1F only.
 4. When using the I/O specific commands IN and OUT, the I/O addresses \$00 - \$3F must be used. When addressing I/O registers as data space using LD and ST instructions, \$20 must be added to these addresses.
The ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P is a complex microcontroller with more peripheral units than can be supported within the 64 location reserved in Opcode for the IN and OUT instructions. For the Extended I/O space from \$60 - \$FF, only the ST/STS/STD and LD/LDS/LDD instructions can be used.
 5. USART in SPI Master Mode.
 6. Only available in the ATmega164PA/324PA/644PA/1284P.
 7. Only available in the ATmega1284/1284P

8. Instruction set summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
ARITHMETIC AND LOGIC INSTRUCTIONS					
ADD	Rd, Rr	Add two Registers	$Rd \leftarrow Rd + Rr$	Z,C,N,V,H	1
ADC	Rd, Rr	Add with Carry two Registers	$Rd \leftarrow Rd + Rr + C$	Z,C,N,V,H	1
ADIW	RdI,K	Add Immediate to Word	$Rdh:Rdl \leftarrow Rdh:Rdl + K$	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract two Registers	$Rd \leftarrow Rd - Rr$	Z,C,N,V,H	1
SUBI	Rd, K	Subtract Constant from Register	$Rd \leftarrow Rd - K$	Z,C,N,V,H	1
SBC	Rd, Rr	Subtract with Carry two Registers	$Rd \leftarrow Rd - Rr - C$	Z,C,N,V,H	1
SBCI	Rd, K	Subtract with Carry Constant from Reg.	$Rd \leftarrow Rd - K - C$	Z,C,N,V,H	1
SBIW	RdI,K	Subtract Immediate from Word	$Rdh:Rdl \leftarrow Rdh:Rdl - K$	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND Registers	$Rd \leftarrow Rd \bullet Rr$	Z,N,V	1
ANDI	Rd, K	Logical AND Register and Constant	$Rd \leftarrow Rd \bullet K$	Z,N,V	1
OR	Rd, Rr	Logical OR Registers	$Rd \leftarrow Rd \vee Rr$	Z,N,V	1
ORI	Rd, K	Logical OR Register and Constant	$Rd \leftarrow Rd \vee K$	Z,N,V	1
EOR	Rd, Rr	Exclusive OR Registers	$Rd \leftarrow Rd \oplus Rr$	Z,N,V	1
COM	Rd	One's Complement	$Rd \leftarrow 0xFF - Rd$	Z,C,N,V	1
NEG	Rd	Two's Complement	$Rd \leftarrow 0x00 - Rd$	Z,C,N,V,H	1
SBR	Rd,K	Set Bit(s) in Register	$Rd \leftarrow Rd \vee K$	Z,N,V	1
CBR	Rd,K	Clear Bit(s) in Register	$Rd \leftarrow Rd \bullet (0xFF - K)$	Z,N,V	1
INC	Rd	Increment	$Rd \leftarrow Rd + 1$	Z,N,V	1
DEC	Rd	Decrement	$Rd \leftarrow Rd - 1$	Z,N,V	1
TST	Rd	Test for Zero or Minus	$Rd \leftarrow Rd \bullet Rd$	Z,N,V	1
CLR	Rd	Clear Register	$Rd \leftarrow Rd \oplus Rd$	Z,N,V	1
SER	Rd	Set Register	$Rd \leftarrow 0xFF$	None	1
MUL	Rd, Rr	Multiply Unsigned	$R1:R0 \leftarrow Rd \times Rr$	Z,C	2
MULS	Rd, Rr	Multiply Signed	$R1:R0 \leftarrow Rd \times Rr$	Z,C	2
MULSU	Rd, Rr	Multiply Signed with Unsigned	$R1:R0 \leftarrow Rd \times Rr$	Z,C	2
FMUL	Rd, Rr	Fractional Multiply Unsigned	$R1:R0 \leftarrow (Rd \times Rr) \ll 1$	Z,C	2
FMULS	Rd, Rr	Fractional Multiply Signed	$R1:R0 \leftarrow (Rd \times Rr) \ll 1$	Z,C	2
FMULSU	Rd, Rr	Fractional Multiply Signed with Unsigned	$R1:R0 \leftarrow (Rd \times Rr) \ll 1$	Z,C	2
BRANCH INSTRUCTIONS					
RJMP	k	Relative Jump	$PC \leftarrow PC + k + 1$	None	2
IJMP		Indirect Jump to (Z)	$PC \leftarrow Z$	None	2
JMP	k	Direct Jump	$PC \leftarrow k$	None	3
RCALL	k	Relative Subroutine Call	$PC \leftarrow PC + k + 1$	None	3
ICALL		Indirect Call to (Z)	$PC \leftarrow Z$	None	3
CALL	k	Direct Subroutine Call	$PC \leftarrow k$	None	4
RET		Subroutine Return	$PC \leftarrow STACK$	None	4
RETI		Interrupt Return	$PC \leftarrow STACK$	I	4
CPSE	Rd,Rr	Compare, Skip if Equal	if $(Rd = Rr)$ $PC \leftarrow PC + 2$ or 3	None	1/2/3
CP	Rd,Rr	Compare	$Rd - Rr$	Z, N,V,C,H	1
CPC	Rd,Rr	Compare with Carry	$Rd - Rr - C$	Z, N,V,C,H	1
CPI	Rd,K	Compare Register with Immediate	$Rd - K$	Z, N,V,C,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if $(Rr(b)=0)$ $PC \leftarrow PC + 2$ or 3	None	1/2/3
SBRS	Rr, b	Skip if Bit in Register is Set	if $(Rr(b)=1)$ $PC \leftarrow PC + 2$ or 3	None	1/2/3
SBIC	P, b	Skip if Bit in I/O Register Cleared	if $(P(b)=0)$ $PC \leftarrow PC + 2$ or 3	None	1/2/3
SBIS	P, b	Skip if Bit in I/O Register is Set	if $(P(b)=1)$ $PC \leftarrow PC + 2$ or 3	None	1/2/3
BRBS	s, k	Branch if Status Flag Set	if $(SREG(s) = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRBC	s, k	Branch if Status Flag Cleared	if $(SREG(s) = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BREQ	k	Branch if Equal	if $(Z = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRNE	k	Branch if Not Equal	if $(Z = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRCS	k	Branch if Carry Set	if $(C = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRCC	k	Branch if Carry Cleared	if $(C = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRSH	k	Branch if Same or Higher	if $(C = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRLO	k	Branch if Lower	if $(C = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRMI	k	Branch if Minus	if $(N = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRPL	k	Branch if Plus	if $(N = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRGE	k	Branch if Greater or Equal, Signed	if $(N \oplus V = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRLT	k	Branch if Less Than Zero, Signed	if $(N \oplus V = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRHS	k	Branch if Half Carry Flag Set	if $(H = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRHC	k	Branch if Half Carry Flag Cleared	if $(H = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRTS	k	Branch if T Flag Set	if $(T = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRTC	k	Branch if T Flag Cleared	if $(T = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRVS	k	Branch if Overflow Flag is Set	if $(V = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2

Mnemonics	Operands	Description	Operation	Flags	#Clocks
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then PC ← PC + k + 1	None	1/2
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then PC ← PC + k + 1	None	1/2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then PC ← PC + k + 1	None	1/2
BIT AND BIT-TEST INSTRUCTIONS					
SBI	P,b	Set Bit in I/O Register	I/O(P,b) ← 1	None	2
CBI	P,b	Clear Bit in I/O Register	I/O(P,b) ← 0	None	2
LSL	Rd	Logical Shift Left	Rd(n+1) ← Rd(n), Rd(0) ← 0	Z,C,N,V	1
LSR	Rd	Logical Shift Right	Rd(n) ← Rd(n+1), Rd(7) ← 0	Z,C,N,V	1
ROL	Rd	Rotate Left Through Carry	Rd(0) ← C, Rd(n+1) ← Rd(n), C ← Rd(7)	Z,C,N,V	1
ROR	Rd	Rotate Right Through Carry	Rd(7) ← C, Rd(n) ← Rd(n+1), C ← Rd(0)	Z,C,N,V	1
ASR	Rd	Arithmetic Shift Right	Rd(n) ← Rd(n+1), n=0..6	Z,C,N,V	1
SWAP	Rd	Swap Nibbles	Rd(3..0) ← Rd(7..4), Rd(7..4) ← Rd(3..0)	None	1
BSET	s	Flag Set	SREG(s) ← 1	SREG(s)	1
BCLR	s	Flag Clear	SREG(s) ← 0	SREG(s)	1
BST	Rr, b	Bit Store from Register to T	T ← Rr(b)	T	1
BLD	Rd, b	Bit load from T to Register	Rd(b) ← T	None	1
SEC		Set Carry	C ← 1	C	1
CLC		Clear Carry	C ← 0	C	1
SEN		Set Negative Flag	N ← 1	N	1
CLN		Clear Negative Flag	N ← 0	N	1
SEZ		Set Zero Flag	Z ← 1	Z	1
CLZ		Clear Zero Flag	Z ← 0	Z	1
SEI		Global Interrupt Enable	I ← 1	I	1
CLI		Global Interrupt Disable	I ← 0	I	1
SES		Set Signed Test Flag	S ← 1	S	1
CLS		Clear Signed Test Flag	S ← 0	S	1
SEV		Set Twos Complement Overflow	V ← 1	V	1
CLV		Clear Twos Complement Overflow	V ← 0	V	1
SET		Set T in SREG	T ← 1	T	1
CLT		Clear T in SREG	T ← 0	T	1
SEH		Set Half Carry Flag in SREG	H ← 1	H	1
CLH		Clear Half Carry Flag in SREG	H ← 0	H	1
DATA TRANSFER INSTRUCTIONS					
MOV	Rd, Rr	Move Between Registers	Rd ← Rr	None	1
MOVW	Rd, Rr	Copy Register Word	Rd+1:Rd ← Rr+1:Rr	None	1
LDI	Rd, K	Load Immediate	Rd ← K	None	1
LD	Rd, X	Load Indirect	Rd ← (X)	None	2
LD	Rd, X+	Load Indirect and Post-Inc.	Rd ← (X), X ← X + 1	None	2
LD	Rd, -X	Load Indirect and Pre-Dec.	X ← X - 1, Rd ← (X)	None	2
LD	Rd, Y	Load Indirect	Rd ← (Y)	None	2
LD	Rd, Y+	Load Indirect and Post-Inc.	Rd ← (Y), Y ← Y + 1	None	2
LD	Rd, -Y	Load Indirect and Pre-Dec.	Y ← Y - 1, Rd ← (Y)	None	2
LDD	Rd,Y+q	Load Indirect with Displacement	Rd ← (Y + q)	None	2
LD	Rd, Z	Load Indirect	Rd ← (Z)	None	2
LD	Rd, Z+	Load Indirect and Post-Inc.	Rd ← (Z), Z ← Z + 1	None	2
LD	Rd, -Z	Load Indirect and Pre-Dec.	Z ← Z - 1, Rd ← (Z)	None	2
LDD	Rd, Z+q	Load Indirect with Displacement	Rd ← (Z + q)	None	2
LDS	Rd, k	Load Direct from SRAM	Rd ← (k)	None	2
ST	X, Rr	Store Indirect	(X) ← Rr	None	2
ST	X+, Rr	Store Indirect and Post-Inc.	(X) ← Rr, X ← X + 1	None	2
ST	-X, Rr	Store Indirect and Pre-Dec.	X ← X - 1, (X) ← Rr	None	2
ST	Y, Rr	Store Indirect	(Y) ← Rr	None	2
ST	Y+, Rr	Store Indirect and Post-Inc.	(Y) ← Rr, Y ← Y + 1	None	2
ST	-Y, Rr	Store Indirect and Pre-Dec.	Y ← Y - 1, (Y) ← Rr	None	2
STD	Y+q,Rr	Store Indirect with Displacement	(Y + q) ← Rr	None	2
ST	Z, Rr	Store Indirect	(Z) ← Rr	None	2
ST	Z+, Rr	Store Indirect and Post-Inc.	(Z) ← Rr, Z ← Z + 1	None	2
ST	-Z, Rr	Store Indirect and Pre-Dec.	Z ← Z - 1, (Z) ← Rr	None	2
STD	Z+q,Rr	Store Indirect with Displacement	(Z + q) ← Rr	None	2
STS	k, Rr	Store Direct to SRAM	(k) ← Rr	None	2
LPM		Load Program Memory	R0 ← (Z)	None	3
LPM	Rd, Z	Load Program Memory	Rd ← (Z)	None	3
LPM	Rd, Z+	Load Program Memory and Post-Inc	Rd ← (Z), Z ← Z + 1	None	3
SPM		Store Program Memory	(Z) ← R1:R0	None	-
IN	Rd, P	In Port	Rd ← P	None	1
OUT	P, Rr	Out Port	P ← Rr	None	1
PUSH	Rr	Push Register on Stack	STACK ← Rr	None	2
POP	Rd	Pop Register from Stack	Rd ← STACK	None	2

9. Ordering information

9.1 Atmel ATmega164A

Speed [MHz] ⁽³⁾	Power supply	Ordering code ⁽²⁾	Package ⁽¹⁾	Operational range
20	1.8 - 5.5V	ATmega164A-AU	44A	Industrial (-40°C to 85°C)
		ATmega164A-AUR ⁽⁵⁾	44A	
		ATmega164A-PU	40P6	
		ATmega164A-MU	44M1	
		ATmega164A-MUR ⁽⁵⁾	44M1	
		ATmega164A-MCH ⁽⁴⁾	44MC	
		ATmega164A-MCHR ⁽⁴⁾⁽⁵⁾	44MC	
		ATmega164A-CU	49C2	
		ATmega164A-CUR ⁽⁵⁾	49C2	

- Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
 2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
 3. For Speed vs. V_{CC} see ["Speed grades" on page 324](#).
 4. NiPdAu Lead Finish.
 5. Tape & Reel.

Package Type	
44A	44-lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP)
40P6	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)
44M1	44-pad, 7 × 7 × 1.0mm body, lead pitch 0.50mm, Thermally Enhanced Plastic Very Thin Quad Flat No-Lead (VQFN)
44MC	44-lead (2-row Staggered), 5 × 5 × 1.0mm body, 2.60 × 2.60mm Exposed Pad, Quad Flat No-Lead Package (QFN)
49C2	49-ball, (7 × 7 Array) 0.65mm Pitch, 5 × 5 × 1mm, Very Thin, Fine-Pitch Ball Grid Array Package (VFBGA)

9.3 Atmel ATmega324A

Speed [MHz] ⁽³⁾	Power supply	Ordering code ⁽²⁾	Package ⁽¹⁾	Operational range
20	1.8 - 5.5V	ATmega324A-AU ATmega324A-AUR ⁽⁵⁾ ATmega324A-PU ATmega324A-MU ATmega324A-MUR ⁽⁵⁾ ATmega324A-MCH ⁽⁴⁾ ATmega324A-MCHR ⁽⁴⁾⁽⁵⁾ ATmega324A-CU ATmega324A-CUR ⁽⁵⁾	44A 44A 40P6 44M1 44M1 44MC 44MC 49C2 49C2	Industrial (-40°C to 85°C)

- Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
 2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
 3. For Speed vs. V_{CC} see ["Speed grades" on page 324](#).
 4. NiPdAu Lead Finish.
 5. Tape & Reel.

Package Type	
44A	44-lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP)
40P6	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)
44M1	44-pad, 7 × 7 × 1.0mm body, lead pitch 0.50mm, Thermally Enhanced Plastic Very Thin Quad Flat No-Lead (VQFN)
44MC	44-lead (2-row Staggered), 5 × 5 × 1.0mm body, 2.60 × 2.60mm Exposed Pad, Quad Flat No-Lead Package (QFN)
49C2	49-ball, (7 × 7 Array) 0.65mm Pitch, 5 × 5 × 1mm, Very Thin, Fine-Pitch Ball Grid Array Package (VFBGA)

9.4 Atmel ATmega324PA

Speed [MHz] ⁽³⁾	Power supply	Ordering code ⁽²⁾	Package ⁽¹⁾	Operational range
20	1.8 - 5.5V	ATmega324PA-AU	44A	Industrial (-40°C to 85°C)
		ATmega324PA-AUR ⁽⁵⁾	44A	
		ATmega324PA-PU	40P6	
		ATmega324PA-MU	44M1	
		ATmega324PA-MUR ⁽⁵⁾	44M1	
		ATmega324PA-MCH ⁽⁴⁾	44MC	
		ATmega324PA-MCHR ⁽⁴⁾⁽⁵⁾	44MC	
		ATmega324PA-CU	49C2	
20	1.8 - 5.5V	ATmega324PA-CUR ⁽⁵⁾	49C2	Industrial (-40°C to 105°C)
		ATmega324PA-AN	44A	
		ATmega324PA-ANR ⁽⁵⁾	44A	
		ATmega324PA-PN	40P6	
		ATmega324PA-MN	44M1	
		ATmega324PA-MNR ⁽⁵⁾	44M1	

- Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
 2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
 3. For Speed vs. V_{CC} see ["Speed grades" on page 324](#).
 4. NiPdAu Lead Finish.
 5. Tape & Reel.

Package Type	
44A	44-lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP)
40P6	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)
44M1	44-pad, 7 × 7 × 1.0mm body, lead pitch 0.50mm, Thermally Enhanced Plastic Very Thin Quad Flat No-Lead (VQFN)
44MC	44-lead (2-row Staggered), 5 × 5 × 1.0mm body, 2.60 × 2.60mm Exposed Pad, Quad Flat No-Lead Package (QFN)
49C2	49-ball, (7 × 7 Array) 0.65mm Pitch, 5 × 5 × 1mm, Very Thin, Fine-Pitch Ball Grid Array Package (VFBGA)

9.5 Atmel ATmega644A

Speed [MHz] ⁽³⁾	Power supply	Ordering code ⁽²⁾	Package ⁽¹⁾	Operational range
20	1.8 - 5.5V	ATmega644A-AU ATmega644A-AUR ⁽⁴⁾ ATmega644A-PU ATmega644A-MU ATmega644A-MUR ⁽⁴⁾	44A 44A 40P6 44M1 44M1	Industrial (-40°C to 85°C)

- Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
 2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
 3. For Speed vs. V_{CC} see ["Speed grades" on page 324](#).
 4. Taper & Reel.

Package Type	
44A	44-lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP)
40P6	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)
44M1	44-pad, 7 × 7 × 1.0mm body, lead pitch 0.5 mm, Thermally Enhanced Plastic Very Thin Quad Flat No-Lead (VQFN)

9.6 Atmel ATmega644PA

Speed [MHz] ⁽³⁾	Power supply	Ordering code ⁽²⁾	Package ⁽¹⁾	Operational range
20	1.8 - 5.5V	ATmega644PA-AU ATmega644PA-AUR ⁽⁴⁾ ATmega644PA-PU ATmega644PA-MU ATmega644PA-MUR ⁽⁴⁾	44A 44A 40P6 44M1 44M1	Industrial (-40°C to 85°C)
20	1.8 - 5.5V	ATmega644PA-AN ATmega644PA-ANR ⁽⁴⁾ ATmega644PA-PN ATmega644PA-MN ATmega644PA-MNR ⁽⁴⁾	44A 44A 40P6 44M1 44M1	Industrial (-40°C to 105°C)

- Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
 2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
 3. For Speed vs. V_{CC} see ["Speed grades" on page 324](#).
 4. Taper & Reel.

Package Type	
44A	44-lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP)
40P6	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)
44M1	44-pad, 7 × 7 × 1.0mm body, lead pitch 0.50mm, Thermally Enhanced Plastic Very Thin Quad Flat No-Lead (VQFN)

9.8 Atmel ATmega1284P

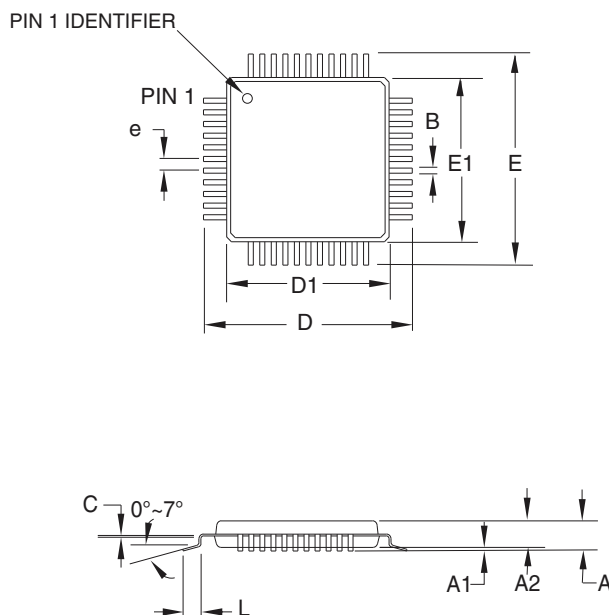
Speed [MHz] ⁽³⁾	Power supply	Ordering code ⁽²⁾	Package ⁽¹⁾	Operational range
20	1.8 - 5.5V	ATmega1284P-AU ATmega1284P-AUR ⁽⁴⁾ ATmega1284P-PU ATmega1284P-MU ATmega1284P-MUR ⁽⁴⁾	44A 44A 40P6 44M1 44M1	Industrial (-40°C to 85°C)
20	1.8 - 5.5V	ATmega1284P-AN ATmega1284P-ANR ⁽⁴⁾ ATmega1284P-PN ATmega1284P-MN ATmega1284P-MNR ⁽⁴⁾	44A 44A 40P6 44M1 44M1	Industrial (-40°C to 105°C)

- Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
 2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
 3. For Speed vs. V_{CC} see ["Speed grades" on page 324](#).
 4. Tape & Reel.

Package Type	
44A	44-lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP)
40P6	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)
44M1	44-pad, 7 × 7 × 1.0mm body, lead pitch 0.50mm, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)

10. Packaging information

10.1 44A



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	—	—	1.20	
A1	0.05	—	0.15	
A2	0.95	1.00	1.05	
D	11.75	12.00	12.25	
D1	9.90	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
B	0.30	0.37	0.45	
C	0.09	(0.17)	0.20	
L	0.45	0.60	0.75	
e	0.80 TYP			

Notes:

1. This package conforms to JEDEC reference MS-026, Variation ACB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

06/02/2014

Atmel Package Drawing Contact:
packagedrawings@atmel.com

TITLE

44A, 44-lead, 10 x 10mm body size, 1.0mm body thickness,
0.8 mm lead pitch, thin profile plastic quad flat package (TQFP)

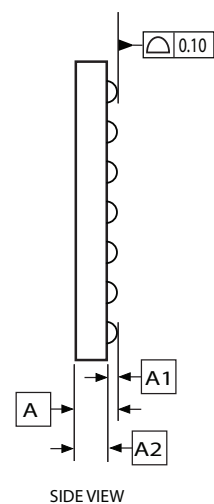
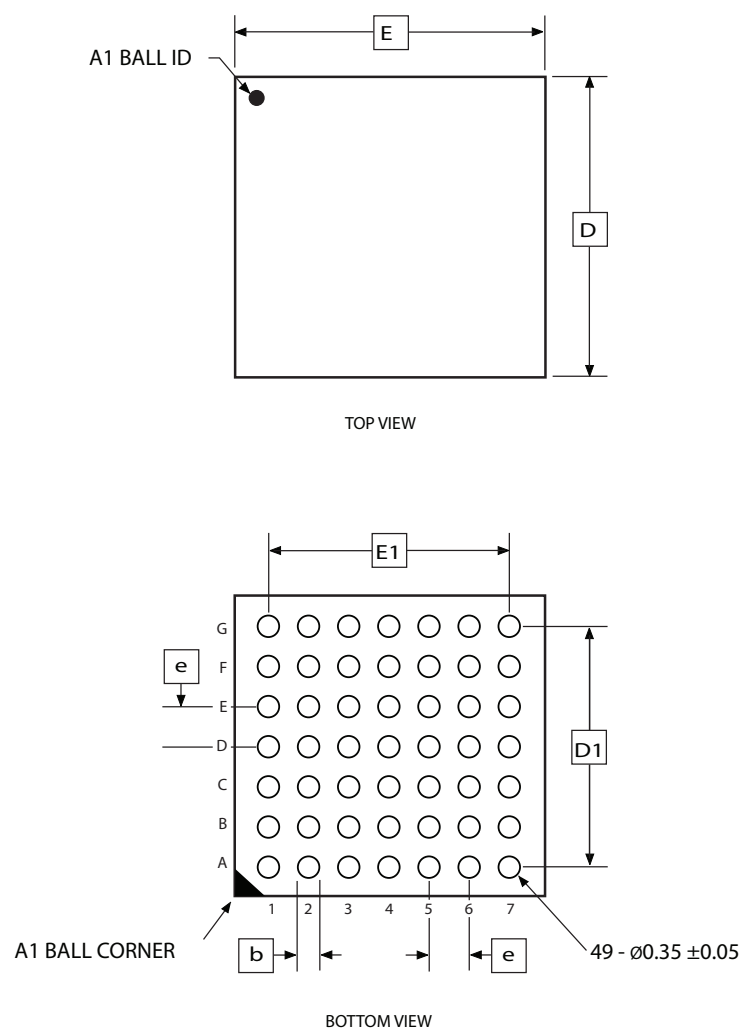
DRAWING NO.

44A

REV.

C

10.5 49C2



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	—	—	1.00	
A1	0.20	—	—	
A2	0.65	—	—	
D	4.90	5.00	5.10	
D1	3.90 BSC			
E 4.90	5.00	5.10		
E1	3.90 BSC			
b	0.30	0.35	0.40	
e	0.65 BSC			

3/14/08



Package Drawing Contact:
packagedrawings@atmel.com

TITLE
49C2, 49-ball (7 x 7 array), 0.65mm pitch,
5.0 x 5.0 x 1.0mm, very thin, fine-pitch
ball grid array package (VFPGA)

GPC

CBD

DRAWING NO.

49C2

REV.

A

12. Datasheet revision history

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

12.1 Rev. 8272G - 01/2015

1. Updated [Table 1-2 on page 5](#), [Table 8-1 on page 25](#), [Table 10-1 on page 42](#), [Table 14-3 on page 79](#), [Table 19-4 on page 187](#), [Table 19-11 on page 192](#) and [Table 28-16 on page 328](#) for formatting consistency errors
2. Updated ["Ordering information" on page 17](#):
 - Added ordering information for ATmega164PA @105°C; ATmega324PA @ 105°C; ATmega324PA @105°C; ATmega644PA @ 105°C and ATmega1284P @ 105°C
3. Updated the ["Packaging information" on page 25](#):
 - Replaced the drawing ["44M1" on page 27](#) by a correct package

12.2 Rev. 8272F - 08/2014

1. Updated text in [Section 13.2.8 "PCMSK1 – Pin Change Mask Register 1" on page 70](#) to: "If PCINT15:8 is set and the PCIE1 bit in PCICR is set, pin change interrupt is enabled on the corresponding I/O pin."
2. Corrected description of PAGESMB in [Table 26-9 on page 281](#). The device has 64 words in a page and not 128.
3. Corrected description of PAGESMB in [Table 26-12 on page 282](#). PAGESMB is 5 and the device has 64 words in a page and not 128. The page require six bits and not seven.
4. Corrected values in [Table 26-16 on page 284](#). PAGESMB is 6. ZPAGESMB is Z7 and PCPAGE is Z15:Z8
5. Corrected value for PCPAGE in [Table 27-7 on page 290](#). The correct value is PC[14:7]
6. Updated description in [Table 17-2 on page 151](#) to "Normal port operation, OC2A disconnected."
7. Updated Assembly code examples on for ["Watchdog Timer" on page 55](#). and onwards
 - "out WDTCR, r16" changed to "sts WDTCR, r16"
 - "in r16, WDTCR" changed to "lds r16, WDTCR"
 - "ldi r16, WDTCR" changed to "lds r16, WDTCR"
8. Updated addresses 0x65 and 0x64 in [Section 7. "Register summary" on page 10](#).
9. Removed notes 5 and 6 from [Table 28-16 on page 328](#).
10. Corrected values in [Section 8. "Instruction set summary" on page 14](#). Changed clock values for RCALL and ICALL to 2, for Call, Ret and RETI to 4. Also changed values in [Section 7.7.1 "Interrupt response time" on page 18](#).
11. Updated layout, footer and back page according to template 0205/2014

12.3 Rev. 8272E - 04/2013

1. Updated [Figure 1-1 on page 3](#) and [Figure 2-1 on page 6](#): T3 and T/C3 only available in ATmega1284/1284P.
2. Updated descriptive text on page 6 to indicate that ATmega1284/1284P has four T/Cs.
3. Updated the Assembly code example for WDT_off (p.56) following the ej# 705736.
4. Added note in ["16-bit Timer/Counter1 and Timer/Counter3^{\(1\)} with PWM" on page 107](#).
5. Added ["Prescaler Reset" on page 112](#).
6. Corrected three typo for Waveform generation mode (WGM) instead of MGM.
7. Updated [Table 23-6 on page 253](#). ADC Auto Trigger Source Selections, ADTS=0b011, the statement is Timer/Counter0 Compare Match A.
8. Updated [Table 27-18 on page 310](#). Command for 6d Poll for Fuse Write Complete: 0111011_00000000
9. Updated the table notes of the [Table 28-1 on page 318](#).
10. Updated ["Register summary" on page 10](#). Added table note 7: Only available in ATmega1284/1284P.

12.4 Rev. 8272D - 05/12

1. Updated ["Power-down mode" on page 44](#).
2. Updated ["Overview" on page 67](#).
3. Corrected references for Bit 2, Bit 1, and Bit 0 in Section ["UCSRnC – USART MSPIM Control and Status Register n C" on page 201](#).
4. Several small corrections throughout the whole document made according to the template
5. Notes in [Table 27-17 on page 304](#) have been corrected
6. Note (1) in [Table 28-3 on page 320](#) is added

12.5 Rev. 8272C - 06/11

1. Updated ["Atmel ATmega1284P DC characteristics" on page 323](#).

12.6 Rev. 8272B - 05/11

1. Added Atmel QTouch Library Support and QTouch Sensing Capability Features.
2. Replaced the [Figure 1-1 on page 3](#) by an updated ["Pinout."](#) that includes Timer/Counter3.
3. Replaced the [Figure 7-1 on page 10](#) by an updated ["Block diagram of the AVR architecture."](#) that includes Timer/Counter3.
4. Added ["RAMPZ – Extended Z-pointer Register for ELPM/SPM^{\(1\)}" on page 15](#).
5. Added ["PRR1 – Power Reduction Register 1" on page 49](#).
6. Renamed PRR to ["PRR0 – Power Reduction Register 0" on page 48](#).
7. Updated ["PCIFR – Pin Change Interrupt Flag Register" on page 69](#). PCICR replaces EIMSR in the PCIF3, PCIF2, PCIF1 and PCIF0 bit description.
8. Updated ["PCMSK3 – Pin Change Mask Register 3" on page 70](#). PCIE3 replaces PCIE2 in the bit description.
9. Updated ["Alternate Functions of Port B" on page 80](#) to include Timer/Counter3
10. Updated ["Alternate Functions of Port D" on page 86](#) to include Timer/Counter3
11. Added ["TCNT3H and TCNT3L –Timer/Counter3" on page 132](#)

