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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	AVR
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	32
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Dual Rows, Exposed Pad
Supplier Device Package	44-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atmega164pa-mchr

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

1.3 Pinout - VFBGA for Atmel ATmega164A/164PA/324A/324PA





Table 1-2.	BGA - pin	out.					
	GND	PB4	PB2	GND	VCC	PA2	GND
	PB6	PB5	PB3	PB0	PA0	PA3	PA5
	VCC	RESET	PB7	PB1	PA1	PA6	AREF
	GND	XTAL2	PD0	GND	PA4	PA7	GND
	XTAL1	PD1	PD5	PD7	PC5	PC7	AVCC
	PD2	PD3	PD6	PC0	PC2	PC4	PC6
	GND	PD4	VCC	GND	PC1	PC3	GND

2. Overview

The Atmel ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

timer base while the rest of the device is sleeping. The ADC Noise Reduction mode stops the CPU and all I/O modules except Asynchronous Timer and ADC, to minimize switching noise during ADC conversions. In Standby mode, the Crystal/Resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low power consumption. In Extended Standby mode, both the main Oscillator and the Asynchronous Timer continue to run.

Atmel offers the QTouch[®] library for embedding capacitive touch buttons, sliders and wheels functionality into AVR microcontrollers. The patented charge-transfer signal acquisition offers robust sensing and includes fully debounced reporting of touch keys and includes Adjacent Key Suppression[®] (AKS[™]) technology for unambiguous detection of key events. The easy-to-use QTouch Suite toolchain allows you to explore, develop and debug your own touch applications.

The device is manufactured using Atmel's high-density nonvolatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed in-system through an SPI serial interface, by a conventional nonvolatile memory programmer, or by an On-chip Boot program running on the AVR core. The boot program can use any interface to download the application program in the application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P is supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, in-circuit emulators, and evaluation kits.

2.2 Comparison between ATmega164A, ATmega164PA, ATmega324A, ATmega324PA, ATmega644A, ATmega644PA, ATmega1284 and ATmega1284P

Device	Flash	EEPROM	RAM	Units
ATmega164A	16K	512	1K	
ATmega164PA	16K	512	1K	
ATmega324A	32K	1K	2К	
ATmega324PA	32K	1K	2К	but a
ATmega644A	64K	2К	4K	bytes
ATmega644PA	64K	2K	4K	
ATmega1284	128K	4K	16K	
ATmega1284P	128K	4K	16K	

Table 2-1.Differences between ATmega164A, ATmega164PA, ATmega324A, ATmega324PA, ATmega644A,
ATmega644PA, ATmega1284 and ATmega1284P.

2.3 Pin Descriptions11

2.3.1 VC

Digital supply voltage.

2.3.2 GND

Ground.

3. Resources

A comprehensive set of development tools, application notes and datasheets are available for download on http://www.atmel.com/avr.

4. About code examples

This documentation contains simple code examples that briefly show how to use various parts of the device. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C compiler documentation for more details.

The code examples assume that the part specific header file is included before compilation. For I/O registers located in extended I/O map, "IN", "OUT", "SBIS", "SBIC", "CBI", and "SBI" instructions must be replaced with instructions that allow access to extended I/O. Typically "LDS" and "STS" combined with "SBRS", "SBRC", "SBR", and "CBR".

5. Data retention

Reliability Qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C or 100 years at 25°C.

6. Capacitive touch sensing

The Atmel QTouch Library provides a simple to use solution to realize touch sensitive interfaces on most Atmel AVR microcontrollers. The QTouch Library includes support for the QTouch and QMatrix acquisition methods.

Touch sensing can be added to any application by linking the appropriate Atmel QTouch Library for the AVR Microcontroller. This is done by using a simple set of APIs to define the touch channels and sensors, and then calling the touch sensing API's to retrieve the channel information and determine the touch sensor states.

The QTouch Library is FREE and downloadable from the Atmel website at the following location: www.atmel.com/qtouchlibrary. For implementation details and other information, refer to the Atmel QTouch Library User Guide - also available for download from the Atmel website.

Address	Nome	Dit 7	Dit C	DitE	Dit 4	D:4 2	Dit 0	Dit 4	Dit 0	Dere
Address	Name	Bit /	BIT 6	BIT 5	BIT 4	BIT 3	Bit 2	Bit 1	BITU	Page
(0x7C)	ADMUX	REFS1	REFS0	ADLAR	MUX4	MUX3	MUX2	MUX1	MUX0	249
(0x7B)	ADCSRB	-	ACME	-	-	-	ADTS2	ADTS1	ADTS0	233
(0x7A)	ADCSRA	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0	250
(0x79)	ADCH				ADC	Data Register H	ligh byte			251
(0x78)	ADCL				ADC	Data Register L	ow byte			251
(0x77)	Reserved	-	-	-	-	-	-	-	-	
(0x76)	Reserved	-	-	-	-	-	-	-	-	
(0x75)	Reserved	-	-	-	-	-	-	-	-	
(0x74)	Reserved	-	-	-	-	-	-	-	-	
(0x73)	PCMSK3	PCINT31	PCINT30	PCINT29	PCINT28	PCINT27	PCINT26	PCINT25	PCINT24	70
(0x72)	Reserved	-	-	-	-	-	-	-	-	
(0x71)	TIMSK3	-	-	ICIE3	-	-	OCIE3B	OCIE3A	TOIE3	134
(0x70)	TIMSK2	-	-	-	-	-	OCIE2B	OCIE2A	TOIE2	156
(0x6F)	TIMSK1	-	-	ICIE1	-	-	OCIE1B	OCIE1A	TOIE1	134
(0x6E)	TIMSK0	-	-	-	-	-	OCIE0B	OCIE0A	TOIE0	105
(0x6D)	PCMSK2	PCINT23	PCINT22	PCINT21	PCINT20	PCINT19	PCINT18	PCINT17	PCINT16	70
(0x6C)	PCMSK1	PCINT15	PCINT14	PCINT13	PCINT12	PCINT11	PCINT10	PCINT9	PCINT8	70
(0x6B)	PCMSK0	PCINT7	PCINT6	PCINT5	PCINT4	PCINT3	PCINT2	PCINT1	PCINT0	71
(0x6A)	Reserved	-	-	-	-	-	-	-	-	
(0x69)	EICRA	-	-	ISC21	ISC20	ISC11	ISC10	ISC01	ISC00	67
(0x68)	PCICR	-	-	-	-	PCIE3	PCIE2	PCIE1	PCIE0	69
(0x67)	Reserved	_	_	_	_	-	-	-	-	
(0x66)	OSCCAL				Oscil	lator Calibration	Register			40
(0x65)	PRR1	_	-	_	-	-	-	-	PRTIM3	49
(0x64)	PRRO	PRTWI	PRTIM2	PRTIMO	PRUSART1	PRTIM1	PRSPI	PRUSARTO	PRADC	48
(0x63)	Peserved		TITTIVIZ	TICTIMO	TROOART	TIXTIWIT	TROLL	TROOMING	TRADO	40
(0x03)	Reserved	-	-	-	-	-	-	-	-	
(0x02)	CLKDD		-	-	-		-			40
(0x01)				-		ULKF33	ULKF32	UKP31	ULKF30	40
(0x60)	WDICSR	WDIF	VVDIE T	WDP3	WDCE	WDE	WDP2		WDP0	59
0x3F (0x5F)	SREG	1	1	H	5	V	N OD40	Ζ	C ODD	11
0x3E (0x5E)	SPH	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	12
0x3D (0x5D)	SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	12
0x3C (0x5C)	Reserved	-	-	-	-	-	-	-	-	
0x3B (0x5B)	Reserved	-	-	-	-	-	-	-	-	
0x3A (0x5A)	Reserved	-	-	-	-	-	-	-	-	
0x39 (0x59)	Reserved	-	-	-	-	-	-	-	-	
0x38 (0x58)	Reserved	-	-	-	-	-	-	-	-	
0x37 (0x57)	SPMCSR	SPMIE	RWWSB	SIGRD	RWWSRE	BLBSET	PGWRT	PGERS	SPMEN	285
0x36 (0x56)	Reserved	-	-	-	-	-	-	-	-	
0x35 (0x55)	MCUCR	JTD	BODS ⁽⁶⁾	BODSE ⁽⁶⁾	PUD	-	-	IVSEL	IVCE	89/268
0x34 (0x54)	MCUSR	-	-	-	JTRF	WDRF	BORF	EXTRF	PORF	58/268
0x33 (0x53)	SMCR	-	-	-	-	SM2	SM1	SM0	SE	47
0x32 (0x52)	Reserved	-	-	-	-	-	-	-	-	
0x31 (0x51)	OCDR		-		0	n-Chip Debug Re	egister	-		259
0x30 (0x50)	ACSR	ACD	ACBG	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	250
0x2F (0x4F)	Reserved	-	-	-	-	-	-	-	-	
0x2E (0x4E)	SPDR					SPI 0 Data Regi	ster			166
0x2D (0x4D)	SPSR	SPIF0	WCOL0	-	-	-	-	-	SPI2X0	165
0x2C (0x4C)	SPCR	SPIE0	SPE0	DORD0	MSTR0	CPOL0	CPHA0	SPR01	SPR00	164
0x2B (0x4B)	GPIOR2		•	•	Gene	al Purpose I/O F	Register 2		•	29
0x2A (0x4A)	GPIOR1				Gene	al Purpose I/O F	Register 1			29
0x29 (0x49)	Reserved	-	-	-	-	-	-	-	-	
0x28 (0x48)	OCR0B				Timer/Coun	ter0 Output Com	pare Register B			105
0x27 (0x47)	OCR0A				Timer/Coun	ter0 Output Com	pare Register A			105
0x26 (0x46)	TCNT0				1	imer/Counter0 (8 Bit)			105
0x25 (0x45)	TCCR0B	FOCOA	FOCOB	_		WGM02	CS02	CS01	CS00	104
0x24 (0x44)	TCCR0A	COM0A1	COMOAO	COM0B1	COM0B0	-	0002	WGM01	WGM00	105
0x27 (0x47)	GTCCP	TEM	COMICAU	CONIDET	CONIDBO	-	-	PEDAEV	PEDEVNIC	157
0x23 (0x43)	FEADU	1 3101	-	-	-	-	FEDDOM Addres	e Register High Puto	FONOTING	24
0x21 (0x42)	FEADI	-	-	-	EEDBOA		ter Low Bute	a register riigit byte		24
0x21 (0x41)					EEPKUN	DROM Data D	ici LUW Dyle			24
0x20 (0x40)	EEDK				E		gister	FEDE		24
	EEUK	-	-	EEPM1	EEPMU			EEPE	EEKE	24
0x1E (0x3E)	GPIOR0				Gene	ai Purpose I/O F	kegister U	n		29
0x1D (0x3D)	EIMSK	-	-	-	-	-	INT2	INT1	INT0	68
0x1C (0x3C)	EIFR	-	-	-	-	-	INTF2	INTF1	INTF0	68
0x1B (0x3B)	PCIFR	-	-	-	-	PCIF3	PCIF2	PCIF1	PCIF0	69
0x1A (0x3A)	Reserved	-	-	-	-	-	-	-	-	
0x19 (0x39)	Reserved	-	-	-	-	-	-	-	-	1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x18 (0x38)	TIFR3	-	-	ICF3	-	-	OCF3B	OCF3A	TOV3	136
0x17 (0x37)	TIFR2	-	-	-	-	-	OCF2B	OCF2A	TOV2	156
0x16 (0x36)	TIFR1	-	-	ICF1	-	-	OCF1B	OCF1A	TOV1	135
0x15 (0x35)	TIFR0	-	-	-	-	-	OCF0B	OCF0A	TOV0	106
0x14 (0x34)	Reserved	-	-	-	-	-	-	-	-	
0x13 (0x33)	Reserved	-	-	-	-	-	-	-	-	
0x12 (0x32)	Reserved	-	-	-	-	-	-	-	-	
0x11 (0x31)	Reserved	-	-	-	-	-	-	-	-	
0x10 (0x30)	Reserved	-	-	-	-	-	-	-	-	
0x0F (0x2F)	Reserved	-	-	-	-	-	-	-	-	
0x0E (0x2E)	Reserved	-	-	-	-	-	-	-	-	
0x0D (0x2D)	Reserved	-	-	-	-	-	-	-	-	
0x0C (0x2C)	Reserved	-	-	-	-	-	-	-	-	
0x0B (0x2B)	PORTD	PORTD7	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	90
0x0A (0x2A)	DDRD	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	90
0x09 (0x29)	PIND	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	90
0x08 (0x28)	PORTC	PORTC7	PORTC6	PORTC5	PORTC4	PORTC3	PORTC2	PORTC1	PORTC0	90
0x07 (0x27)	DDRC	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	90
0x06 (0x26)	PINC	PINC7	PINC6	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0	90
0x05 (0x25)	PORTB	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	89
0x04 (0x24)	DDRB	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	89
0x03 (0x23)	PINB	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	90
0x02 (0x22)	PORTA	PORTA7	PORTA6	PORTA5	PORTA4	PORTA3	PORTA2	PORTA1	PORTA0	89
0x01 (0x21)	DDRA	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0	89
0x00 (0x20)	PINA	PINA7	PINA6	PINA5	PINA4	PINA3	PINA2	PINA1	PINA0	89

Notes: 1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.

2. I/O registers within the address range \$00 - \$1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions.

- 3. Some of the status flags are cleared by writing a logical one to them. Note that the CBI and SBI instructions will operate on all bits in the I/O register, writing a one back into any flag read as set, thus clearing the flag. The CBI and SBI instructions work with registers 0x00 to 0x1F only.
- 4. When using the I/O specific commands IN and OUT, the I/O addresses \$00 \$3F must be used. When addressing I/O registers as data space using LD and ST instructions, \$20 must be added to these addresses. The ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P is a complex microcontroller with more peripheral units than can be supported within the 64 location reserved in Opcode for the IN and OUT instructions. For the Extended I/O space from \$60 \$FF, only the ST/STS/STD and LD/LDS/LDD instructions can be used.
- 5. USART in SPI Master Mode.
- 6. Only available in the ATmega164PA/324PA/644PA/1284P.
- 7. Only available in the ATmega1284/1284P

Mnemonics	Operands	Description	Operation	Flags	#Clocks
MCU CONTROL INS	TRUCTIONS				
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep function)	None	1
WDR		Watchdog Reset	(see specific descr. for WDR/timer)	None	1
BREAK		Break	For On-chip Debug Only	None	N/A

9.5 Atmel ATmega644A

Speed [MHz] ⁽³⁾	Power supply	Ordering code ⁽²⁾	Package ⁽¹⁾	Operational range
20	1.8 - 5.5V	ATmega644A-AU ATmega644A-AUR ⁽⁴⁾ ATmega644A-PU ATmega644A-MU ATmega644A-MUR ⁽⁴⁾	44A 44A 40P6 44M1 44M1	Industrial (-40°C to 85°C)

Notes: 1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.

3. For Speed vs. V_{CC} see "Speed grades" on page 324.

4. Taper & Reel.

	Package Type					
44A	44-lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP)					
40P6	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)					
44M1	44-pad, 7 × 7 × 1.0mm body, lead pitch 0.5 mm, Thermally Enhanced Plastic Very Thin Quad Flat No-Lead (VQFN)					

9.6 Atmel ATmega644PA

Speed [MHz] ⁽³⁾	Power supply	Ordering code ⁽²⁾	Package ⁽¹⁾	Operational range
20	1.8 - 5.5V	ATmega644PA-AU ATmega644PA-AUR ⁽⁴⁾ ATmega644PA-PU ATmega644PA-MU ATmega644PA-MUR ⁽⁴⁾	44A 44A 40P6 44M1 44M1	Industrial (-40°C to 85°C)
20	1.8 - 5.5V	ATmega644PA-AN ATmega644PA-ANR ⁽⁴⁾ ATmega644PA-PN ATmega644PA-MN ATmega644PA-MNR ⁽⁴⁾	44A 44A 40P6 44M1 44M1	Industrial (-40°C to 105°C)

Notes: 1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.

3. For Speed vs. V_{CC} see "Speed grades" on page 324.

4. Taper & Reel.

	Package Type				
44A	44-lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP)				
40P6	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)				
44M1	44-pad, 7 × 7 × 1.0mm body, lead pitch 0.50mm, Thermally Enhanced Plastic Very Thin Quad Flat No-Lead (VQFN)				

9.7 Atmel ATmega1284

Speed [MHz] ⁽³⁾	Power supply	Ordering code ⁽²⁾	Package ⁽¹⁾	Operational range
20	1.8 - 5.5V	ATmega1284-AU ATmega1284-AUR ⁽⁴⁾ ATmega1284-PU ATmega1284-MU ATmega1284-MUR ⁽⁴⁾	44A 44A 40P6 44M1 44M1	Industrial (-40°C to 85°C)

Notes: 1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.

3. For Speed vs. V_{CC} see "Speed grades" on page 324.

4. Tape & Reel.

Package Type					
44A	44-lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP)				
40P6	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)				
44M1	44-pad, 7 × 7 × 1.0mm body, lead pitch 0.50mm, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)				

9.8 Atmel ATmega1284P

Speed [MHz] ⁽³⁾	Power supply	Ordering code ⁽²⁾	Package ⁽¹⁾	Operational range
20	1.8 - 5.5V	ATmega1284P-AU ATmega1284P-AUR ⁽⁴⁾ ATmega1284P-PU ATmega1284P-MU ATmega1284P-MUR ⁽⁴⁾	44A 44A 40P6 44M1 44M1	Industrial (-40°C to 85°C)
20	1.8 - 5.5V	ATmega1284P-AN ATmega1284P-ANR ⁽⁴⁾ ATmega1284P-PN ATmega1284P-MN ATmega1284P-MNR ⁽⁴⁾	44A 44A 40P6 44M1 44M1	Industrial (-40°C to 105°C)

Notes: 1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.

- 3. For Speed vs. V_{CC} see "Speed grades" on page 324.
- 4. Tape & Reel.

Package Type				
44A	44-lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP)			
40P6	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)			
44M1	44-pad, 7 × 7 × 1.0mm body, lead pitch 0.50mm, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)			

10. Packaging information

10.1 44A

10.2 40P6

10.5 49C2

11. Errata

11.1 Errata for ATmega164A

11.1.1 Rev. E

No known Errata.

11.2 Errata for ATmega164PA

11.2.1 Rev. E

No known Errata.

11.3 Errata for ATmega324A

11.3.1 Rev. F

No known Errata.

11.4 Errata for ATmega324PA

11.4.1 Rev. F

No known Errata.

11.5 Errata for ATmega644A

11.5.1 Rev. F

No known Errata.

11.6 Errata for ATmega644PA

11.6.1 Rev. F

No known Errata.

11.7 Errata for ATmega1284

11.7.1 Rev. B

No known Errata.

11.8 Errata for ATmega1284P

11.8.1 Rev. B

No known Errata.

12. Datasheet revision history

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

12.1 Rev. 8272G - 01/2015

1.	Updated Table 1-2 on page 5, Table 8-1 on page 25, Table 10-1 on page 42, Table 14-3 on page 79, Table 19-4 on page 187, Table 19-11 on page 192 and Table 28-16 on page 328 for formatting consistency errors
2.	Updated "Ordering information" on page 17: - Added ordering information for ATmega164PA @105°C; ATmega324PA @ 105°C; ATmega324PA @105°C; ATmega644PA @ 105°C and ATmega1284P @ 105°C
3.	Updated the "Packaging information" on page 25: – Replaced the drawing "44M1" on page 27 by a correct package

12.2 Rev. 8272F - 08/2014

- 1. Updated text in Section 13.2.8 "PCMSK1 Pin Change Mask Register 1" on page 70 to: "If PCINT15:8 is set and the PCIE1 bit in PCICR is set, pin change interrupt is enabled on the corresponding I/O pin."
- 2. Corrected description of PAGEMSB in Table 26-9 on page 281. The device has 64 words in a page and not 128.
- 3. Corrected description of PAGEMSB in Table 26-12 on page 282. PAGESMB is 5 and the device has 64 words in a page and not 128. The page require six bits and not seven.
- 4. Corrected values in Table 26-16 on page 284. PAGEMSB is 6. ZPAGEMSB is Z7 and PCPAGE is Z15:Z8
- 5. Corrected value for PCPAGE in Table 27-7 on page 290. The correct value is PC[14:7]
- 6. Updated description in Table 17-2 on page 151 to "Normal port operation, OC2A disconnected."

Updated Assembly code examples on for "Watchdog Timer" on page 55. and onwards "out WDTCSR, r16" changed to "sts WDTCSR, r16"

- "in r16, WDTCSR" changed to "lds r16, WDTCSR"
 "idi r16, WDTCSR" changed to "lds r16, WDTCSR"
- 8. Updated addresses 0x65 and 0x64 in Section 7. "Register summary" on page 10.
- 9. Removed notes 5 and 6 from Table 28-16 on page 328.
- 10. Corrected values in Section 8. "Instruction set summary" on page 14. Changed clock values for RCALL and ICALL to 2, for Call, Ret and RETI to 4. Also changed values in Section 7.7.1 "Interrupt response time" on page 18.
- 11. Updated layout, footer and back page according to template 0205/2014

12.3 Rev. 8272E - 04/2013

- 1. Updated Figure 1-1 on page 3 and Figure 2-1 on page 6: T3 and T/C3 only available in ATmega1284/1284P.
- 2. Updated descriptive text on page 6 to indicate that ATmega1284/1284P has four T/Cs.
- 3. Updated the Assembly code example for WDT_off (p.56) following the ej# 705736.
- 4. Added note in "16-bit Timer/Counter1 and Timer/Counter3⁽¹⁾ with PWM" on page 107.
- 5. Added "Prescaler Reset" on page 112.
- 6. Corrected three typo for Waveform generation mode (WGM) instead of MGM.
- 7. Updated Table 23-6 on page 253. ADC Auto Trigger Source Selections, ADTS=0b011, the statement is Timer/Counter0 Compare Match A.
- 8. Updated Table 27-18 on page 310. Command for 6d Poll for Fuse Write Complete: 0111011 0000000
- 9. Updated the table notes of the Table 28-1 on page 318.
- 10. Updated "Register summary" on page 10. Added table note 7: Only available in ATmega1284/1284P.

12.4 Rev. 8272D - 05/12

- 1. Updated "Power-down mode" on page 44.
- 2. Updated "Overview" on page 67.
- 3. Corrected references for Bit 2, Bit 1, and Bit 0 in Section "UCSRnC USART MSPIM Control and Status Register n C" on page 201.
- 4. Several small corrections throughout the whole document made according to the template
- 5. Notes in Table 27-17 on page 304 have been corrected
- 6. Note (1) in Table 28-3 on page 320 is added

12.5 Rev. 8272C - 06/11

1. Updated "Atmel ATmega1284P DC characteristics" on page 323.

12.6 Rev. 8272B - 05/11

- 1. Added Atmel QTouch Library Support and QTouch Sensing Capability Features.
- 2. Replaced the Figure 1-1 on page 3 by an updated "Pinout." that includes Timer/Counter3.
- 3. Replaced the Figure 7-1 on page 10 by an updated "Block diagram of the AVR architecture." that includes Timer/Counter3.
- 4. Added "RAMPZ Extended Z-pointer Register for ELPM/SPM⁽¹⁾" on page 15.
- 5. Added "PRR1 Power Reduction Register 1" on page 49.
- 6. Renamed PRR to "PRR0 Power Reduction Register 0" on page 48.
- 7. Updated "PCIFR Pin Change Interrupt Flag Register" on page 69. PCICR replaces EIMSR in the PCIF3, PCIF2, PCIF1 and PCIF0 bit description.
- 8. Updated "PCMSK3 Pin Change Mask Register 3" on page 70. PCIE3 replaces PCIE2 in the bit description.
- 9. Updated "Alternate Functions of Port B" on page 80 to include Timer/Counter3
- 10. Updated "Alternate Functions of Port D" on page 86 to include Timer/Counter3
- 11. Added "TCNT3H and TCNT3L –Timer/Counter3" on page 132

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 Atmel Corporation
 1600 Technology Drive, San Jose, CA 95110 USA
 T: (+1)(408) 441.0311
 F: (+1)(408) 436.4200
 www.atmel.com

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