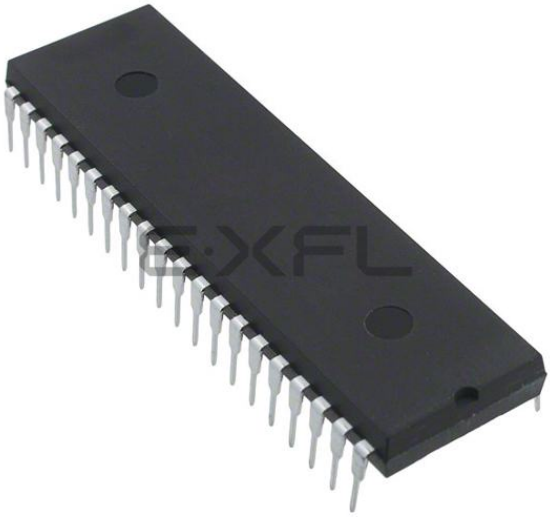

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	32
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atmega324a-pu

- Programmable Watchdog Timer with Separate On-chip Oscillator
- On-chip Analog Comparator
- Interrupt and Wake-up on Pin Change

- Special Microcontroller Features
  - Power-on Reset and Programmable Brown-out Detection
  - Internal Calibrated RC Oscillator
  - External and Internal Interrupt Sources
  - Six Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby and Extended Standby
- I/O and Packages
  - 32 Programmable I/O Lines
  - 40-pin PDIP, 44-lead TQFP, 44-pad VQFN/QFN/MLF
  - 44-pad DRQFN

– 49-ball VFBGA

- Operating Voltages
  - 1.8 - 5.5V
- Speed Grades
  - 0 - 4MHz @ 1.8 - 5.5V
  - 0 - 10MHz @ 2.7 - 5.5V
  - 0 - 20MHz @ 4.5 - 5.5V
- Power Consumption at 1MHz, 1.8V, 25°C
  - Active: 0.4mA
  - Power-down Mode: 0.1µA
  - Power-save Mode: 0.6µA (Including 32kHz RTC)

Note: 1. See ”Data retention” on page 9 for details.

1.2 Pinout - DRQFN for Atmel ATmega164A/164PA/324A/324PA

Figure 1-2. DRQFN - pinout.

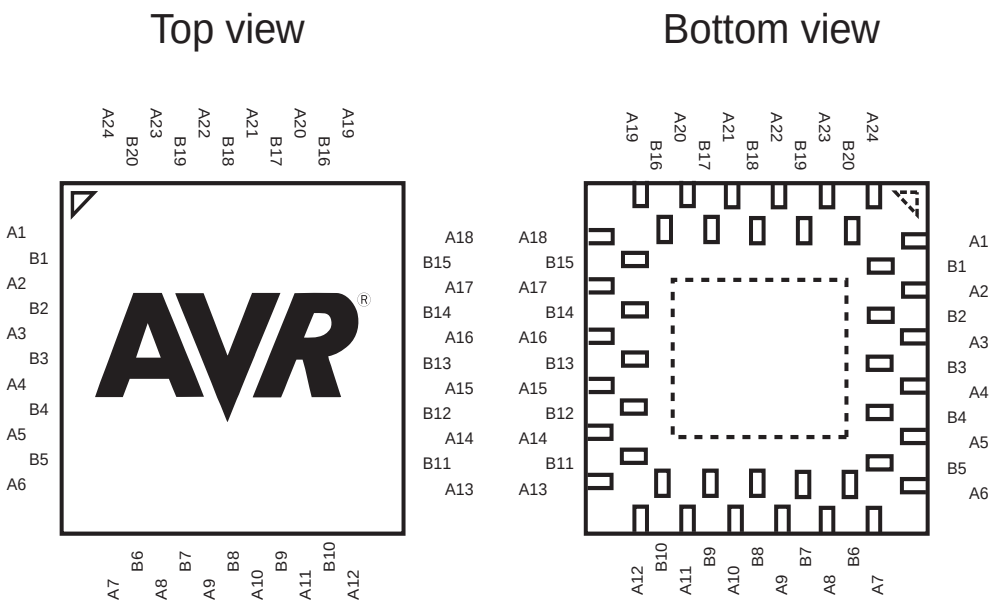


Table 1-1. DRQFN - pinout.

A1	PB5	**A7**	PD3	**A13**	PC4	**A19**	PA3
B1	PB6	**B6**	PD4	**B11**	PC5	**B16**	PA2
A2	PB7	**A8**	PD5	**A14**	PC6	**A20**	PA1
B2	$\overline{\text{RESET}}$	**B7**	PD6	**B12**	PC7	**B17**	PA0
A3	VCC	**A9**	PD7	**A15**	AVCC	**A21**	VCC
B3	GND	**B8**	VCC	**B13**	GND	**B18**	GND
A4	XTAL2	**A10**	GND	**A16**	AREF	**A22**	PB0
B4	XTAL1	**B9**	PC0	**B14**	PA7	**B19**	PB1
A5	PD0	**A11**	PC1	**A17**	PA6	**A23**	PB2
B5	PD1	**B10**	PC2	**B15**	PA5	**B20**	PB3
A6	PD2	**A12**	PC3	**A18**	PA4	**A24**	PB4

1.3 Pinout - VFBGA for Atmel ATmega164A/164PA/324A/324PA

Figure 1-3. VFBGA - pinout.

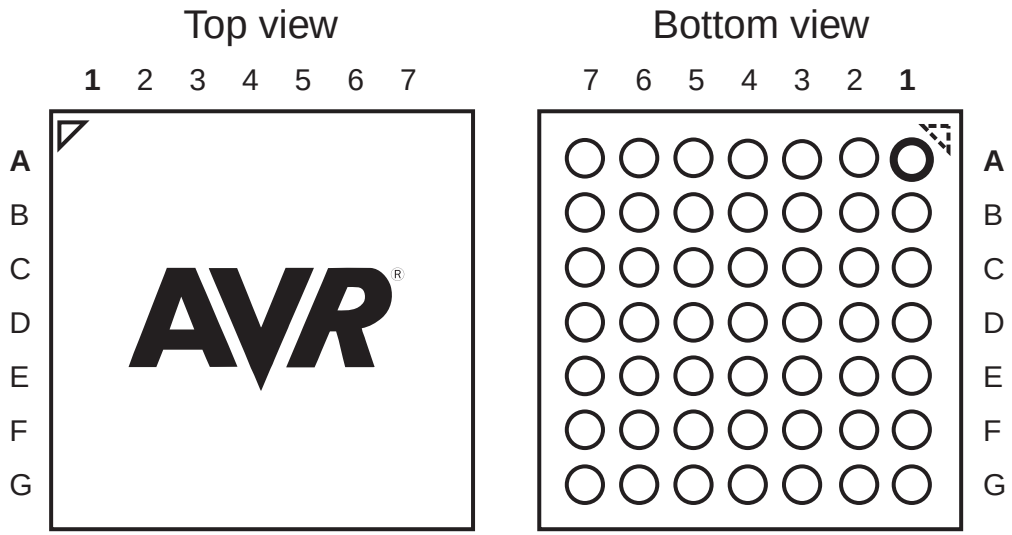


Table 1-2. BGA - pinout.

	GND	PB4	PB2	GND	VCC	PA2	GND
	PB6	PB5	PB3	PB0	PA0	PA3	PA5
	VCC	RESET	PB7	PB1	PA1	PA6	AREF
	GND	XTAL2	PD0	GND	PA4	PA7	GND
	XTAL1	PD1	PD5	PD7	PC5	PC7	AVCC
	PD2	PD3	PD6	PC0	PC2	PC4	PC6
	GND	PD4	VCC	GND	PC1	PC3	GND

2. Overview

The Atmel ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

2.3.3 Port A (PA7:PA0)

Port A serves as analog inputs to the Analog-to-digital Converter.
Port A also serves as an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port A output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port A pins that are externally pulled low will source current if the pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running.
Port A also serves the functions of various special features of the Atmel ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P as listed on page 79.

2.3.4 Port B (PB7:PB0)

Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.
Port B also serves the functions of various special features of the ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P as listed on page 80.

2.3.5 Port C (PC7:PC0)

Port C is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.
Port C also serves the functions of the JTAG interface, along with special features of the Atmel ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P as listed on page 83.

2.3.6 Port D (PD7:PD0)

Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.
Port D also serves the functions of various special features of the ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P as listed on page 86.

2.3.7 $\overline{\text{RESET}}$

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in "" on page 325. Shorter pulses are not guaranteed to generate a reset.

2.3.8 XTAL1

Input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

2.3.9 XTAL2

Output from the inverting Oscillator amplifier.

2.3.10 AVCC

AVCC is the supply voltage pin for Port A and the Analog-to-digital Converter. It should be externally connected to V_{CC}, even if the ADC is not used. If the ADC is used, it should be connected to V_{CC} through a low-pass filter.

2.3.11 AREF

This is the analog reference pin for the Analog-to-digital Converter.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
(0x7C)	ADMUX	REFS1	REFS0	ADLAR	MUX4	MUX3	MUX2	MUX1	MUX0	249
(0x7B)	ADCSRB	-	ACME	-	-	-	ADTS2	ADTS1	ADTS0	233
(0x7A)	ADCSRA	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0	250
(0x79)	ADCH	ADC Data Register High byte								251
(0x78)	ADCL	ADC Data Register Low byte								251
(0x77)	Reserved	-	-	-	-	-	-	-	-	
(0x76)	Reserved	-	-	-	-	-	-	-	-	
(0x75)	Reserved	-	-	-	-	-	-	-	-	
(0x74)	Reserved	-	-	-	-	-	-	-	-	
(0x73)	PCMSK3	PCINT31	PCINT30	PCINT29	PCINT28	PCINT27	PCINT26	PCINT25	PCINT24	70
(0x72)	Reserved	-	-	-	-	-	-	-	-	
(0x71)	TIMSK3	-	-	ICIE3	-	-	OCIE3B	OCIE3A	TOIE3	134
(0x70)	TIMSK2	-	-	-	-	-	OCIE2B	OCIE2A	TOIE2	156
(0x6F)	TIMSK1	-	-	ICIE1	-	-	OCIE1B	OCIE1A	TOIE1	134
(0x6E)	TIMSK0	-	-	-	-	-	OCIE0B	OCIE0A	TOIE0	105
(0x6D)	PCMSK2	PCINT23	PCINT22	PCINT21	PCINT20	PCINT19	PCINT18	PCINT17	PCINT16	70
(0x6C)	PCMSK1	PCINT15	PCINT14	PCINT13	PCINT12	PCINT11	PCINT10	PCINT9	PCINT8	70
(0x6B)	PCMSK0	PCINT7	PCINT6	PCINT5	PCINT4	PCINT3	PCINT2	PCINT1	PCINT0	71
(0x6A)	Reserved	-	-	-	-	-	-	-	-	
(0x69)	EICRA	-	-	ISC21	ISC20	ISC11	ISC10	ISC01	ISC00	67
(0x68)	PCICR	-	-	-	-	PCIE3	PCIE2	PCIE1	PCIE0	69
(0x67)	Reserved	-	-	-	-	-	-	-	-	
(0x66)	OSCCAL	Oscillator Calibration Register								40
(0x65)	PRR1	-	-	-	-	-	-	-	--PRTIM3	49
(0x64)	PRR0	PRTWI	PRTIM2	PRTIM0	PRUSART1	PRTIM1	PRSPI	PRUSART0	PRADC	48
(0x63)	Reserved	-	-	-	-	-	-	-	-	
(0x62)	Reserved	-	-	-	-	-	-	-	-	
(0x61)	CLKPR	CLKPCE	-	-	-	CLKPS3	CLKPS2	CLKPS1	CLKPS0	40
(0x60)	WDTCSR	WDIF	WDIE	WDP3	WDCE	WDE	WDP2	WDP1	WDP0	59
0x3F (0x5F)	SREG	I	T	H	S	V	N	Z	C	11
0x3E (0x5E)	SPH	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	12
0x3D (0x5D)	SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	12
0x3C (0x5C)	Reserved	-	-	-	-	-	-	-	-	
0x3B (0x5B)	Reserved	-	-	-	-	-	-	-	-	
0x3A (0x5A)	Reserved	-	-	-	-	-	-	-	-	
0x39 (0x59)	Reserved	-	-	-	-	-	-	-	-	
0x38 (0x58)	Reserved	-	-	-	-	-	-	-	-	
0x37 (0x57)	SPMCSR	SPMIE	RWWSB	SIGRD	RWWSRE	BLBSET	PGWRT	PGERS	SPMEN	285
0x36 (0x56)	Reserved	-	-	-	-	-	-	-	-	
0x35 (0x55)	MCUCR	JTD	BODS[6]	BODSE[6]	PUD	-	-	IVSEL	IVCE	89/268
0x34 (0x54)	MCUSR	-	-	-	JTRF	WDRF	BORF	EXTRF	PORF	58/268
0x33 (0x53)	SMCR	-	-	-	-	SM2	SM1	SM0	SE	47
0x32 (0x52)	Reserved	-	-	-	-	-	-	-	-	
0x31 (0x51)	OCDR	On-Chip Debug Register								259
0x30 (0x50)	ACSR	ACD	ACBG	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	250
0x2F (0x4F)	Reserved	-	-	-	-	-	-	-	-	
0x2E (0x4E)	SPDR	SPI 0 Data Register								166
0x2D (0x4D)	SPSR	SPIF0	WCOL0	-	-	-	-	-	SPI2X0	165
0x2C (0x4C)	SPCR	SPIE0	SPE0	DORD0	MSTR0	CPOL0	CPHA0	SPR01	SPR00	164
0x2B (0x4B)	GPIOR2	General Purpose I/O Register 2								29
0x2A (0x4A)	GPIOR1	General Purpose I/O Register 1								29
0x29 (0x49)	Reserved	-	-	-	-	-	-	-	-	
0x28 (0x48)	OCR0B	Timer/Counter0 Output Compare Register B								105
0x27 (0x47)	OCR0A	Timer/Counter0 Output Compare Register A								105
0x26 (0x46)	TCNT0	Timer/Counter0 (8 Bit)								105
0x25 (0x45)	TCCR0B	FOC0A	FOC0B	-	-	WGM02	CS02	CS01	CS00	104
0x24 (0x44)	TCCR0A	COM0A1	COM0A0	COM0B1	COM0B0	-	-	WGM01	WGM00	105
0x23 (0x43)	GTCCR	TSM	-	-	-	-	-	PSRASY	PSRSYNC	157
0x22 (0x42)	EEARH	-	-	-	-	EEPROM Address Register High Byte				24
0x21 (0x41)	EEARL	EEPROM Address Register Low Byte								24
0x20 (0x40)	EEDR	EEPROM Data Register								24
0x1F (0x3F)	EECR	-	-	EEPM1	EEPM0	EERIE	EEMPE	EEPE	EERE	24
0x1E (0x3E)	GPIOR0	General Purpose I/O Register 0								29
0x1D (0x3D)	EIMSK	-	-	-	-	-	INT2	INT1	INT0	68
0x1C (0x3C)	EIFR	-	-	-	-	-	INTF2	INTF1	INTF0	68
0x1B (0x3B)	PCIFR	-	-	-	-	PCIF3	PCIF2	PCIF1	PCIF0	69
0x1A (0x3A)	Reserved	-	-	-	-	-	-	-	-	
0x19 (0x39)	Reserved	-	-	-	-	-	-	-	-	

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x18 (0x38)	TIFR3	-	-	ICF3	-	-	OCF3B	OCF3A	TOV3	136
0x17 (0x37)	TIFR2	-	-	-	-	-	OCF2B	OCF2A	TOV2	156
0x16 (0x36)	TIFR1	-	-	ICF1	-	-	OCF1B	OCF1A	TOV1	135
0x15 (0x35)	TIFR0	-	-	-	-	-	OCF0B	OCF0A	TOV0	106
0x14 (0x34)	Reserved	-	-	-	-	-	-	-	-	
0x13 (0x33)	Reserved	-	-	-	-	-	-	-	-	
0x12 (0x32)	Reserved	-	-	-	-	-	-	-	-	
0x11 (0x31)	Reserved	-	-	-	-	-	-	-	-	
0x10 (0x30)	Reserved	-	-	-	-	-	-	-	-	
0x0F (0x2F)	Reserved	-	-	-	-	-	-	-	-	
0x0E (0x2E)	Reserved	-	-	-	-	-	-	-	-	
0x0D (0x2D)	Reserved	-	-	-	-	-	-	-	-	
0x0C (0x2C)	Reserved	-	-	-	-	-	-	-	-	
0x0B (0x2B)	PORTD	PORTD7	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	90
0x0A (0x2A)	DDRD	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	90
0x09 (0x29)	PIND	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	90
0x08 (0x28)	PORTC	PORTC7	PORTC6	PORTC5	PORTC4	PORTC3	PORTC2	PORTC1	PORTC0	90
0x07 (0x27)	DDRC	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	90
0x06 (0x26)	PINC	PINC7	PINC6	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0	90
0x05 (0x25)	PORTB	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	89
0x04 (0x24)	DDRB	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	89
0x03 (0x23)	PINB	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	90
0x02 (0x22)	PORTA	PORTA7	PORTA6	PORTA5	PORTA4	PORTA3	PORTA2	PORTA1	PORTA0	89
0x01 (0x21)	DDRA	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0	89
0x00 (0x20)	PINA	PINA7	PINA6	PINA5	PINA4	PINA3	PINA2	PINA1	PINA0	89

Notes:
1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
2. I/O registers within the address range $00 - $1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions.
3. Some of the status flags are cleared by writing a logical one to them. Note that the CBI and SBI instructions will operate on all bits in the I/O register, writing a one back into any flag read as set, thus clearing the flag. The CBI and SBI instructions work with registers 0x00 to 0x1F only.
4. When using the I/O specific commands IN and OUT, the I/O addresses $00 - $3F must be used. When addressing I/O registers as data space using LD and ST instructions, $20 must be added to these addresses. The ATmega164A/164PA/324A/324PA/644A/644PA/1284/1284P is a complex microcontroller with more peripheral units than can be supported within the 64 location reserved in Opcode for the IN and OUT instructions. For the Extended I/O space from $60 - $FF, only the ST/STS/STD and LD/LDS/LDD instructions can be used.
5. USART in SPI Master Mode.
6. Only available in the ATmega164PA/324PA/644PA/1284P.
7. Only available in the ATmega1284/1284P

8. Instruction set summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
ARITHMETIC AND LOGIC INSTRUCTIONS					
ADD	Rd, Rr	Add two Registers	Rd ← Rd + Rr	Z,C,N,V,H	1
ADC	Rd, Rr	Add with Carry two Registers	Rd ← Rd + Rr + C	Z,C,N,V,H	1
ADIW	Rdl,K	Add Immediate to Word	Rdh:Rdl ← Rdh:Rdl + K	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract two Registers	Rd ← Rd - Rr	Z,C,N,V,H	1
SUBI	Rd, K	Subtract Constant from Register	Rd ← Rd - K	Z,C,N,V,H	1
SBC	Rd, Rr	Subtract with Carry two Registers	Rd ← Rd - Rr - C	Z,C,N,V,H	1
SBCI	Rd, K	Subtract with Carry Constant from Reg.	Rd ← Rd - K - C	Z,C,N,V,H	1
SBIW	Rdl,K	Subtract Immediate from Word	Rdh:Rdl ← Rdh:Rdl - K	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND Registers	Rd ← Rd • Rr	Z,N,V	1
ANDI	Rd, K	Logical AND Register and Constant	Rd ← Rd • K	Z,N,V	1
OR	Rd, Rr	Logical OR Registers	Rd ← Rd v Rr	Z,N,V	1
ORI	Rd, K	Logical OR Register and Constant	Rd ← Rd v K	Z,N,V	1
EOR	Rd, Rr	Exclusive OR Registers	Rd ← Rd ⊕ Rr	Z,N,V	1
COM	Rd	One's Complement	Rd ← 0xFF – Rd	Z,C,N,V	1
NEG	Rd	Two's Complement	Rd ← 0x00 – Rd	Z,C,N,V,H	1
SBR	Rd,K	Set Bit(s) in Register	Rd ← Rd v K	Z,N,V	1
CBR	Rd,K	Clear Bit(s) in Register	Rd ← Rd • (0xFF - K)	Z,N,V	1
INC	Rd	Increment	Rd ← Rd + 1	Z,N,V	1
DEC	Rd	Decrement	Rd ← Rd – 1	Z,N,V	1
TST	Rd	Test for Zero or Minus	Rd ← Rd • Rd	Z,N,V	1
CLR	Rd	Clear Register	Rd ← Rd ⊕ Rd	Z,N,V	1
SER	Rd	Set Register	Rd ← 0xFF	None	1
MUL	Rd, Rr	Multiply Unsigned	R1:R0 ← Rd x Rr	Z,C	2
MULS	Rd, Rr	Multiply Signed	R1:R0 ← Rd x Rr	Z,C	2
MULSU	Rd, Rr	Multiply Signed with Unsigned	R1:R0 ← Rd x Rr	Z,C	2
FMUL	Rd, Rr	Fractional Multiply Unsigned	R1:R0 ← (Rd x Rr) << 1	Z,C	2
FMULS	Rd, Rr	Fractional Multiply Signed	R1:R0 ← (Rd x Rr) << 1	Z,C	2
FMULSU	Rd, Rr	Fractional Multiply Signed with Unsigned	R1:R0 ← (Rd x Rr) << 1	Z,C	2
BRANCH INSTRUCTIONS					
RJMP	k	Relative Jump	PC ← PC + k + 1	None	2
IJMP		Indirect Jump to (Z)	PC ← Z	None	2
JMP	k	Direct Jump	PC ← k	None	3
RCALL	k	Relative Subroutine Call	PC ← PC + k + 1	None	3
ICALL		Indirect Call to (Z)	PC ← Z	None	3
CALL	k	Direct Subroutine Call	PC ← k	None	4
RET		Subroutine Return	PC ← STACK	None	4
RETI		Interrupt Return	PC ← STACK	I	4
CPSE	Rd,Rr	Compare, Skip if Equal	if (Rd = Rr) PC ← PC + 2 or 3	None	1/2/3
CP	Rd,Rr	Compare	Rd – Rr	Z, N,V,C,H	1
CPC	Rd,Rr	Compare with Carry	Rd – Rr – C	Z, N,V,C,H	1
CPI	Rd,K	Compare Register with Immediate	Rd – K	Z, N,V,C,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b)=0) PC ← PC + 2 or 3	None	1/2/3
SBRS	Rr, b	Skip if Bit in Register is Set	if (Rr(b)=1) PC ← PC + 2 or 3	None	1/2/3
SBIC	P, b	Skip if Bit in I/O Register Cleared	if (P(b)=0) PC ← PC + 2 or 3	None	1/2/3
SBIS	P, b	Skip if Bit in I/O Register is Set	if (P(b)=1) PC ← PC + 2 or 3	None	1/2/3
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then PC←PC+k + 1	None	1/2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then PC←PC+k + 1	None	1/2
BREQ	k	Branch if Equal	if (Z = 1) then PC ← PC + k + 1	None	1/2
BRNE	k	Branch if Not Equal	if (Z = 0) then PC ← PC + k + 1	None	1/2
BRCS	k	Branch if Carry Set	if (C = 1) then PC ← PC + k + 1	None	1/2
BRCC	k	Branch if Carry Cleared	if (C = 0) then PC ← PC + k + 1	None	1/2
BRSH	k	Branch if Same or Higher	if (C = 0) then PC ← PC + k + 1	None	1/2
BRLO	k	Branch if Lower	if (C = 1) then PC ← PC + k + 1	None	1/2
BRMI	k	Branch if Minus	if (N = 1) then PC ← PC + k + 1	None	1/2
BRPL	k	Branch if Plus	if (N = 0) then PC ← PC + k + 1	None	1/2
BRGE	k	Branch if Greater or Equal, Signed	if (N ⊕ V= 0) then PC ← PC + k + 1	None	1/2
BRLT	k	Branch if Less Than Zero, Signed	if (N ⊕ V= 1) then PC ← PC + k + 1	None	1/2
BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then PC ← PC + k + 1	None	1/2
BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then PC ← PC + k + 1	None	1/2
BRTS	k	Branch if T Flag Set	if (T = 1) then PC ← PC + k + 1	None	1/2
BRTC	k	Branch if T Flag Cleared	if (T = 0) then PC ← PC + k + 1	None	1/2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then PC ← PC + k + 1	None	1/2

Mnemonics	Operands	Description	Operation	Flags	#Clocks
MCU CONTROL INSTRUCTIONS					
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep function)	None	1
WDR		Watchdog Reset	(see specific descr. for WDR/timer)	None	1
BREAK		Break	For On-chip Debug Only	None	N/A

9. Ordering information

9.1 Atmel ATmega164A

Speed [MHz] (3)	Power supply	Ordering code (2)	Package (1)	Operational range
20	1.8 - 5.5V	ATmega164A-AU ATmega164A-AUR(5) ATmega164A-PU ATmega164A-MU ATmega164A-MUR(5) ATmega164A-MCH(4) ATmega164A-MCHR(4)(5) ATmega164A-CU ATmega164A-CUR(5)	44A 44A 40P6 44M1 44M1 44MC 44MC 49C2 49C2	Industrial (-40°C to 85°C)

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For Speed vs. V_{CC} see ”Speed grades” on page 324.
4. NiPdAu Lead Finish.
5. Tape & Reel.

Package Type	
44A	44-lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP)
40P6	40-pin, 0.600” Wide, Plastic Dual Inline Package (PDIP)
44M1	44-pad, 7 × 7 × 1.0mm body, lead pitch 0.50mm, Thermally Enhanced Plastic Very Thin Quad Flat No-Lead (VQFN)
44MC	44-lead (2-row Staggered), 5 × 5 × 1.0mm body, 2.60 × 2.60mm Exposed Pad, Quad Flat No-Lead Package (QFN)
49C2	49-ball, (7 × 7 Array) 0.65mm Pitch, 5 × 5 × 1mm, Very Thin, Fine-Pitch Ball Grid Array Package (VFBGA)

9.2 Atmel ATmega164PA

Speed [MHz] (3)	Power supply	Ordering code (2)	Package (1)	Operational range
20	1.8 - 5.5V	ATmega164PA-AU ATmega164PA-AUR(5) ATmega164PA-PU ATmega164PA-MU ATmega164PA-MUR(5) ATmega164PA-MCH(4) ATmega164PA-MCHR(4)(5) ATmega164PA-CU ATmega164PA-CUR(5)	44A 44A 40P6 44M1 44M1 44MC 44MC 49C2 49C2	Industrial (-40°C to 85°C)
20	1.8 - 5.5V	ATmega164PA-AN ATmega164PA-ANR(5) ATmega164PA-PN ATmega164PA-MN ATmega164PA-MNR(5)	44A 44A 40P6 44M1 44M1	Industrial (-40°C to 105°C)

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For Speed vs. V_{CC} see ”Speed grades” on page 324.
4. NiPdAu Lead Finish.
5. Tape & Reel.

Package Type	
44A	44-lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP)
40P6	40-pin, 0.600” Wide, Plastic Dual Inline Package (PDIP)
44M1	44-pad, 7 × 7 × 1.0mm body, lead pitch 0.50mm, Thermally Enhanced Plastic Very Thin Quad Flat No-Lead (VQFN)
44MC	44-lead (2-row Staggered), 5 × 5 × 1.0mm body, 2.60 × 2.60mm Exposed Pad, Quad Flat No-Lead Package (QFN)
49C2	49-ball, (7 × 7 Array) 0.65mm Pitch, 5 × 5 × 1mm, Very Thin, Fine-Pitch Ball Grid Array Package (VFBGA)

9.3 Atmel ATmega324A

Speed [MHz] (3)	Power supply	Ordering code (2)	Package (1)	Operational range
20	1.8 - 5.5V	ATmega324A-AU ATmega324A-AUR(5) ATmega324A-PU ATmega324A-MU ATmega324A-MUR(5) ATmega324A-MCH(4) ATmega324A-MCHR(4)(5) ATmega324A-CU ATmega324A-CUR(5)	44A 44A 40P6 44M1 44M1 44MC 44MC 49C2 49C2	Industrial (-40°C to 85°C)

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For Speed vs. V_{CC} see ”Speed grades” on page 324.
4. NiPdAu Lead Finish.
5. Tape & Reel.

Package Type	
44A	44-lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP)
40P6	40-pin, 0.600” Wide, Plastic Dual Inline Package (PDIP)
44M1	44-pad, 7 × 7 × 1.0mm body, lead pitch 0.50mm, Thermally Enhanced Plastic Very Thin Quad Flat No-Lead (VQFN)
44MC	44-lead (2-row Staggered), 5 × 5 × 1.0mm body, 2.60 × 2.60mm Exposed Pad, Quad Flat No-Lead Package (QFN)
49C2	49-ball, (7 × 7 Array) 0.65mm Pitch, 5 × 5 × 1mm, Very Thin, Fine-Pitch Ball Grid Array Package (VFBGA)

9.4 Atmel ATmega324PA

Speed [MHz] (3)	Power supply	Ordering code (2)	Package (1)	Operational range
20	1.8 - 5.5V	ATmega324PA-AU ATmega324PA-AUR(5) ATmega324PA-PU ATmega324PA-MU ATmega324PA-MUR(5) ATmega324PA-MCH(4) ATmega324PA-MCHR(4)(5) ATmega324PA-CU ATmega324PA-CUR(5)	44A 44A 40P6 44M1 44M1 44MC 44MC 49C2 49C2	Industrial (-40°C to 85°C)
20	1.8 - 5.5V	ATmega324PA-AN ATmega324PA-ANR(5) ATmega324PA-PN ATmega324PA-MN ATmega324PA-MNR(5)	44A 44A 40P6 44M1 44M1	Industrial (-40°C to 105°C)

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For Speed vs. V_{CC} see ”Speed grades” on page 324.
4. NiPdAu Lead Finish.
5. Tape & Reel.

Package Type	
44A	44-lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP)
40P6	40-pin, 0.600” Wide, Plastic Dual Inline Package (PDIP)
44M1	44-pad, 7 × 7 × 1.0mm body, lead pitch 0.50mm, Thermally Enhanced Plastic Very Thin Quad Flat No-Lead (VQFN)
44MC	44-lead (2-row Staggered), 5 × 5 × 1.0mm body, 2.60 × 2.60mm Exposed Pad, Quad Flat No-Lead Package (QFN)
49C2	49-ball, (7 × 7 Array) 0.65mm Pitch, 5 × 5 × 1mm, Very Thin, Fine-Pitch Ball Grid Array Package (VFBGA)

9.5 Atmel ATmega644A

Speed [MHz](3)	Power supply	Ordering code(2)	Package(1)	Operational range
20	1.8 - 5.5V	ATmega644A-AU ATmega644A-AUR(4) ATmega644A-PU ATmega644A-MU ATmega644A-MUR(4)	44A 44A 40P6 44M1 44M1	Industrial (-40°C to 85°C)

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For Speed vs. V_{CC} see ”Speed grades” on page 324.
4. Taper & Reel.

Package Type	
44A	44-lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP)
40P6	40-pin, 0.600” Wide, Plastic Dual Inline Package (PDIP)
44M1	44-pad, 7 × 7 × 1.0mm body, lead pitch 0.5 mm, Thermally Enhanced Plastic Very Thin Quad Flat No-Lead (VQFN)

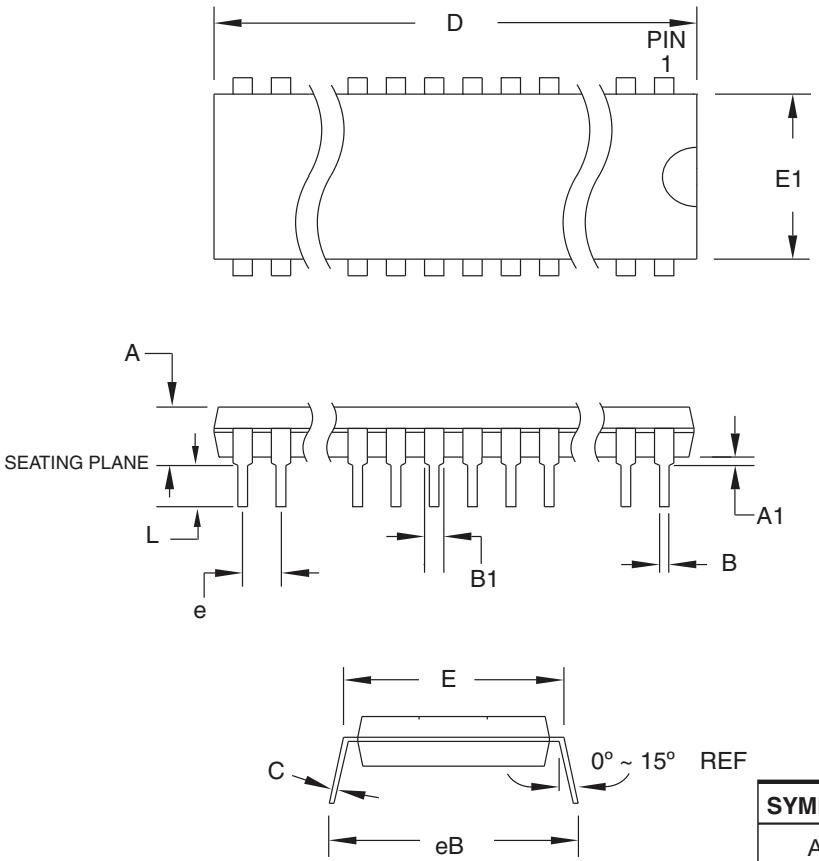
9.8 Atmel ATmega1284P

Speed [MHz] (3)	Power supply	Ordering code (2)	Package (1)	Operational range
20	1.8 - 5.5V	ATmega1284P-AU ATmega1284P-AUR(4) ATmega1284P-PU ATmega1284P-MU ATmega1284P-MUR(4)	44A 44A 40P6 44M1 44M1	Industrial (-40°C to 85°C)
20	1.8 - 5.5V	ATmega1284P-AN ATmega1284P-ANR(4) ATmega1284P-PN ATmega1284P-MN ATmega1284P-MNR(4)	44A 44A 40P6 44M1 44M1	Industrial (-40°C to 105°C)

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For Speed vs. V_{CC} see ”Speed grades” on page 324.
4. Tape & Reel.

Package Type	
44A	44-lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP)
40P6	40-pin, 0.600” Wide, Plastic Dual Inline Package (PDIP)
44M1	44-pad, 7 × 7 × 1.0mm body, lead pitch 0.50mm, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)

10.2 40P6



COMMON DIMENSIONS
(Unit of Measure = mm)

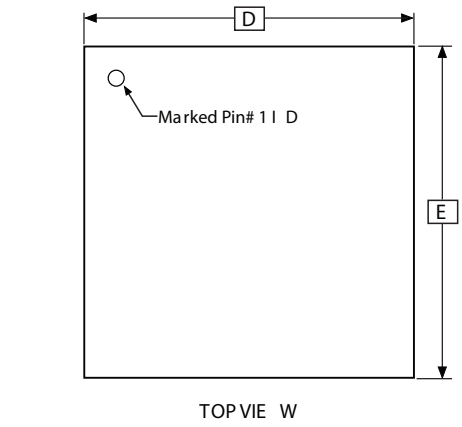
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.826	
A1	0.381	–	–	
D	52.070	–	52.578	Note 2
E	15.240	–	15.875	
E1	13.462	–	13.970	Note 2
B	0.356	–	0.559	
B1	1.041	–	1.651	
L	3.048	–	3.556	
C	0.203	–	0.381	
eB	15.494	–	17.526	
e	2.540 TYP			

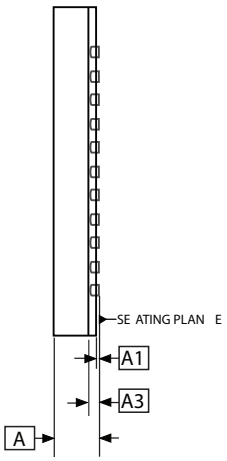
Notes:
1. This package conforms to JEDEC reference MS-011, Variation AC.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25mm (0.010").

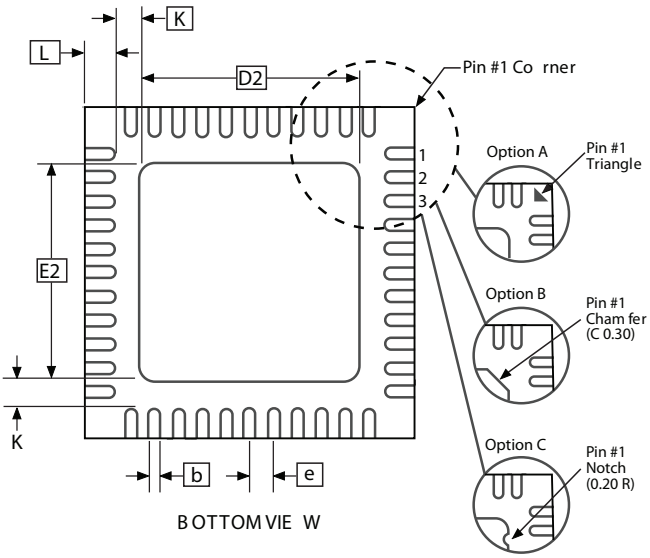
13/02/2014

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE	DRAWING NO.	REV.
	40P6, 40-lead (0.600"/15.24mm Wide) Plastic Dual Inline Package (PDIP)	40P6	C

10.3 44M1







Note: JEDEC Standard MO-220, Fig . 1 (S AW Singulation) VKKD-3 .

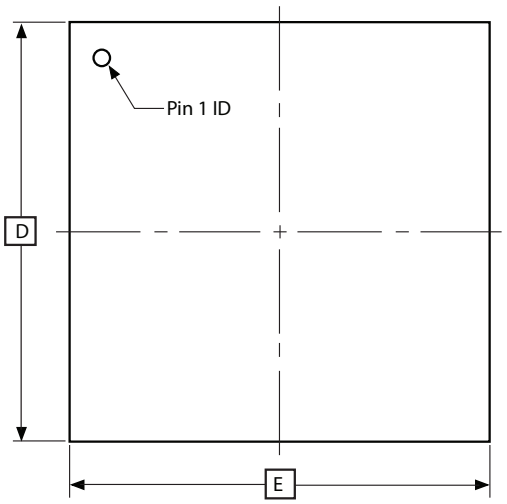
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	–	0.02	0.05	
A3		0.20 REF		
b	0.18	0.23	0.30	
D	6.90	7.00	7.10	
D2	5.00	5.20	5.40	
E	6.90	7.00	7.10	
E2	5.00	5.20	5.40	
e		0.50 BSC		
L	0.59	0.64	0.69	
K	0.20	0.26	0.41	

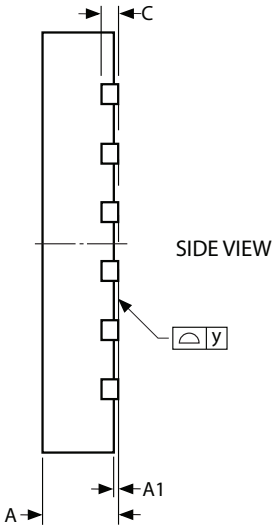
9/26/08

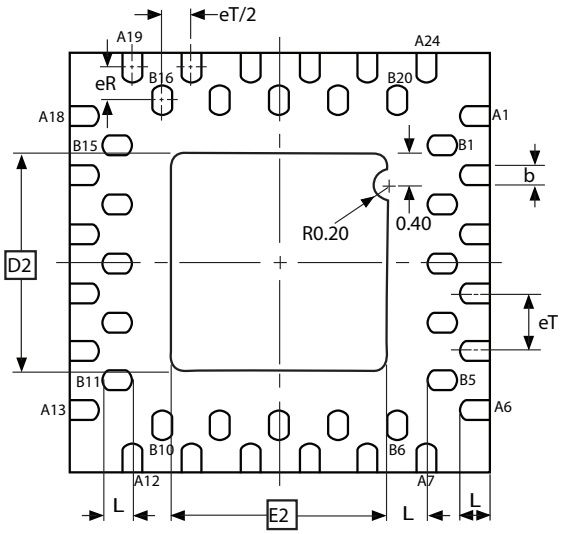
Atmel Package Drawing Contact: avr@atmel.com	TITLE 44M1, 44-pad, 7 x 7 x 1.0mm body, lead pitch 0.50mm, 5.20mm exposed pad, thermally enhanced plastic very thin quad flat no lead package (VQFN)	GPC ZWS	DRAWING NO. 44M1	REV. H

10.4 44MC



TOP VIEW





BOTTOM VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	0.00	0.02	0.05	
b	0.18	0.23	0.30	
C		0.20 REF		
D	4.90	5.00	5.10	
D2	2.55	2.60	2.65	
E	4.90	5.00	5.10	
E2	2.55	2.60	2.65	
eT	–	0.70	–	
eR	–	0.40	–	
K	0.45	–	–	
L	0.30	0.35	0.40	
y	0.00	–	0.075	

Note: 1. The terminal #1 ID is a Laser-marked Feature.

9/13/07

Atmel	Package Drawing Contact: packagedrawings@atmel.com	TITLE 44MC, 44QFN (2-Row Staggered), 5 x 5 x 1.00 mm Body, 2.60 x 2.60 mm Exposed Pad, Quad Flat No Lead Package	DRA WING NO . 44MC	REV . A

12. Datasheet revision history

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

12.1 Rev. 8272G - 01/2015

1.	Updated Table 1-2 on page 5, Table 8-1 on page 25, Table 10-1 on page 42, Table 14-3 on page 79, Table 19-4 on page 187, Table 19-11 on page 192 and Table 28-16 on page 328 for formatting consistency errors
2.	Updated ”Ordering information” on page 17: – Added ordering information for ATmega164PA @105°C; ATmega324PA @ 105°C; ATmega324PA @105°C; ATmega644PA @ 105°C and ATmega1284P @ 105°C
3.	Updated the ”Packaging information” on page 25: – Replaced the drawing ”44M1” on page 27 by a correct package

12.2 Rev. 8272F - 08/2014

1.	Updated text in Section 13.2.8 ”PCMSK1 – Pin Change Mask Register 1” on page 70 to: “If PCINT15:8 is set and the PCIE1 bit in PCICR is set, pin change interrupt is enabled on the corresponding I/O pin.”
2.	Corrected description of PAGEMSB in Table 26-9 on page 281. The device has 64 words in a page and not 128.
3.	Corrected description of PAGEMSB in Table 26-12 on page 282. PAGESMB is 5 and the device has 64 words in a page and not 128. The page require six bits and not seven.
4.	Corrected values in Table 26-16 on page 284. PAGEMSB is 6. ZPAGEMSB is Z7 and PCPAGE is Z15:Z8
5.	Corrected value for PCPAGE in Table 27-7 on page 290. The correct value is PC[14:7]
6.	Updated description in Table 17-2 on page 151 to “Normal port operation, OC2A disconnected.”
7.	Updated Assembly code examples on for ”Watchdog Timer” on page 55. and onwards “out WDTCSR, r16” changed to “sts WDTCSR, r16” “in r16, WDTCSR” changed to “lds r16, WDTCSR” “idi r16, WDTCSR” changed to “lds r16, WDTCSR”
8.	Updated addresses 0x65 and 0x64 in Section 7. ”Register summary” on page 10.
9.	Removed notes 5 and 6 from Table 28-16 on page 328.
10.	Corrected values in Section 8. ”Instruction set summary” on page 14.Changed clock values for RCALL and ICALL to 2, for Call, Ret and RETI to 4. Also changed values in Section 7.7.1 ”Interrupt response time” on page 18.
11.	Updated layout, footer and back page according to template 0205/2014

12.3 Rev. 8272E - 04/2013

1.	Updated Figure 1-1 on page 3 and Figure 2-1 on page 6: T3 and T/C3 only available in ATmega1284/1284P.
2.	Updated descriptive text on page 6 to indicate that ATmega1284/1284P has four T/Cs.
3.	Updated the Assembly code example for WDT_off (p.56) following the ej# 705736.
4.	Added note in ”16-bit Timer/Counter1 and Timer/Counter3(1) with PWM” on page 107.
5.	Added ”Prescaler Reset” on page 112.
6.	Corrected three typo for Waveform generation mode (WGM) instead of MGM.
7.	Updated Table 23-6 on page 253. ADC Auto Trigger Source Selections, ADTS=0b011, the statement is Timer/Counter0 Compare Match A.
8.	Updated Table 27-18 on page 310. Command for 6d Poll for Fuse Write Complete: 0111011_00000000
9.	Updated the table notes of the Table 28-1 on page 318.
10.	Updated ”Register summary” on page 10. Added table note 7: Only available in ATmega1284/1284P.

12.4 Rev. 8272D - 05/12

1.	Updated ”Power-down mode” on page 44.
2.	Updated ”Overview” on page 67.
3.	Corrected references for Bit 2, Bit 1, and Bit 0 in Section ”UCSRnC – USART MSPIM Control and Status Register n C” on page 201.
4.	Several small corrections throughout the whole document made according to the template
5.	Notes in Table 27-17 on page 304 have been corrected
6.	Note (1) in Table 28-3 on page 320 is added

12.5 Rev. 8272C - 06/11

1.	Updated ”Atmel ATmega1284P DC characteristics” on page 323.

12.6 Rev. 8272B - 05/11

1.	Added Atmel QTouch Library Support and QTouch Sensing Capability Features.
2.	Replaced the Figure 1-1 on page 3 by an updated “Pinout.” that includes Timer/Counter3.
3.	Replaced the Figure 7-1 on page 10 by an updated “Block diagram of the AVR architecture.” that includes Timer/Counter3.
4.	Added ”RAMPZ – Extended Z-pointer Register for ELPM/SPM(1)” on page 15.
5.	Added ”PRR1 – Power Reduction Register 1” on page 49.
6.	Renamed PRR to ”PRR0 – Power Reduction Register 0” on page 48.
7.	Updated ”PCIFR – Pin Change Interrupt Flag Register” on page 69. PCICR replaces EIMSR in the PCIF3, PCIF2, PCIF1 and PCIF0 bit description.
8.	Updated ”PCMSK3 – Pin Change Mask Register 3” on page 70. PCIE3 replaces PCIE2 in the bit description.
9.	Updated ”Alternate Functions of Port B” on page 80 to include Timer/Counter3
10.	Updated ”Alternate Functions of Port D” on page 86 to include Timer/Counter3
11.	Added ”TCNT3H and TCNT3L –Timer/Counter3” on page 132